To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M51362SP

PLL–SPLIT VIF/SIF

DESCRIPTION

The M51362SP is a semiconductor IC consisting of IF signal processor suitable for color TV sets and VCRs with AV which is a revision of M51365SP.
The circuit includes VIF amplifier, Video detector, VCO, APC detector, AFT, video equalizer, IF/RF AGC, SIF detector, SIF limiter, FM detector functions.

FEATURES

- A full synchronous detector circuit using PLL as video detector provides excellent DG, DP, 920kHz beat and cross color characteristics.
- The PLL–SPLIT method in which video IF and audio IF signal processings are separated and VCO output is used to obtain intercarrier provides good sound sensitivity and reduces buzz. In consumer sets, intercarrier is also available from the video detector output.
- Built-in video equalizer is suitable for VCRs and color TV sets equipped with video output terminals.
- The quadrature detector circuit for FM detector has good linearity with a simple coil.
- The M51362SP has better video S/N ratio than M51365SP by 2~4dB.

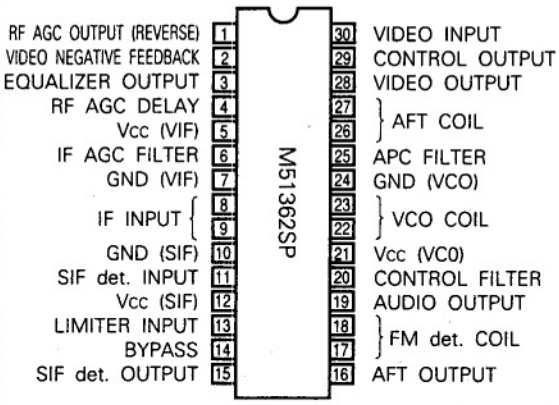
APPLICATIONS

TV sets, VCR tuners

RECOMMENDED OPERATING CONDITIONS

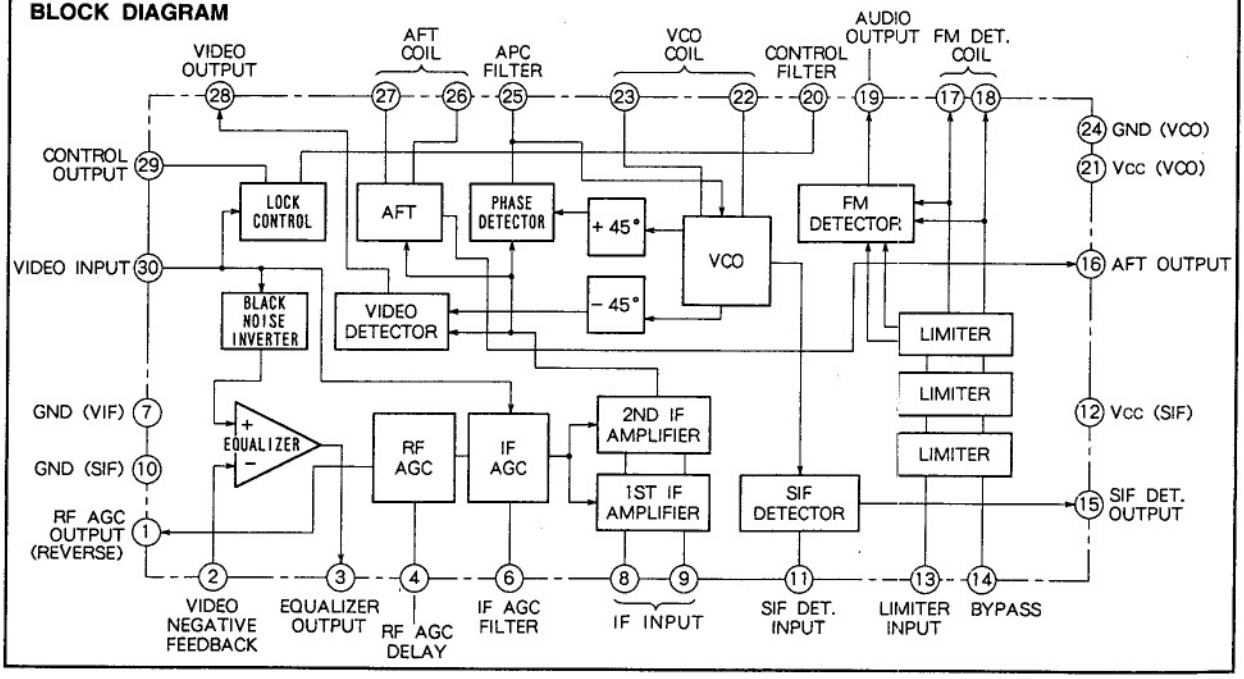
Supply voltage range ..... 8~10V
Rated supply voltage 9V

PIN CONFIGURATION (TOP VIEW)



Outline 30P4B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	14	V
P_d	Power dissipation	1250	mW
T_{opr}	Operating temperature	−20~75	℃
T_{stg}	Storage temperature	−40~125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, Vcc = 9V unless otherwise noted)

VIF SECTION

Symbol	Parameter	Test circuit	Test point	Test conditions: Input signal VIF	SIF1	External power supply (V) V_1	V_6	V_{20}	* Switches should usually be set to 1.	Limits Min.	Typ.	Max.	Unit
Icc (VIF)	Circuit current (VIF)	1	A1	–	–	3	–	–	SW1 = 2	33	45	57	mA
V_{28}	Video detector output DC voltage 1	1	TP9	–	–	3	0	–	SW3 = 2	3.4	3.75	4.1	V
V_3	Video detector output DC voltage 2	1	TP2	–	–	3	0	–	SW3 = 2	4.4	4.8	5.2	V
$V_{O\ det1}$	Video detector output 1	1	TP9	SG1	–	3	–	–		1.15	1.45	1.75	V_{P-P}
$V_{O\ det2}$	Video detector output 2	1	TP2	SG1	–	3	–	–		1.6	1.95	2.3	V_{P-P}
P/N	Video S/N	1	TP10	SG6	–	3	–	–	SW6 = 2 (note 1)	44	52		dB
Bw	Video frequency characteristics	1	TP9	SG3	–	3	–	–	(note 2)	5.5	7.5		MHz
$V_{in\ (min)}$	Input sensitivity	1	TP9	SG4	–	3	–	–	(note 3)		46	51	dB μ
$V_{in\ (max)}$	Maximum allowable input	1	TP9	SG5	–	3	–	–	(note 4)	107	110		dB μ
GR	AGC control range	1	–	–	–	–	–	–	(note 5)	58	64		dB
V_{IH}	IF AGC maximum voltage	1	TP3	–	–	3	–	–		6.5	8.6		V
$V_{I\ (80dB\mu)}$	IF AGC (80dB μ)	1	TP3	SG6	–	3	–	–		4.3	4.9	5.5	V
V_{IL}	IF AGC minimum voltage	1	TP3	SG7	–	3	–	–		3.4	3.9	4.4	V
$V_{O\ SIF-1}$	SIF det. 4.5MHz output (100dB μ)	1	TP4	SG2	SG8	3	–	–		104	109	114	dB μ
$V_{O\ SIF-2}$	SIF det. 4.5MHz output (80dB μ)	1	TP4	SG2	SG9	3	–	–		90	96	101	dB μ
V_{16}	AFT output voltage	1	TP5	–	–	3	0	–		3.2	4.3	5.4	V
μ	AFT detector sensitivity	1	TP5	SG10	–	3	–	–	(note 6)	48	70	92	mV/kHz
V_{16H}	AFT maximum voltage	1	TP5	SG10	–	3	–	–	(note 7)	8	8.7		V
V_{16L}	AFT minimum voltage	1	TP5	SG10	–	3	–	–	(note 8)		0.38	1.0	V
V_{1H}	RF AGC maximum voltage	1	TP1	SG2	–	2	–	–		7	7.85		V
V_{1L}	RF AGC minimum voltage	1	TP1	SG2	–	4	–	–			0	1.0	V
CL-U1	Capture range (U)	1	TP9	SG11	–	3	–	–	(note 9)	0.45	0.8		MHz
CL-L1	Capture range (L)	1	TP9	SG11	–	3	–	–	(note 10)	1.4	2.0		MHz
CL-T	Capture range (T)	1	–	–	–	–	–	–	(note 11)	2.0	2.8		MHz
CL-U2	Capture range (U)	1	TP9	SG11	–	3	–	–	SW5 = 2 (note 9)	0.45	0.8	1.2	MHz
CL-L2	Capture range (L)	1	TP9	SG11	–	3	–	–	SW5 = 2 (note 10)	1.0	1.6	2.2	MHz
V_{20TH}	Lock detector threshold voltage	1	TP8	–	–	3	5	Variable	SW3,4,5 = 2 (note 12)	3.6	4.0	4.4	V
V_{29L}	Minimum voltage at pin ㉙	1	TP8	–	–	3	5	Variable	SW3,4,5 = 2 (note 13)		0.05	0.5	V
FC1	EQ frequency characteristics 1	1	TP9 TP2	SG12	–	3	–	–	Refer to (note 14)	1.4	2.4	3.4	dB
FC2	EQ frequency characteristics 2	1	TP9 TP2	SG13	–	3	–	–	Refer to (note 14)	4.2	5.7	7.2	dB
FC3	EQ frequency characteristics 3	1	TP9 TP2	SG14	–	3	–	–	Refer to (note 14)	9.5	12.0	14.5	dB
IM	Intermodulation	1	TP9	SG15	–	3	Variable	–	SW3 = 2 Refer to (note 15)	34	39		dB
DG	DG	1	TP9	SG16	–	3	–	–	(note 16)		2	5	%
DP	DP	1	TP9	SG16	–	3	–	–	(note 16)		2	5	deg.

VIF SECTION (cont.)

Symbol	Parameter	Test circuit	Test point	Test conditions: Input signal VIF	Input signal SIF1	External power supply (V) V_1	V_6	V_{20}	* Switches should usually be set to 1.	Limits Min.	Typ.	Max.	Unit
V_{BTH}	Black spot inverter threshold level	1	TP2	SG1	–	3	Variable	–	SW3 = 2 (note 17)	1.3	1.7	2.1	V
V_{BCL}	Black spot inverter clamp level	1	TP2	SG1	–	3	Variable	–	SW3 = 2 (note 17)	3.7	4.2	4.7	V
V_{SYNC}	Sync tip level at pin ③	1	TP2	SG2	–	3	–	–		2.1	2.5	2.9	V
Rin (V)	VIF input resistance	2		90dBμ	–	3	–	–			0.9		kΩ
Cin (V)	VIF input capacitance	2		90dBμ	–	3	–	–			6.6		pF
Rin (S1)	SIF1 input resistance	2		–	90dBμ	3	–	–			2.1		kΩ
Cin (S1)	SIF1 input capacitance	2		–	90dBμ	3	–	–			2.5		pF

SIF SECTION

Symbol	Parameter	Test circuit	Test point	Test conditions: Input signal SIF2	External power supply (V) V_1	V_6	V_{20}	* Switches should usually be set to 1.	Limits Min.	Typ.	Max.	Unit
Icc (SIF)	Circuit current (SIF)	1	A2	–	0	–	–	SW2 = 2	6.1	8.7	11.4	mA
V_{19}	AF output DC voltage	1	TP6	–	0	–	–		4.1	4.9	5.7	V
V_{OAFMAX}	Maximum AF output	1	TP6	SG17	0	–	–		225	300	375	mVrms
THD_{AF}	AF output distortion	1	TP6	SG21	0	–	–			0.2	1.0	%
Vin (lim)	Input limiting sensitivity	1	TP6	SG18	0	–	–	(note 13)		34	42	dBμ
AMR	AMR	1	TP6	SG19	0	–	–	(note 19)	58	68		dB
S/N	AF S/N	1	TP6	SG20	0	–	–	(note 20)	58	73		dB

ELECTRICAL CHARACTERISTICS TEST METHOD

Note1. Video S/N "P/N"

a. Input SG6 in VIF IN.

b. The noise appearing at pin ㉘ is determined by measuring the r.m.s. voltage at TP10 through low pass filter (–3dB at 5MHz).

c. $P/N = 20 \log \left\{ \frac{\text{Vodet 1 } (V_{P\text{-}P}) \times 0.7}{\text{noise (Vrms)}} \right\}$,

where Vodet 1 denotes video detector output 1.

Note2. Video frequency characteristics "Bw"

a. Set SG3 as follows:

$f_1 = 58.75MHz$ ' $V_i = 90dB\mu$
$f_2 = 57.75MHz$ $V_i = 70dB\mu$ } mixed signal

b. Measure the element of 1MHz at TP9 and the result is defined as V_1.

c. Decrease the frequency until element (f_1–f_2) at TP9 reaches 3dB less than V_1. Then, read the frequency.

d. Bw = 58.75 – f_2 (MHz)

Note3. Input sensitivity "Vin (min)"

a. Input SG4 in VIF IN.

b. Decrease the SG4 level and the level at which detector output at pin ㉘ reaches 3dB less than Vodet 1 is defined as input sensitivity.

Note4. Maximum allowable input "$V_{in\ (max)}$"

a. Set SG5 to 90dBμ and input it in VIF IN.

b. Detector output at pin ㉘ at this time is defined as V_2.

c. Increase the voltage of SG5 and voltage at which detector output reaches 3dB less than V_2 is defined as maximum allowable input.

Note5 AGC control range "GR"

a. AGC control range is defined as follows:

GR = Maximum allowable input – Input sensitivity

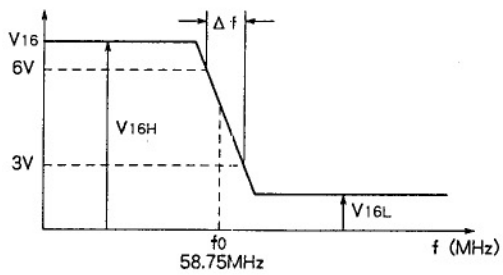
Note6 AFT detector sensitivity "μ"

a. Input SG10 in VIF IN.

b. Measure difference of frequency between 3.0V and 6.0V of DC voltage at TP5 and the difference is defined as Δf.

c. AFT detector sensitivity μ is defined as follows:

$$\mu = \frac{3000mV}{\Delta f\ (kHz)}\ (mV/kHz)$$



Note7. AFT maximum voltage "V_{16H}"

a. Maximum DC voltage in the figure on the previous page is defined as V_{16H}.

Note8. AFT minimum voltage "V_{16L}"

b. Minimum DC voltage in the figure on the previous page is defined as V_{16L}.

Note9. Capture range (U) "CL–U–1," "CL–U–2"

a. Input SG11 in VIF IN and increase the frequency till VCO lock is released.

b. Decrease the frequency of SG11 and the frequency at which VCO locks again is defined as fv (MHz).

c. Capture range (U) is defined as fv – 58.75 (MHz).

Note10. Capture range (L) "CL–L–1," "CL–L–2"

a. Input SG11 in VIF IN and decrease the frequency till VCO lock is released.

b. Increase the frequency of SG11 and the frequency at which VCO locks again is defined as f_L (MHz).

c. Capture range (L) is defined as 58.75 – f_L (MHz).

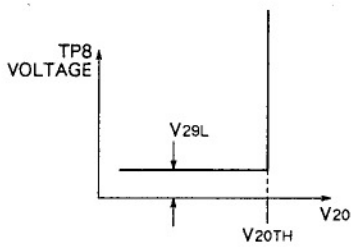
Note11. Capture range (T) "CT–T"

a. "CL–T" is defined as "CL–U–1" + "CL–L–1" (MHz).

Note12. Lock detector threshold voltage "V_{20TH}"

a. Set the voltage at V_{20} to 3V and observe TP8.

b. Increase the voltage at V_{20} and the point at which TP8 voltage changes drastically is defined as V_{20TH} (threshold 1V).



Note13. Minimum voltage at pin ㉙ "V_{29L}"

a. Minimum voltage in Note12 is defined as V_{29L}.

Note14. EQ frequency characteristics "FC1" "FC2" "FC3"

a. Input SG12, SG13 or SG14 to VIF IN.

b. Measure the level of element (f_1–f_2) at TP9 and it is defined as $V_{EQ\ IN}$ (dBμ).

c. Measure the level of element (f_1–f_2) at TP2 and it is defined as $V_{EQ\ OUT}$ (dBμ).

d. EQ frequency characteristics is defined as follows:
FC1~3 = $V_{EQ\ OUT}$ – $V_{EQ\ IN}$ (dB)

Note15. Intermodulation "IM"

a. Input SG15 in VIF IN.

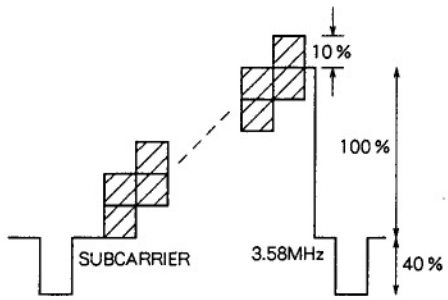
b. Observe TP9 with oscilloscope, and adjust the voltage of V_6 so that the minimum level of detector output waveform will come to 2V.

c. Observe TP9 with spectrum analyzer at this time, and the ratio of the 920kHz level to the 3.58MHz level is defined as intermodulation.

Note16. DG, DP "DG, DP"

a. Modulated waves of SG16 is generated by 87.5% video modulation of the 10-step waves as shown in the figure below.

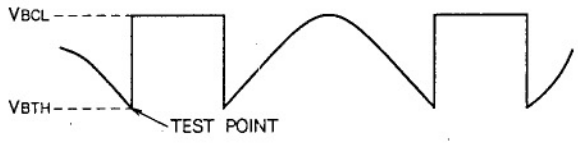
b. Measure DG and DP at TP9 with vectorscope.



Note17. Black spot inverter threshold level, clamp level "$V_{B\ TH}$, $V_{B\ CL}$"

a. Input SG1 in VIF IN.

b. By varying V_6, output the waveform as shown in the figure below to TP2 and measure each DC voltage.



Note18 Input limiting sensitivity "$V_{in\ (lim)}$"

a. Set SG18 to 80dBμ and input it in SIF2 IN.

b. Decrease the output level of SG18 until detector output at TP6 becomes 3dB smaller than $V_{O\ AF\ MAX.}$
The level of SG18 at this time is input limiting sensitivity.

Note19. AMR "AMR"

a. Input SG19 in SIF2 IN.

b. Measure the output voltage at TP6 and it is defined as V_{AM}.

c. AMR is defined as follows:

$$AMR = 20 \log \left\{ \frac{V_{O\ AF\ MAX}\ (mVrms)}{V_{AM}\ (mVrms)} \right\} (dB)$$

Note20. AF S/N "S/N"

a. Input SG20 in SIF2 IN.

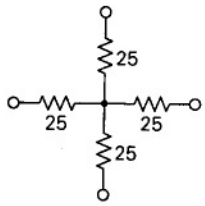
b. Measure the output voltage at TP6 and it is defined as V_N.

c. AF S/N is defined as follows:

$$S/N = 20 \log \left\{ \frac{V_{O\ AF\ MAX}\ (mVrms)}{V_N\ (mVrms)} \right\} (dB)$$

✱• Amplitude level of all AM modulated waves are the peak level of modulated waves.

• The following is used for the mixer:

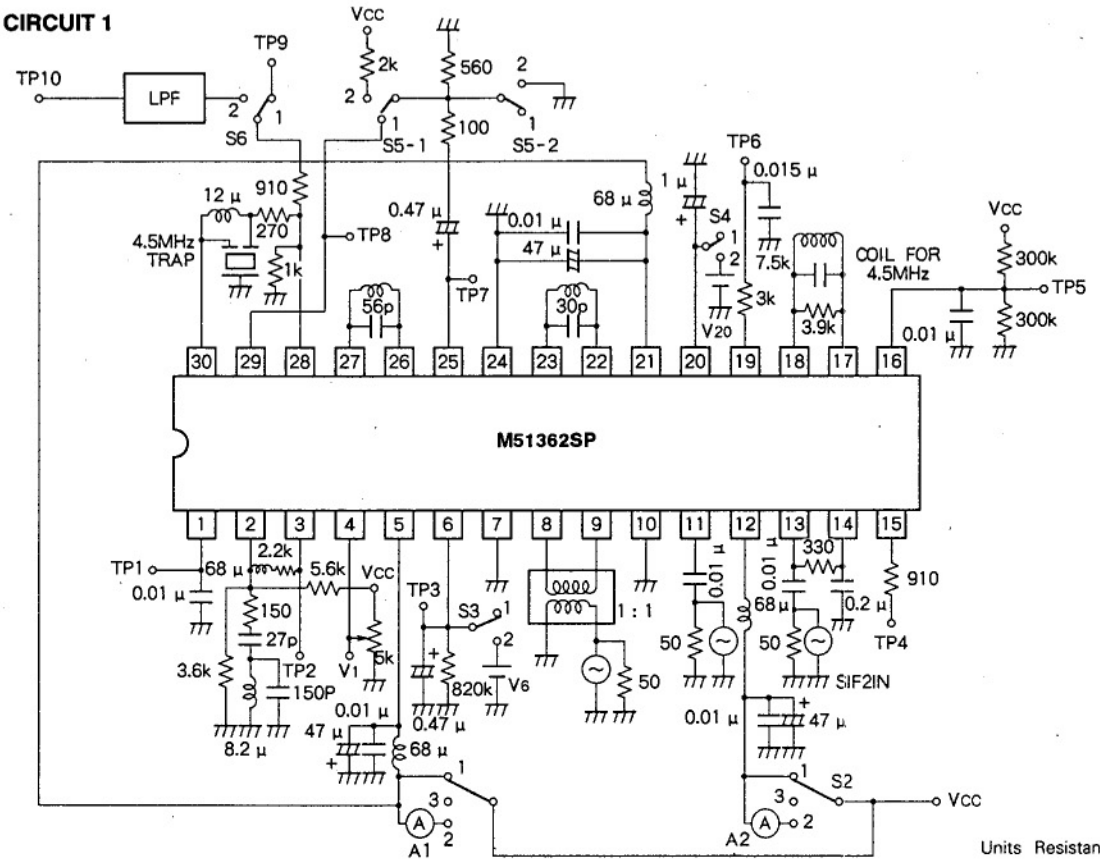


• With Vco coil, IF AGC 0V and non-input condition, adjust free run frequency to 58.75MHz.

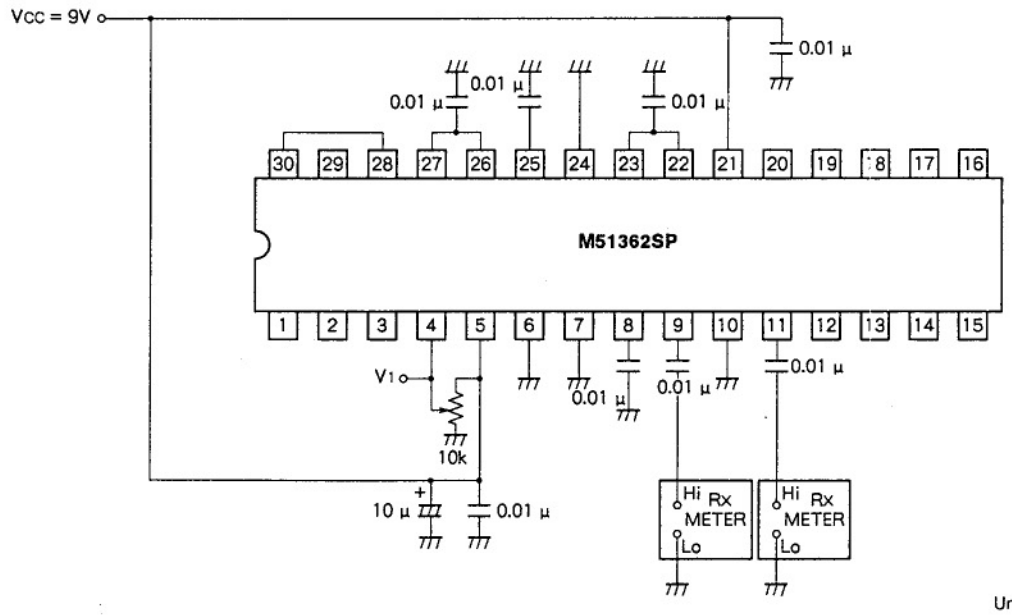
INPUT SIGNAL

SG No.	Signals (50 Ω termination)
SG1	f_0=58.75MHz V_i=90dBμ 77.78%AM (Corresponding to 87.5% video modulation fm=20kHz)
SG2	f_0 = 58.75MHz V_i = 90dBμ
SG3	f_1 = 58.75MHz V_i = 90dBμ f_2 = 53 ± 5MHz V_i = 70dBμ } mixed signal
SG4	f_0 = 58.75MHz V_i = Vaviable f_m = 20kHz 77.78% AM
SG5	f_0 = 58.75MHz V_i = Vaviable f_m = 20kHz 16% AM
SG6	f_0 = 58.75MHz V_i = 80dBμ
SG7	f_0 = 58.75MHz V_i = 110dBμ
SG8	f_0 = 54.25MHz V_i = 100dBμ
SG9	f_0 = 54.25MHz V_i = 80dBμ
SG10	f_0 = 58.75MHz ± 5MHz V_i = 90dBμ
SG11	f_0=58.75MHz ± 5MHz V_i=90dBμ f_m=20kHz 77.78%AM
SG12	f_1 = 58.75MHz V_i = 90dBμ f_2 = 58.25MHz V_i = 60dBμ } mixed signal
SG13	f_1 = 58.75MHz V_i = 90dBμ f_2 = 55.75MHz V_i = 60dBμ } mixed signal
SG14	f_1 = 58.75MHz V_i = 90dBμ f_2 = 54.75MHz V_i = 60dBμ } mixed signal
SG15	f_1 = 58.75MHz V_i = 90dBμ f_2 = 55.17MHz V_i = 80dBμ f_3 = 54.25MHz V_i = 80dBμ } mixed signal
SG16	f_0 = 58.75MHz standard 10 − step modulation m = 87.5% video modulation, sync tip level 90dBμ
SG17	f_0 = 4.5MHz ±25kHz dev V_i = 100dBμ f_m = 400Hz
SG18	f_0 = 4.5MHz ±25kHZ dev V_i = Vaviable f_m = 400Hz
SG19	f_0 = 4.5MHz V_i = 100dBμ 30% AM f_m = 400Hz
SG20	f_0 = 4.5MHz V_i = 100dBμ
SG21	f_0 = 4.5MHz V_i = 100dBμ f_m = 400Hz ± 7.5kHz dev

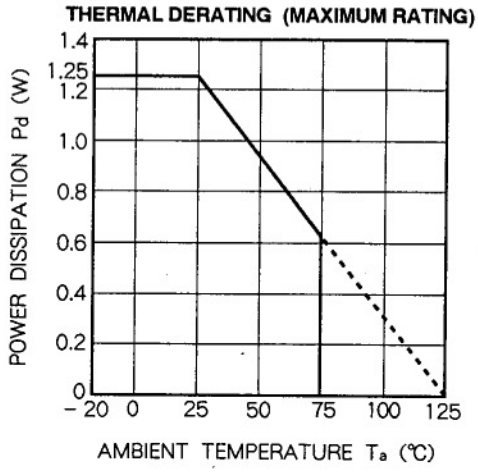
TEST CIRCUIT 1



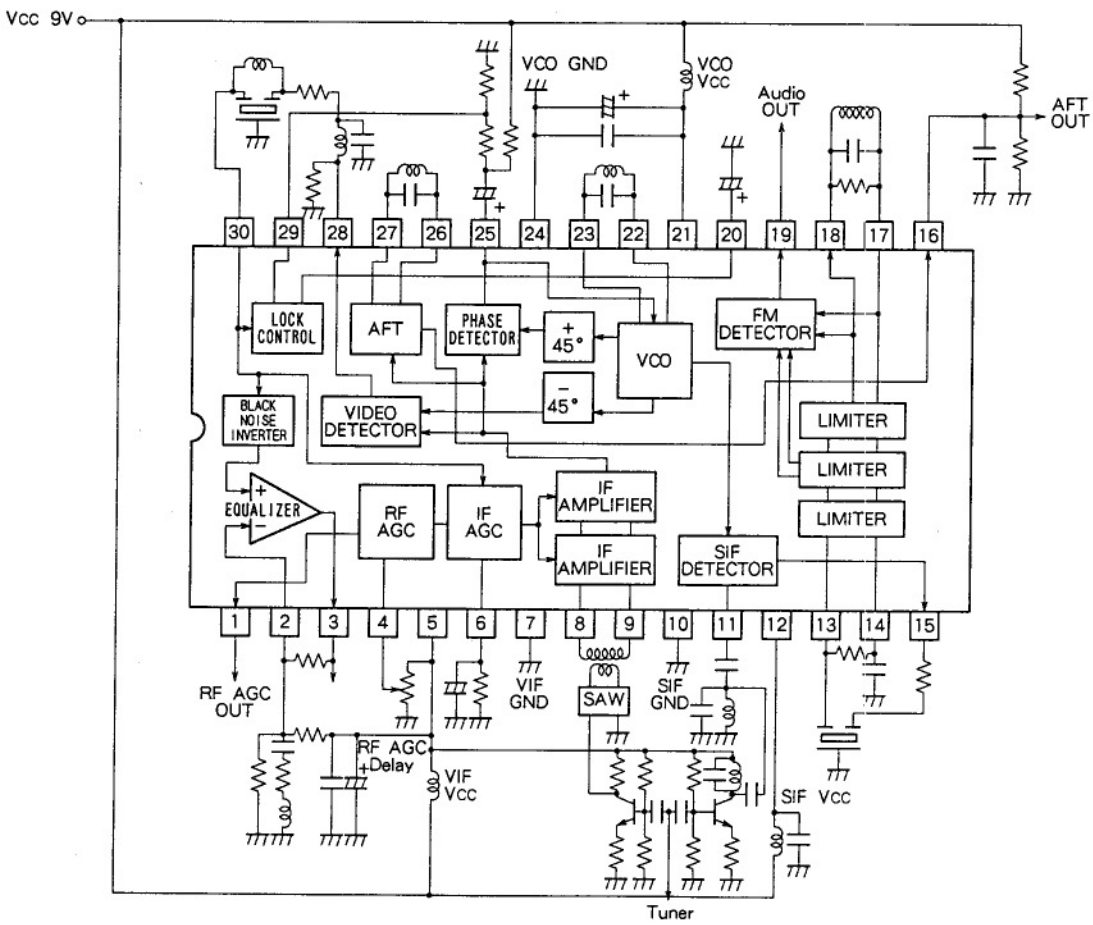
TEST CIRCUIT 2



TYPICAL CHARACTERISTICS



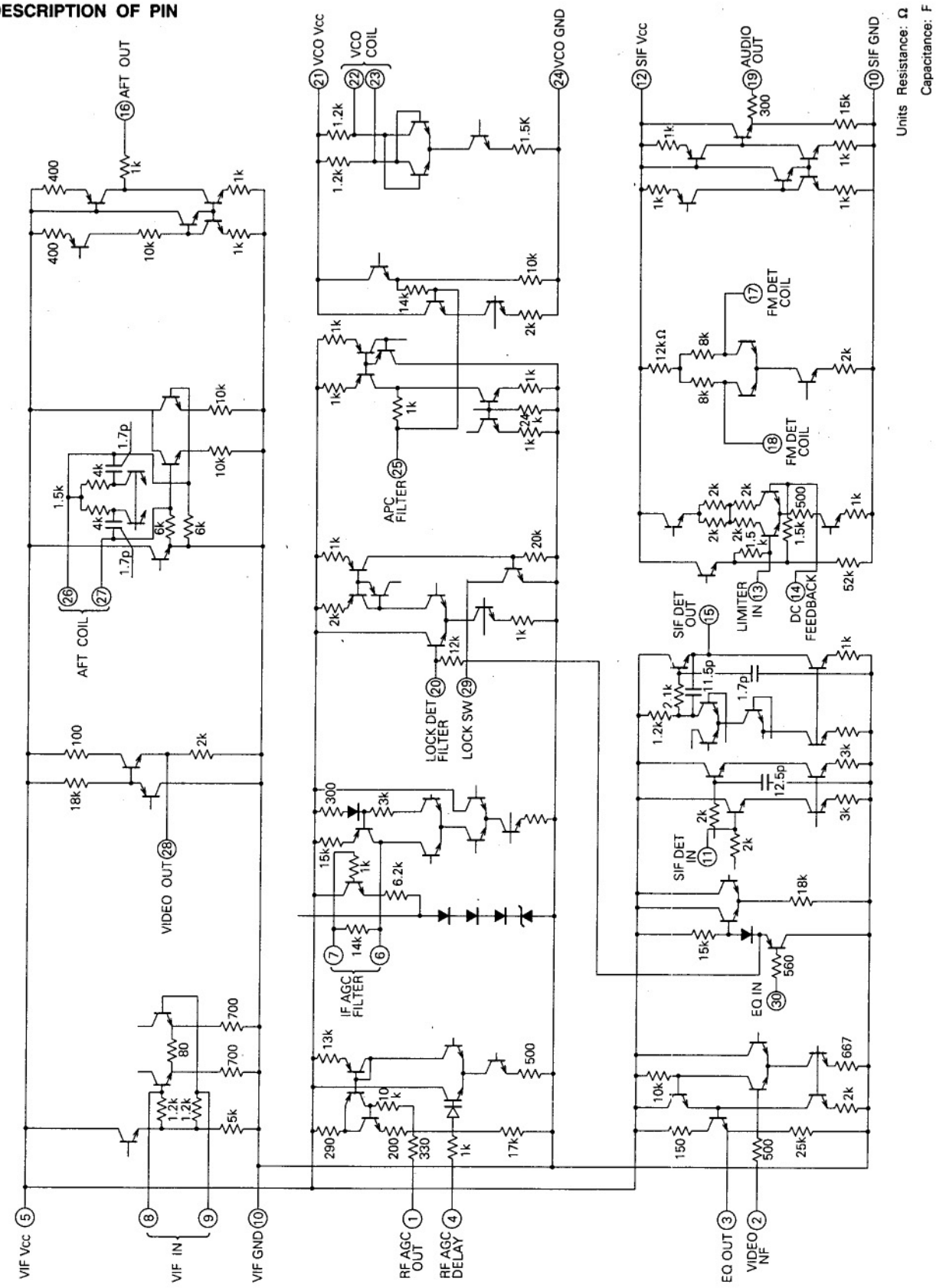
APPLICATION EXAMPLE



Units Resistance: Ω

Capacitance: F

DESCRIPTION OF PIN



PRECAUTIONS FOR APPLICATION

1. VIF Amplifier

The VIF amplifier is a two-stage amplifier without DC feedback.

With a gain of approx. 40dB, the VIF amplifier is connected to a video detector via an internal capacitor.

Maximum input amplitude is determined by the input dynamic range of the VIF amplifier, allowing up to 110dBμ input. During excessive input, surpassing this limit will cause the linearity to worsen, while leaving amplitude unchanged.

Since gain control has the characteristic that AGC speed is fastest in the range 50~60dBμ, to prevent sag, select an appropriate filter time constant.

IF input impedance is approx. 1KΩ and must be input in balanced type.

2. Video Detector, PLL Section

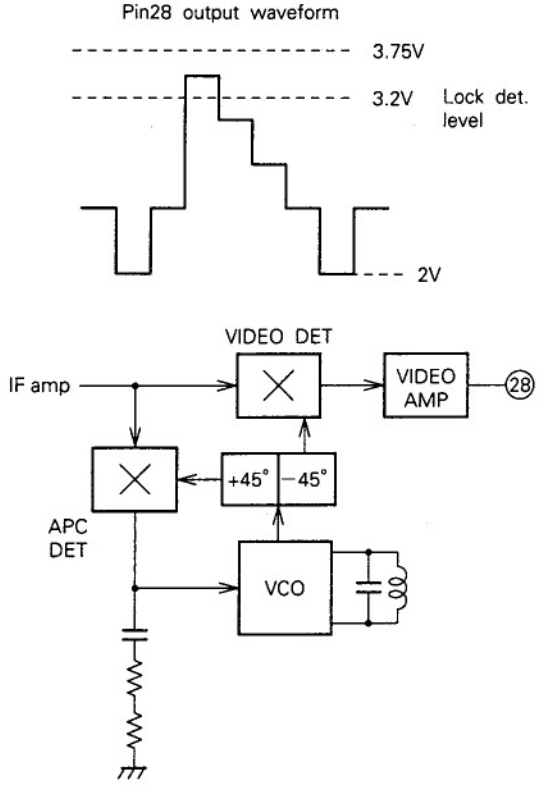
The PLL system produces a pure carrier wave. The PLL is locked as shown in the diagram below.

The VIDEO DET and APC DET employ a double balanced mixer.

Detector output (pin ㉘) is $1.5V_{P\text{-}P}$ (Vcc = 9V, negative sync).

Detector output is almost proportional to supply voltage.

Pin ㉘ is an emitter follower, containing a 2KΩ emitter resistor, and requires an externally attached resistor (2KΩ~1KΩ) as it is insufficient alone to drive a 4.5MHz trap.



The lock detector determines locked/unlocked conditions by the average level of detector output.

In pin ㉘, the threshold is 3.2V.

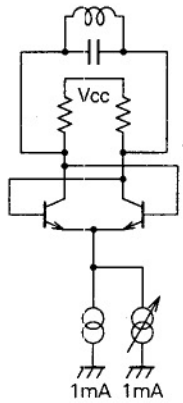
The time constant switch is pin ㉙.

The VCO circuit diagram is shown to the right, and illustrates how sinking current is varied to adjust frequency.

The variable range falls between −1.7MHz and +1.3MHz at a capacity of 27PF (45.75MHz).

The variable range widens as the capacity decreases, while the temperature drift characteristic and harmonics worsen.

Vcc and GND of the VCO section are independent of those of the VIF, while the same DC voltage must be supplied as for the VIF.



3. SIF Det.

4.5MHz issues from pin ㉘, however, for M51362SP, inputting 41.25MHz thru pin ⑪ causes 4.5MHz to be output from pin ⑮, the product of multiplying 45.75MHz by the carrier wave gained at the VCO.

Since conversion gain is 18dB, which is constant, note that at a lower level than the delay point, the output level is also lowered linearly.

Input impedance is approx. 2KΩ, output pin ⑮ is an emitter follower type circuit, current sink is 0.6mA, and a 300Ω resistor is connected in series.

4. AFT

The AFT circuit is of the conventional type. Output is also of the conventional current-drive type.

Since internal operating current is reduced, use a load resistor three times larger than the conventional one. A defeat terminal is not provided here.

Therefore, using the middle point in the coil between pins ㉘ and ㉗, lower the voltage of pins ㉖ and ㉗ to less than 1V. The internal resistor of pins ㉖ and ㉗ is 6KΩ.

5. IF/RF AGC

IF AGC input is applied from pin ㉘ Video Out. → 4.5MHz trap → pin ㉚ to PNP emitter follower.

The IF AGC amplifier is a two-stage amplifier, with pin ⑥ & pin ⑦ serving as a filter terminal.

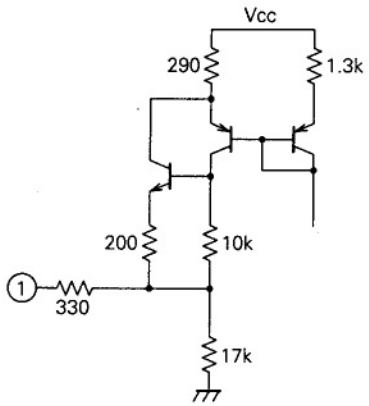
Output to pin ⑥ is a current-drive type, and a current sink is 0.5mA.

The RF AGC is a reverse output type; its pin ① output is illustrated in the figure to the right.

Output voltage is (7.8V~0V) at Vcc = 9V.

Black spot inverter works before EQ amp. Voltage lower than sync chip by 0.45V (pin ㉘) is to be threshold.

Clamp voltage is nearly at the white level.

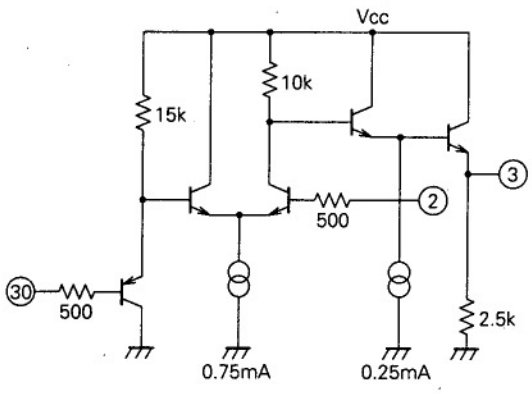


6. EQ Amplifier

Basically, the EQ amplifier is as shown in the diagram to the right.

Providing the feedback to pin ②, it has the frequency characteristic.

It can also be used as an amplifier with a fixed gain.



7. SIF Section

As Vcc and GND of the SIF section are independent of those of the VIF, the supply voltage of the SIF section can be changed.

The limiter amplifier is a triple amplification device, including an internal differential amplifier. Pin ⑭ is a DC feedback terminal.

The resistor between pins ⑬ and ⑭ is provided to prevent parasitic oscillation.

The FM detector employs a quadrature detection method and requires a tank coil and damping resistor at pins ⑰ and ⑱.

Note that use of a ceramic discriminator would not obtain a good characteristic.

Pin ⑲ audio output also employs an emitter follower and the output impedance is approx. 700Ω.

Principle of M51362SP PLL Section

M51362SP's PLL section is formed as shown in Fig. 1. The locked loop is indicated by broken lines.

The APC and video detector are double balance-type multipliers, and the LPF is a lag-lead filter with external C.R.

The APC detector is a phase comparator and outputs voltage corresponding to the phase difference between the IF signal and VCO output (output through +45° phase shift device).

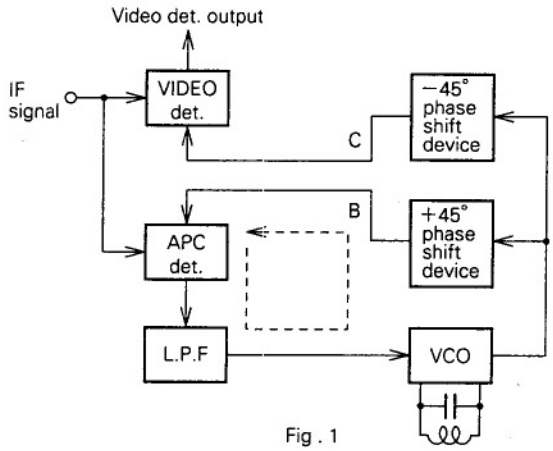


Fig . 1

The phase comparator usually has such a characteristic as the one illustrated in Fig. 2: When the phase angle of B is +90° out-of-phase for the IF signal, the APC output current becomes 0, while APC output current becomes positive when the phase angle lags.

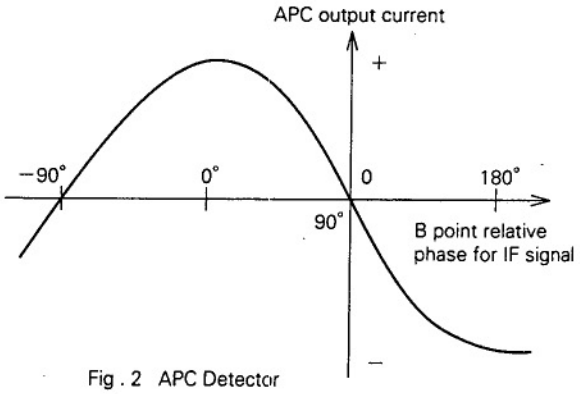


Fig . 2 APC Detector

Output current is converted into voltage, and unnecessary frequency is cut off via LPF. Then, the voltage is applied to VCO as controlled voltage. Here, the VCO characteristic is shown in Fig. 3, and for the IF signal, the phase at B relative to the IF signal is −90°.

The procedure by which the VCO follows the IF signal is described below: For example, when the phase of the IF signal lags (the phase at B relative to the IF signal leads more than −90°), APC output current becomes positive, controlled current increases, frequency tends to decrease and, consequently, the phase lags.

So at point B, the VCO locked in phase angle is −90°. Meanwhile, when the frequency of the IF signal becomes high, APC output is negative, controlled voltage decreases, and the VCO frequency becomes higher, because the instantaneous phase is equivalent to leading.

However, with phase error inversely proportional to loop gain, the VCO locks.

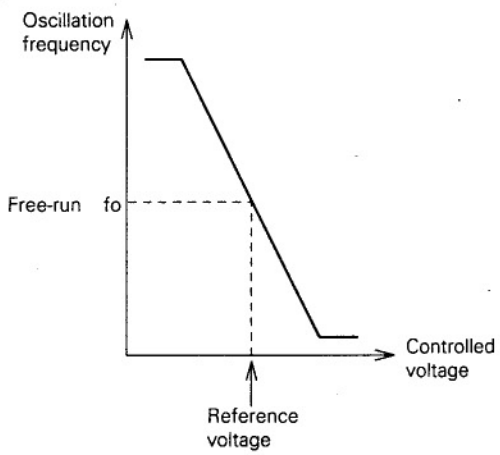


Fig . 3 VCO Characteristic

Free-run frequency is oscillation frequency produced when center voltage is applied to the VCO.

When locked, the input frequency lock range depends on the variable frequency range, and the lower loop gain narrows this range. Description of the capture procedure for the IF signal is omitted here due to its complexity. The capture range is narrower than that of the lock in relation to loop gain, and narrower than the LPF bandwidth.

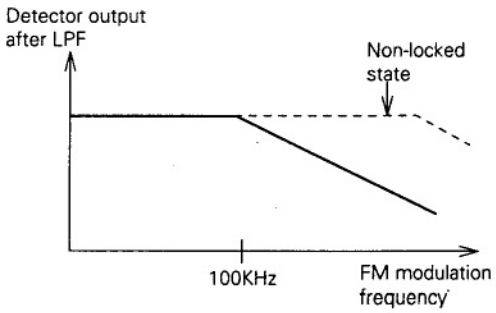


Fig . 4

When the M51362SP is in the non-locked state and a locked condition is detected, the LPF time constant is reduced to widen the capture range.

The frequency response characteristic under the locked state is shown in Fig. 4; cut-off frequency is approx. 100KHz, and is equivalent to the bandwidth of the carrier wave reproduced from the IF signal.

Here, the AM detector section is now described. If, in Fig. 5, the phase at point B is locked at −90°, phase lags by 45° at point A, this means the IF signal carrier wave will be −135°.

Consequently, the carrier wave phase at point C, where the signal is input into the video detector, lags by an additional 45°, producing −180° (out-of-phase).

A correct phase produces the most complete and effective demodulation of the video signal. (See Fig. 5).

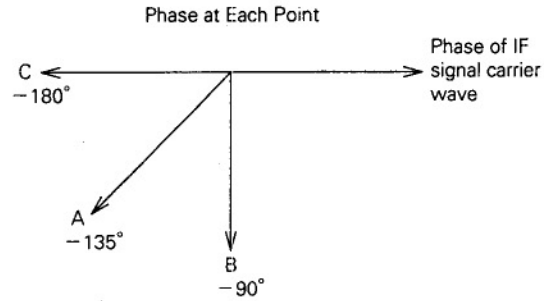


Fig . 5

Fig.6 illustrates the basic circuit of the phase shift device. Each phase shift device comprises an LPF (−45°), an HPF (+45°) having simple C and R and set so that the phase will rotate by ±45° at 45.75MHz.

Consequently, although the phase rotation varies in the other IF band, the relative phase angle is 90°, independent of frequency, as the values of R and C are set equal to one another.

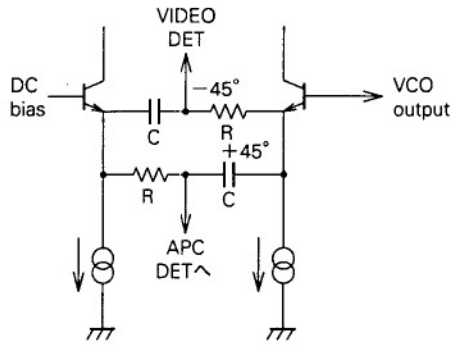


Fig . 6

SPECIAL PARTS

Coil Specification

f = 45.75MHz

1) VCO coil pin ㉒, ㉓

Qu	Co(pF)	Turns	Bobbin	Wire
92±20%	27 Stray 7.2	(1–6) $6\frac{1}{2}$t	10K type	0.12Φ OUEW

Variable range widens as Co is reduced.

2) AFT coil pin ㉖, ㉗

Qu	Co(pF)	Turns	Bobbin	Wire
84±20%	59±6%	(1–6) $4\frac{1}{4}$t	10K type	0.12Φ OUEW

3) SIF coil pin ⑪

Filter passing only 41.25MHz. Can be used in AFT coil. When SAW filter (41.25MHz) is used, compensation for loss is necessary.

4) SIF FM det. coil pin ⑰, ⑱

Qu	Co(pF)	Turns	Bobbin	Wire
60±20%	68pF	(4–6) 36t	10K type	0.12Φ OUEW