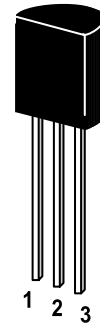


ST 2SB1116 / 2SB1116A

PNP Silicon Epitaxial Planar Transistor

Audio frequency power amplifier and medium speed switching.

The transistor is subdivided into three groups, Y, G and L, according to its DC current gain.



1. Emitter 2. Collector 3. Base

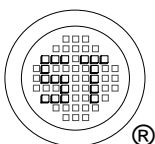
TO-92 Plastic Package
Weight approx. 0.19g

Absolute Maximum Ratings ($T_a = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Collector Base Voltage 2SB1116 2SB1116A	$-V_{CBO}$	60 80	V
Collector Emitter Voltage 2SB1116 2SB1116A	$-V_{CEO}$	50 60	V
Emitter Base Voltage	$-V_{EBO}$	6	V
Collector Current	$-I_C$	1	A
Collector Current (Pulse)	$-I_{CP}$	2	A
Power Dissipation	P_{tot}	0.75	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature Range	T_s	- 55 to + 150	$^\circ\text{C}$

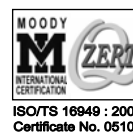
Characteristics at $T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Min.	Max.	Unit	
DC Current Gain at $-V_{CE} = 2\text{ V}$, $-I_C = 0.1\text{ A}$ at $-V_{CE} = 2\text{ V}$, $-I_C = 1\text{ A}$	Y G L	h_{FE} h_{FE} h_{FE}	135 200 300	- - -	
		h_{FE}	81	-	
	Collector Cutoff Current at $-V_{CB} = 60\text{ V}$	$-I_{CBO}$	-	100	nA
	Emitter Cutoff Current at $-V_{EB} = 6\text{ V}$	$-I_{EBO}$	-	100	nA
Collector Emitter Saturation Voltage at $-I_C = 1\text{ A}$, $-I_B = 50\text{ mA}$	$-V_{CE(sat)}$	-	0.4	V	
Base Emitter Saturation Voltage at $-I_C = 1\text{ A}$, $-I_B = 50\text{ mA}$	$-V_{BE(sat)}$	-	1.2	V	
Base Emitter On Voltage at $-V_{CE} = 2\text{ V}$, $-I_C = 50\text{ mA}$	$-V_{BE(on)}$	0.6	0.7	V	
Gain Bandwidth Product at $-V_{CE} = 2\text{ V}$, $-I_C = 100\text{ mA}$	f_T	70	-	MHz	



SEMTECH ELECTRONICS LTD.

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ISO/TS 16949 : 2002
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ISO 14001:2004
Certificate No. 71116

ISO 9001:2000
Certificate No. 0506098

Dated : 10/11/2006

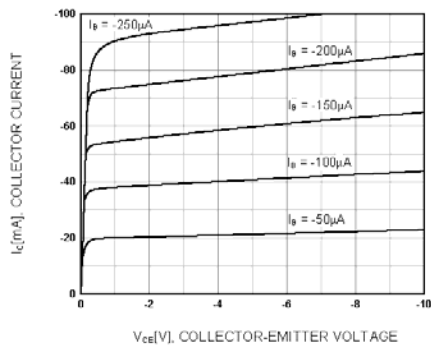


Figure 1. Static Characteristic

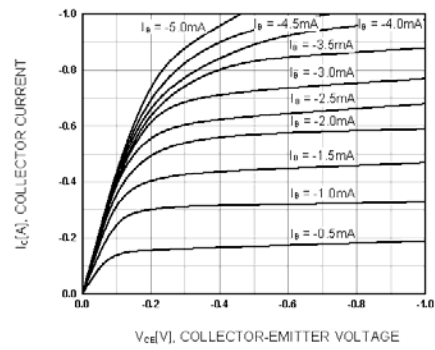


Figure 2. Static Characteristic

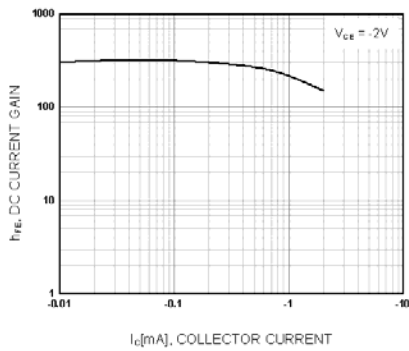


Figure 3. DC current Gain

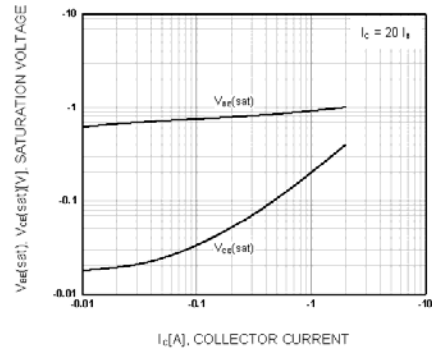


Figure 4. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

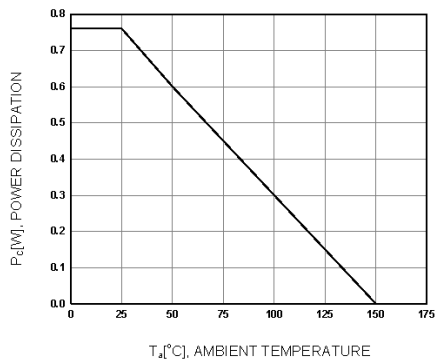
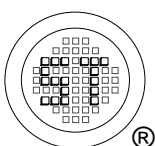
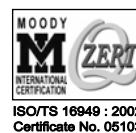


Figure 5. Power Derating



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