



January 2006



- Pletronics' SQ33D Series is a quartz crystal controlled precision square wave generator with a CMOS output.
- The SQ33D series will directly interface TTL devices also.
- Greatly reduces RFI and EMI system sensitivity
- Minimizes RFI radiation, eases meeting FCC Class B emissions standards.
- · Capable of driving up to 30pF capacitive loads
- Tube packaging is available.

- 70 to 107 MHz
- · Half Size Thru-Hole DIP package
- Enable/Disable Function
- Disable function includes low standby power mode
- 3rd Overtone Crystals used
- Improved circuit to minimize oscillator issues such as multi-mode output signal.
- Low Jitter
- · Has internal bypass capacitor on the Vcc lead
- 5x7 mm LCC ceramic oscillator inside

Pletronics Inc. certifies this device is in accordance with the RoHS (2002/95/EC) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's

Weight of the Device: 2.0 grams

Moisture Sensitivity Level: 1 As defined in J-STD-020C

Second Level Interconnect code: e1 or e2

Absolute Maximum Ratings:

Parameter	Unit
V _{cc} Supply Voltage	-0.5V to +7.0V
Vi Input Voltage	-0.5V to V _{CC} + 0.5V
Vo Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics

The maximum die or junction temperature is 155°C

The thermal resistance junction to board is 110°C/Watt depending on the solder pads, ground plane and construction of the PCB.



January 2006

Part Number:

SQ33	45	D	ES	-100.0M	-30	-XX		Marking
							Internal code or blank	
							Output Load Capacitance Blank = 15pF maximum 30 = 30pF maximum	none
							Frequency in MHz	fff.fff M
							Supply Voltage V _{cc} Blank = 5.0V ± 10%	none
							Enhanced Specifications (apply in the order shown) E = Temperature range -40 to 85°C S = Symmetry 45%/55% at 50% of V _{CC}	E S
							Series Model	
							Frequency Stability 45 = ± 50 ppm 44 = ± 25 ppm 20 = ± 20 ppm	5 4 2
							Series Model	SQ3

Part Marking:

PLEWhere: x= Frequency stabilitySQ3xssss= Enhanced specificationfff.fff Mfff.fff= Frequency in MHzyywwaLFyywwa= Date codeLF= Lead Free

.F = Lead Free (Voltage not shown)

Pletronics may ship the following combinations without notice (this is an enhanced specified device)

44 (25 ppm) stability parts when 45 (50 ppm) was ordered

20 (20 ppm) stability parts when 45 (50 ppm) or 44 (25 ppm) was ordered.

E temperature range parts when extended was not ordered.

S symmetry parts when 40/60% symmetry was ordered.

Pletronics may ship parts that are not marked for extended temperature range but were tested for extended temperature range, a Certificate of Conformance will accompany these parts.



January 2006

Electrical Specification for $5.00V \pm 10\%$ over the specified temperature range

Item	Min	Max	Unit	Condition
Frequency Range	70	107	MHz	
Frequency Accuracy "45"	-50	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures
"44"	-25	+25		
" 20 "	-20	+20		
Output Waveform	CMOS			
Output High Level	0.5	-	V	Below V _{CC} (See load circuit)
Output Low Level	1	0.4	V	(See load circuit)
Output Symmetry	40	60	%	at 50% point of V_{CC} (See load circuit) Standard
	45	55	%	for "S" option parts
Jitter	-	1	pS RMS	12 KHz to 20 MHz from the output frequency
	-	4	pS RMS	10 Hz to 1 MHz from the output frequency
Enable/Disable Internal Pull-up	50	-	Kohm	to V _{CC}
V disable	-	0.5	V	Applied to pad 1
V enable	2.0	-	V	Applied to pad 1
Output leakage V _{OUT} = V _{CC}	-10	+10	uA	Pad 1 low, device disabled
V _{OUT} = 0V	-10	+10	uA	
Enable time	-	100	nS	Time for output to reach a logic state
Disable time	-	100	nS	Time for output to reach a high Z state
Start up time	-	10	mS	Time for output to reach specified frequency
Operating Temperature Range	0	+70	°C	Standard Temperature Range
	-40	+85	°C	Extended Temperature Range "E" Option
Storage Temperature Range	-55	+125	°C	



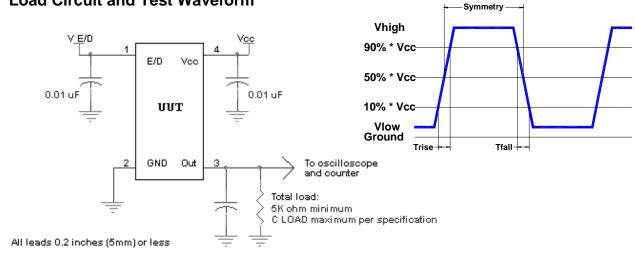
January 2006

Electrical Specification for 5.00V ±10% over the specified temperature range

Item	Min	Тур	Max	Unit	Condition	
V _{OUT} High (V _{OH})	0.5	0.3	-	V	Below V _{CC} , I _{OH} = +16 mA	4
V _{OUT} Low (V _{OL})	-	0.3	0.4	V	I _{OL} = -16 mA	
Output T_{RISE} and T_{FALL}	-	2.0	4.0	nS	C _{LOAD} = 15 pF,	
	-	3.0	6.0	nS	C _{LOAD} =30 pF,	
V _{CC} Supply Current	-	50	90	mA	>100 MHz	C _{LOAD} = 15 pF
(I _{cc})	-	45	80	mA	<=100 MHz	10% to 90% of V _{cc} (See load circuit)
	-	60	100	mA	>100 MHz	C _{LOAD} = 30 pF
	-	50	100	mA	<=100 MHz	10% to 90% of V _{CC} (See load circuit)

Specifications with Pad 1 E/D open circuit

Load Circuit and Test Waveform





January 2006

Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition A
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm) Font is Courier New Bar code is 39-Full ASCII



Label is 1" x 2.6" (25.4mm x 66.7mm) Font is Arial

Pb Free

2nd LvL Interconnect Catagory=e1

Max Safe Temp=280C for 15s (Wave solder only)
Max Safe Temp=245C for 10s (Reflow only)

Pb Free

2nd LvL Interconnect Catagory=e2

Max Safe Temp=280C for 15s (Wave solder only)
Max Safe Temp=245C for 10s (Reflow only)

PCB Mounting (typical for lead free processing)

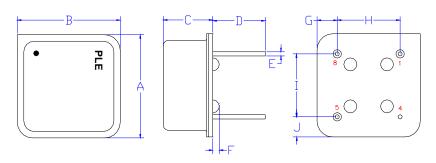
Hand soldering is recommended.

Wave solder at 255°C to 280°C with maximum wave exposure of 15 seconds Reflow solder maximum exposure of 245°C for 15 seconds Soldering done in a nitrogen atmosphere enhances the solder joint quality.



January 2006

Mechanical:



Cover:

Kovar

Electroless Nickel Plated 1 µinch (25 µm) typical

Resistance welded to base

Label:

White Kapton with Black Letters

Blue Epoxy heat cure ink with laser marked lettering

Base: Kovar

Glass to metal sealed leads

Pin 4 Connected to case

Not to scale

Inches	mm
0.487 <u>+</u> 0.005	12.37 <u>+</u> 0.13
0.487 <u>+</u> 0.005	12.37 <u>+</u> 0.13
0.225 <u>+</u> 0.011	5.72 <u>+</u> 0.28
0.250	6.35
0.020	0.51
0.031	0.79
0.094	2.37
0.300	7.62
0.200	7.62
0.094	2.37
	0.487 ±0.005 0.487 ±0.005 0.225 ±0.011 0.250 0.020 0.031 0.094 0.300 0.200

¹ Nominal dimension

Pad	Function	Note
1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. When this pad is logic low the output will be inhibited (high impedance state.) Recommend connecting this pad to $V_{\rm CC}$ if the oscillator is to be always on.
4	Ground (GND)	
5	Output	
8	Supply Voltage (V _{cc})	Recommend connecting appropriate power supply bypass capacitors as close as possible.

Layout and application information

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.





January 2006

IMPORTANT NOTICE

Pletronics Incorporated (PLE) reserves the right to make corrections, improvements, modifications and other changes to this product at anytime. PLE reserves the right to discontinue any product or service without notice. Customers are responsible for obtaining the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to PLE's terms and conditions of sale supplied at the time of order acknowledgment.

PLE warrants performance of this product to the specifications applicable at the time of sale in accordance with PLE's standard warranty. Testing and other quality control techniques are used to the extent PLE deems necessary to support this warranty. Except where mandated by specific contractual documents, testing of all parameters of each product is not necessarily performed.

PLE assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using PLE components. To minimize the risks associated with the customer products and applications, customers should provide adequate design and operating safeguards.

PLE does not warrant or represent that any license, either express or implied, is granted under any PLE patent right, copyright, artwork or other intellectual property right relating to any combination, machine or process which PLE product or services are used. Information published by PLE regarding third-party products or services does not constitute a license from PLE to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from PLE under the patents or other intellectual property of PLE.

Reproduction of information in PLE data sheets or web site is permissible only if the reproduction is without alteration and is accompanied by associated warranties, conditions, limitations and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. PLE is not responsible or liable for such altered documents.

Resale of PLE products or services with statements different from or beyond the parameters stated by PLE for that product or service voids all express and implied warranties for the associated PLE product or service and is an unfair or deceptive business practice. PLE is not responsible for any such statements.

Contacting Pletronics Inc.

Pletronics Inc. 19013 36th Ave. W, Suite H Lynnwood, Washington 98036-5761 USA Tel: 425-776-1880 Fax: 425-776-2760 E-mail: ple-sales@pletronics.com

=-mail: <u>pie-sales@pletronics.com</u> URL: <u>www.pletronics.com</u>

Copyright © 2005, Pletronics Inc.