GENERAL DESCRIPTION

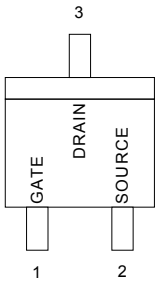
This N-Channel enhancement mode field effect transistor is produced using high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. It can be used in most applications requiring up to 115mA DC and can deliver pulsed currents up to 800mA. This product is particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

FEATURES

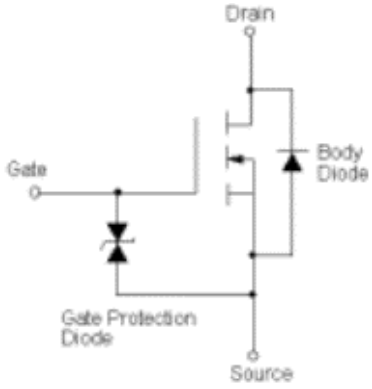
- High Density Cell Design for Low $R_{DS(ON)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable
- High Saturation Current Capability
- Built-in G-S Protection Diode

PIN CONFIGURATION

SOT-23
Top View



SYMBOL



N-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT2N7002AG	SOT-23

***Note:** G : Suffix for Pb Free Product

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage (R_{GS} = 1.0MΩ)	V_{DGR}	60	V
Drain to Current — Continuous — Pulsed	I_D I_{DM}	±115 ±800	mA
Gate-to-Source Voltage	V_{GS}	±20	V
Total Power Dissipation Derate above 25℃	P_D	225 1.8	mW mW/℃
Single Pulse Drain-to-Source Avalanche Energy — T_J = 25℃ (V_{DD} = 50V, V_{GS} = 10V, I_{AS} = 0.5A, L = 20mH, R_G = 25Ω)	E_{AS}	2.5	mJ
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃
Thermal Resistance — Junction to Ambient	θ_{JA}	417	℃/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	300	℃

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, T_J = 25℃.)

			CMT2N7002AG			
Characteristic		**Symbol**	**Min**	**Typ**	**Max**	**Units**
Drain-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 10 μA)		$V_{(BR)DSS}$	60			V
Drain-Source Leakage Current (V_{DS} = 60 V, V_{GS} = 0 V) (V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125℃)		I_{DSS}			 1.0 0.5	 μA mA
Gate-Source Leakage Current-Forward (V_{gsf} = 20 V)		I_{GSS}			10	uA
Gate-Source Leakage Current-Reverse (V_{gsf} = -20 V)		I_{GSS}			-10	uA
Gate Threshold Voltage * (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	1.0		2.5	V
On-State Drain Current (V_{DS} ≧ 2.0 $V_{DS(on)}$, V_{GS} = 10V)		$I_{d(on)}$	500			mA
Static Drain-Source On-Resistance * (V_{GS} = 10 V, I_D = 0.5A) (V_{GS} = 10 V, I_D = 0.5A, T_C = 125℃) (V_{GS} = 5.0 V, I_D = 50mA) (V_{GS} = 5.0 V, I_D = 50mA, T_C = 125℃)		$R_{DS(on)}$			 7.5 13.5 7.5 13.5	Ω
Drain-Source On-Voltage * (V_{GS} = 10 V, I_D = 0.5A) (V_{GS} = 5.0 V, I_D = 50mA)		$V_{DS(on)}$			 3.75 0.375	V
Forward Transconductance (V_{DS} ≧ 2.0 $V_{DS(on)}$, I_D = 200mA) *		g_{FS}	80			mmhos
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}			50	pF
Output Capacitance		C_{oss}			25	pF
Reverse Transfer Capacitance		C_{rss}			5.0	pF
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 500 mA, V_{gen} = 10 V, R_G = 25Ω, R_L = 50Ω) *	$t_{d(on)}$			20	ns
Turn-Off Delay Time		$t_{d(off)}$			40	ns
Diode Forward On-Voltage (IS = 115 mA, VGS = 0V)		V_{SD}			-1.5	V
Source Current Continuous (Body Diode)		I_S			-115	mA
Source Current Pulsed		I_{SM}			-800	mA

* Pulse Test: Pulse Width ≦300μs, Duty Cycle ≦2%

TYPICAL ELECTRICAL CHARACTERISTICS

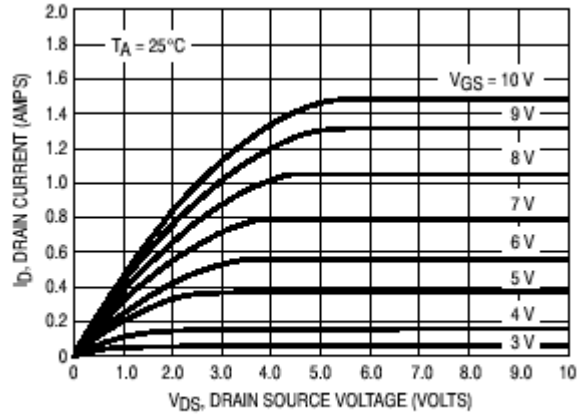


Figure 1. Ohmic Region

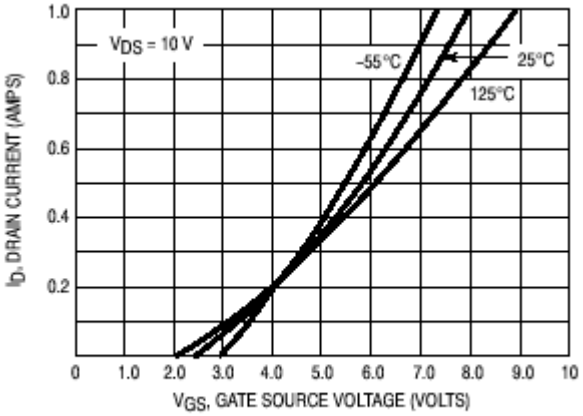


Figure 2. Transfer Characteristics

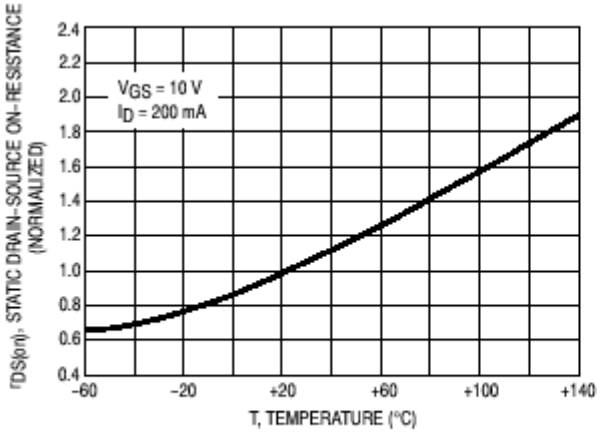


Figure 3. Temperature versus Static Drain–Source On–Resistance

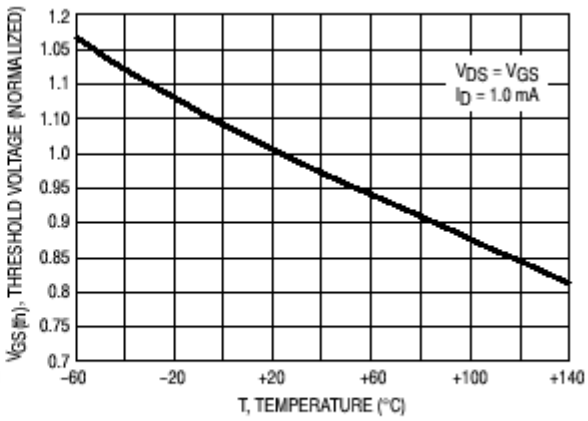


Figure 4. Temperature versus Gate Threshold Voltage

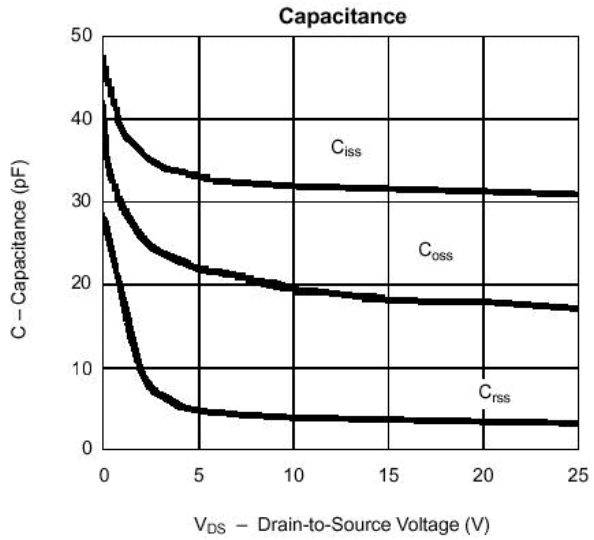
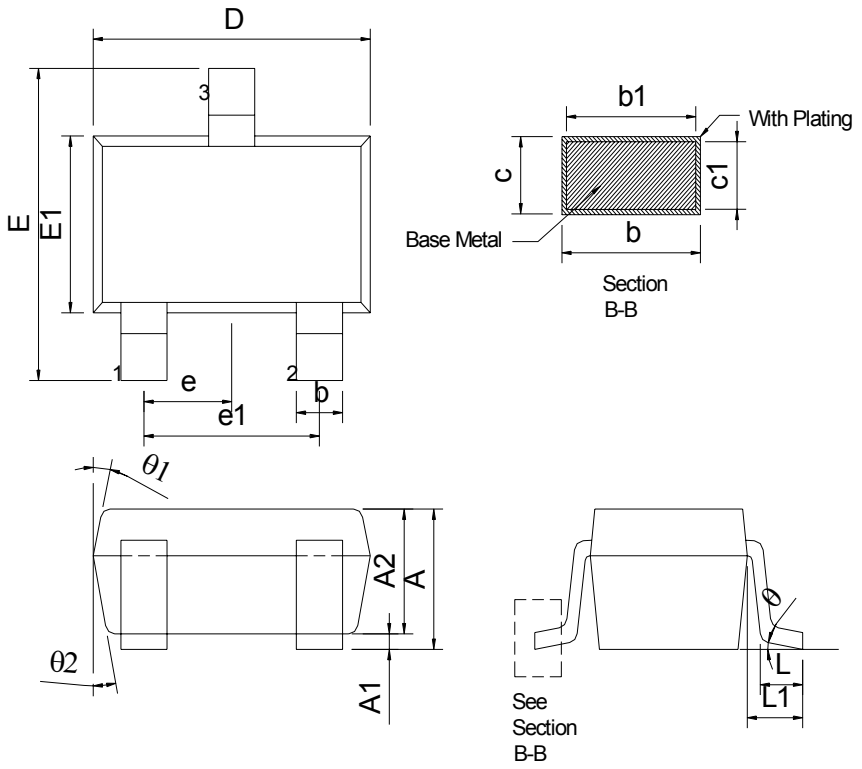


Figure 5. Capacitance

PACKAGE DIMENSION

SOT-23



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	---	1.35	0.041	---	0.053
A1	0.05	---	0.15	0.002	---	0.006
A2	1.00	1.10	1.20	0.039	0.043	0.047
b	0.25	---	0.50	0.010	---	0.020
b1	0.25	0.40	0.45	0.010	0.016	0.018
c	0.08	---	0.20	0.003	---	0.008
c1	0.08	0.11	0.15	0.003	0.004	0.006
D	2.70	2.90	3.00	0.106	0.114	0.118
E	2.20	2.40	2.60	0.087	0.094	0.102
E1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.35	0.45	0.55	0.014	0.018	0.022
L1	0.60 REF			0.024 REF		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
θ	0°	5°	10°	0°	5°	10°
θ1	3°	5°	7°	3°	5°	7°
θ2	6°	8°	10°	6°	8°	10°

IMPORTANT NOTICE

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