

Description

The Intersil ICL7116 are high performance, low power, 3 1₂ digit, A/D converters. Incl uded are seven segment decoders, display drivers, a reference, and a clock. The ICL7116 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive. The ICL7116 have all of the featur es of the ICL7106 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and retain the value on the display indefinitely. To make room for this feature the reference low input has been connected to Common internally rather than being fully differential.

These circuits retain the accuracy, versatility, and true economy of the ICL7106. They feature

auto-zero to less than 10μ V, zero drift of less than 1μ V/ $^{\circ}$ C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (ICL7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display.

Features

- HOLD Reading Input Allows Indefinite Display Hold
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- Direct Display Drive
 - LCD ICL7116
- Low Noise Less Than 15µV P-P (Typ)
- On Chip Clock and Reference
- Low Power Dissipation Typically Less Than 10mW
- No Additional Active Circuits Required
- Surface Mount Package Available

Operating Conditions



Electrical Characteristics

 $T_A = 25^{0}C$, $f_{CLOCK} = 48kHz$, $V_{REF} = 100mV$

PARAMETER	TEST COND		MIN.	TYP.	MAX.	
UNITS						
Zero Input Reading	V _{IN} = 0V, Full Scale = 200mV	-000.0	±000.0	+000.0	Digital	
Ratiometric Reading	VIN = VREE. VREE = 100mV	999	999/1000	1000	Digital	
Rollover Error	-V _{IN} = +V _{IN} ≅ 195mV Difference in Reading for Egual Positive and Negative Inputs Near Full Scale	-	±0.2	±1	Counts	
Linearity	Full Scale = 200mV or Full Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 5)	-	±0.2	±1	Counts	
Common Mode Rejection Ratio	$V_{CM} = \pm 1 V$, $V_{IN} = 0 V$, Full Scale = 200mV (Note 5)	-		50 -	μV/V	
Noise	V _{IN} = 0V, Full Scale = 200 mV (Peak-To-Peak Value Not Exceeded 95% of Time) (Note 5)	-		15 -	μV	
Leakage Current Input	V _{IN} = 0 (Note 5)	-	1	10	рА	
Zero Reading Drift	$V_{IN} = 0,0^{\circ}C$ To $70^{\circ}C$ (Note 5)	-	0.2	1	µV/⁰C	
Scale Factor Temperature	$V_{IN} = 199 \text{mV}, 0^{\circ} \text{C} \text{ To } 70^{\circ} \text{C} \text{ (Note 5)}$	-	1	5	ppm/ ⁰ C	
V + Supply Current	$V_{IN} = 0$	-	1.0	1.8	mA	
COMMON Pin Analog Common Voltage	$25k\Omega$ Between Common and Positive Supply (With Respect to + Supply)	2.4	:	3.0 3.2	V	
Temperature Coefficient of Analog Common	$25k\Omega$ Between Common and Positive Supply (With Respect to + Supply) (Note 5)	-		80 -	ppm/ ⁰ C	
DISPLAY DRIVER (ICL7116						
ONLY) Peak-To-Peak Segment Drive Voltage Peak-To-Peak Backplane	V + = to V - = 9V, (Note 4)	4	5.5	6	V	

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to $\pm 100 \mu$ A.

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

3. Unless otherwise noted, specifications apply to both the ICL7116. ICL7116 is tested in the circuit of Figure 1.

4. Back plane drive is in phase with segment drive for 'off' segment, 180 degrees out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

5. Not tested, guaranteed by design.



Absolute Maximum Ratings

Thermal Information

Maximum Junction Temperature	150 °C
Maximum Storage Temperature Range	65 ⁰ C to 150 ⁰
C Maximum Lead Temperature (Soldering 10s)	
O ⁰	
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Typical Applications Circuit



FIGURE 1. ICL7116 TEST CIRCUIT AND TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

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DESIGN INFORMATION SUMMARY SHEET

VINT MAXIMUM SWING: OSCILLATOR FREQUENCY fosc = 0.45/RC (V- + 1.0V) < V_{INT} < (V+ - 0.5V), V_{INT} (Typ) = 2 V DISPLAY COUNT Cosc > 50pF; Rosc > 50kΩ fosc (Typ) = 48kHz VIN $COUNT = 1000 \times \frac{11}{V_{REF}}$ OSCILLATOR PERIOD tosc = RC/0.45 INTEGRATION CLOCK FREQUENCY CONVERSION CYCLE f_{CLOCK} = f_{OSC}/4 t_{сус} = t_{сьоск} х 4000 INTEGRATION PERIOD tcyc = tosc x 16,000 t_{INT} = 1000 x (4/fosc) when fosc = 48KHz; toyc = 333ms 60/50Hz REJECTION CRITERION COMMON MODE INPUT VOLTAGE tINT/ t80Hz or tINT/t50Hz = Integer $(V - + 1V) < V_{IN} < (V + - 0.5V)$ **OPTIMUM INTEGRATION CURRENT** AUTO-ZERO CAPACITOR INT = 4uA 0.01µF < CAZ < 1µF FULL SCALE ANALOG INPUT VOLTAGE REFERENCE CAPACITOR ٠ VINFS (Typ) = 200mV or 2V $0.1\mu F < C_{REF} < 1\mu F$ INTEGRATE RESISTOR V_{сом} Biased between V+ and V-. VINFS R_{INT} V_{COM} ≅ V+ - 2.8V INT Regulation lost when V+ to V- < ≈ 6.8V. If V_{COM} is externally pulled down to (V+to V-)/2, INTEGRATE CAPACITOR the VCOM circuit will turn off. ICL7116 POWER SUPPLY: SINGLE 9V $C_{INT} = \frac{(t_{INT})(l_{INT})}{V_{INT}}$ V+ - V- = 9V Digital supply is generated internally V_{TEST} ≅ V+ - 4.5V INTEGRATOR OUTPUT VOLTAGE SWING ICL7116 DISPLAY: LCD $V_{\rm INT} = \frac{(t_{\rm INT})(l_{\rm INT})}{2}$ Type: Direct drive with digital logic supply amplitude. CINT **TYPICAL INTEGRATOR AMPLIFIER OUTPUT WAVEFORM (INT PIN)**



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