M62364FP/GP

8-bit 8ch Multiplying D/A Converter with Buffer Amplifiers

REJ03D0875-0400
Rev.4.00
Oct 02, 2009

Description

The M62364 is a CMOS 8-bit 8ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by the simple three-wiring method (DI, CLK, LD).

The output buffer amplifiers operating in AB-class has both sinking and driving capabilities of 1.0 mA or more and can operate in a whole supply range from V_{DD} to GND.

The IC is suitable for a use in automatic adjustment applications in conjunction with a MCU by utilizing the terminal D_O for a cascading connection.

Features

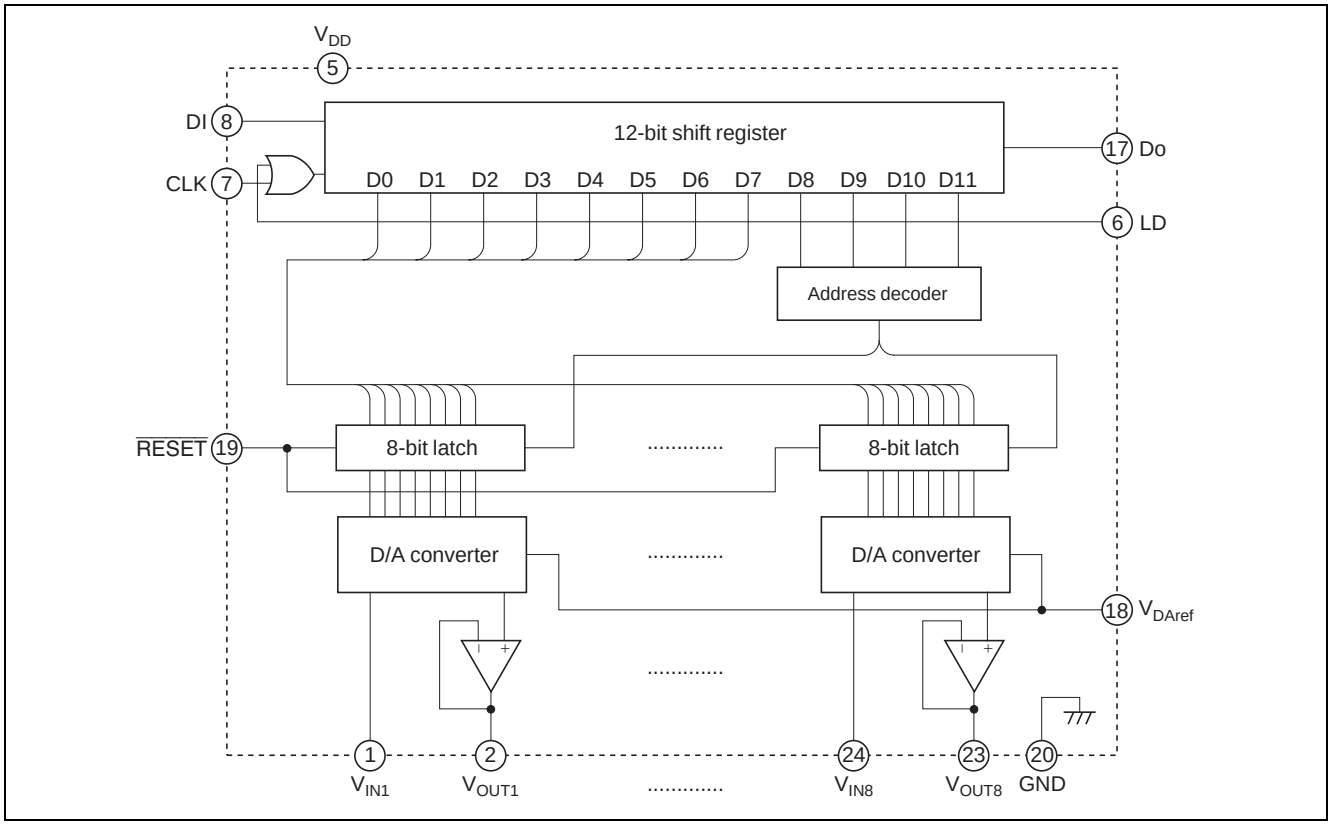
- Three-wiring serial data transmission
- Doubled precision 8ch D/A converter employing an R-2R with higher-order segment method
- 8 buffer amplifiers operating in a whole supply voltage range from V_{DD} to GND
- 4 quadrant multiplication

Application

Digital to analog conversion for consumer and industrial equipment.

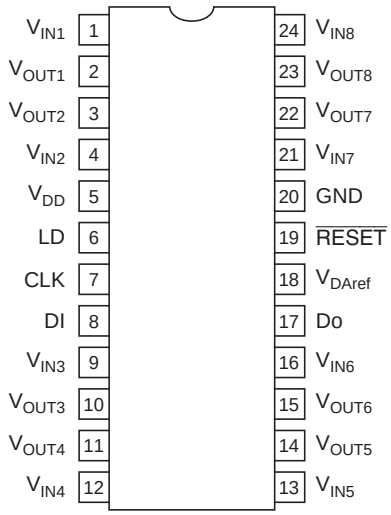
Gain setting and automatic adjustment of display-monitor and CTV.

Block Diagram



Pin Arrangement

M62364FP/GP



(Top view)

Outline: PRSP0024GA-A (24P2Q-A)
PLSP0024JA-A (24P2E-A)

Pin Description

Pin No.	Pin Name	Function
8	DI	Serial data input
17	D_O	Serial data output
7	CLK	Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge of the clock.
6	LD	A low state enables data loading to the 12-bit shift register. During a rising edge of LD, the data will be loaded to the output register.
19	$\overline{RESET}$	Reset 8-bit latches
2	V_{OUT1}	D/A converter output with 8-bit resolution
3	V_{OUT2}	
10	V_{OUT3}	
11	V_{OUT4}	
14	V_{OUT5}	
15	V_{OUT6}	
22	V_{OUT7}	
23	V_{OUT8}	
5	V_{DD}	Power supply
20	GND	Ground
1	V_{IN1}	D/A converter input
4	V_{IN2}	
9	V_{IN3}	
12	V_{IN4}	
13	V_{IN5}	
16	V_{IN6}	
21	V_{IN7}	
24	V_{IN8}	
18	V_{DAref}	D/A converter reference voltage input

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Digital input voltage	V_{IND}	–0.3 to +7.0	V
Analog input voltage	V_{IN}	–0.3 to V_{DD} + 0.3	V
Analog output voltage	V_{OUT}	–0.3 to V_{DD} + 0.3	V
D/A reference voltage	V_{DAref}	–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–40 to +125	°C

Electrical Characteristics

<Ana/Dig Common Part>

(V_{DD} = 5 V ± 10%, $V_{DD} \geq V_{IN}$, GND, V_{DAref} = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{DD}	2.7	5.0	5.5	V	
Supply current	I_{DD}	—	—	3.5	mA	CLK = 1 MHz, V_{CC} = 3 V, I_{AO} = 0 µA

<Digital Part>

(V_{DD} = 5 V ± 10%, $V_{DD} \geq V_{IN}$, GND, V_{DAref} = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input leak current	I_{ILK}	–10	—	10	µA	V_{IN} = 0 to V_{DD}
Digital input "Low" voltage	V_{IL}	—	—	0.2 V_{DD}	V	
Digital input "High" voltage	V_{IH}	0.8 V_{DD}	—	—	V	
D_O terminal output "Low" voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.5 mA
D_O terminal output "High" voltage	V_{OH}	V_{DD} – 0.4	—	—	V	I_{OH} = –400 µA

<Analog Part>

(V_{DD} = 5 V ± 10%, $V_{DD} \geq V_{IN}$, GND, V_{DAref} = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

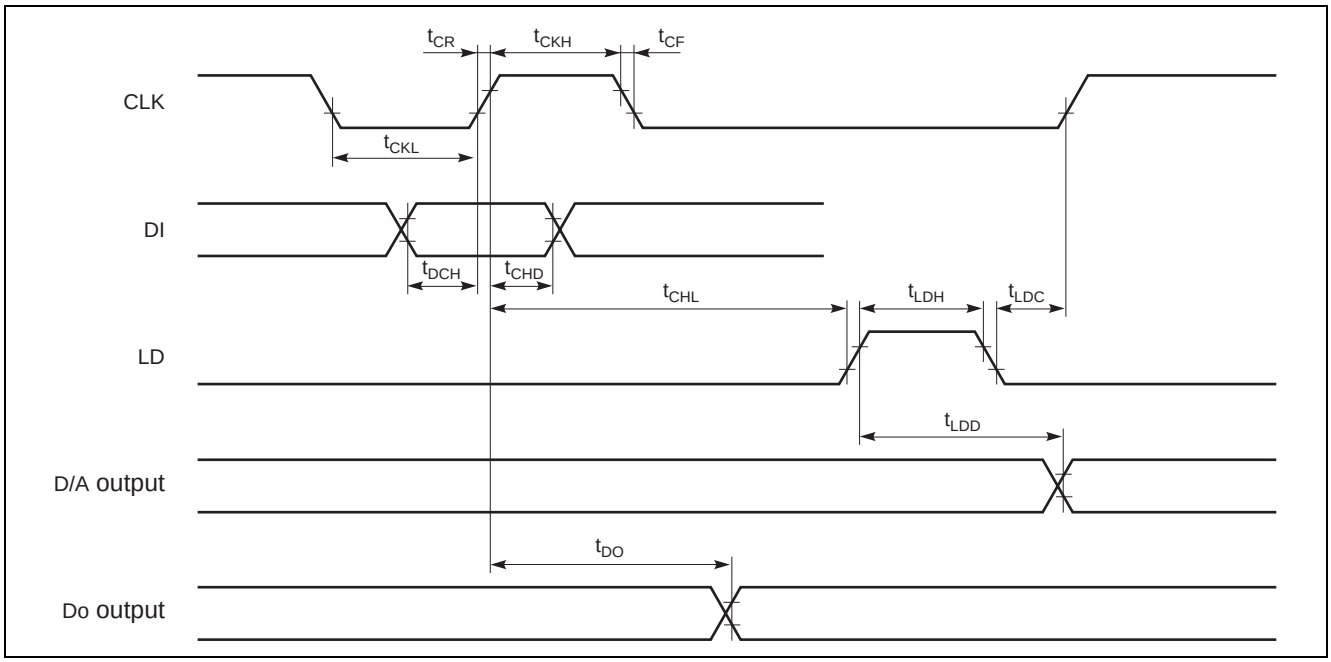
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input current	I_{IN}	—	—	0.30	mA	V_{IN} = 5 V, V_{DAref} = 0 V Proportional to Max. input current condition (V_{IN} – V_{DAref}) and digital data of each channels
D/A reference input current	I_{DAref}	–2.40	—	—	mA	V_{IN} = 5 V, V_{DAref} = 0 V Proportional to Max. input current condition (V_{IN} – V_{DAref}) and digital data of each channels
Resolution	RES	—	8	—	bit	
Differential nonlinearity	DNL	–1	—	1	LSB	V_{DAref} = 0.050 V (10 mV/LSB) Without load (I_{AO} = ±0)
Nonlinearity	NL	–1	—	1	LSB	
Buffer amplifier output voltage range	V_{AO}	0.1	—	V_{CC} – 0.1	V	I_{AO} = ±100 µA
		0.2	—	V_{CC} – 0.2		I_{AO} = ±500 µA
Buffer amplifier output current range	I_{AO}	–1	—	1	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Output capacitive load	C_O	—	—	0.1	µF	
Buffer amplifier output impedance	R_O	—	5	—	Ω	

AC Characteristics

(V_{DD} = 5 V ± 10%, $V_{DD} \geq V_{IN}$, GND, V_{DAref} = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

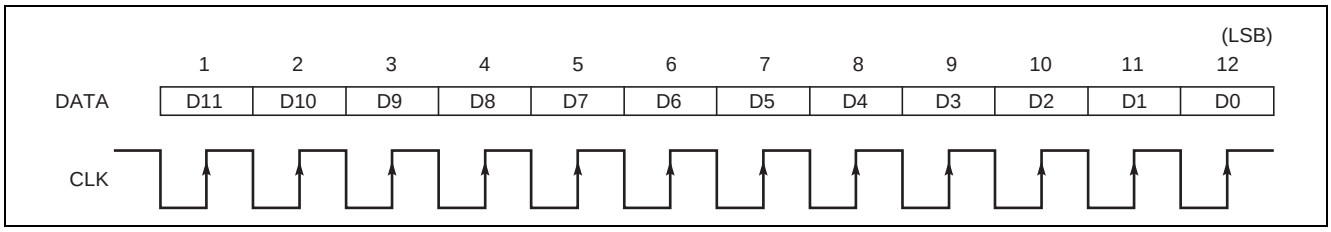
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	60	—	—	ns	
Data hold time	t_{CHD}	100	—	—	ns	
LD setup time	t_{CHL}	200	—	—	ns	
LD hold time	t_{LDC}	100	—	—	ns	
LD "H" pulse duration time	t_{LDH}	100	—	—	ns	
Data output delay time	t_{DO}	70	—	350	ns	C_L = 100 pF
D/A output setting time	t_{LDD}	—	—	300	µs	$C_L \leq$ 100 pF, V_{AO}: 0.1 ↔ 2.6 V This time until the output becomes the final value of 1/2 LSB

Timing Chart



Digital Data Format

12-bit serial data



Data Assignment

D0	D1	D2	D3	D4	D5	D6	D7	: DAC data
(LSB)							(MSB)	

D8	D9	D10	D11	: DAC select data

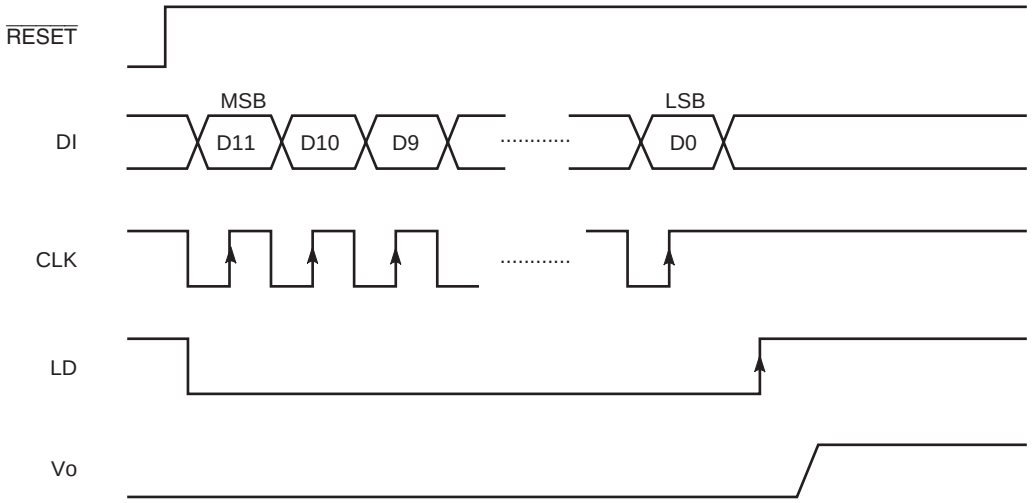
DAC Data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	V_{DAref}
1	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 1 + V_{DAref}$
0	1	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 2 + V_{DAref}$
1	1	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 3 + V_{DAref}$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	$(V_{IN} - V_{DAref}) / 256 \times 255 + V_{DAref}$

DAC Select Data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	V_{OUT1} selection
0	0	1	0	V_{OUT2} selection
0	0	1	1	V_{OUT3} selection
0	1	0	0	V_{OUT4} selection
0	1	0	1	V_{OUT5} selection
0	1	1	0	V_{OUT6} selection
0	1	1	1	V_{OUT7} selection
1	0	0	0	V_{OUT8} selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

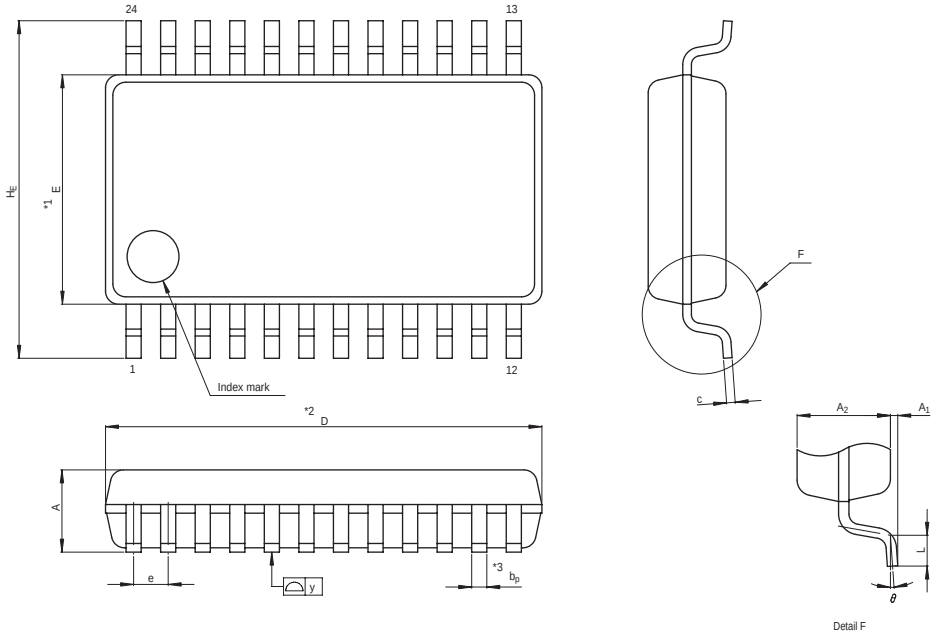
Timing Chart (Model)



Note: Input data is carried out LD signal low besides CLK signal positive edge. CLK, LD is keep generally high level.

Package Dimensions

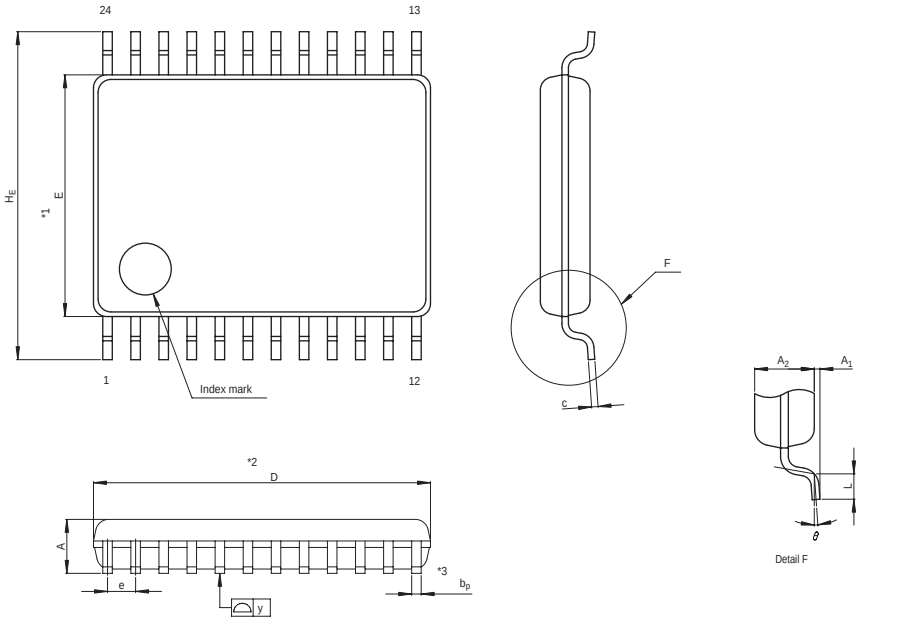
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP24-5.3x10.1-0.80	PRSP0024GA-A	24P2Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A_2	—	1.8	—
A	—	—	2.1
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	0.65	0.8	0.95
y	—	—	0.10
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP24-5.6x7.8-0.65	PLSP0024JA-A	24P2E-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.7	7.8	7.9
E	5.5	5.6	5.7
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	7.4	7.6	7.8
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

Ordering Information

Part No.	Package Name	Package Code	Taping Spec.
M62364FP#DF1J,DF1G,DF2G, TF1J,TF1G,TF2G	24P2Q-A	PRSP0024GA-A	2,000/Reel
M62364GP#DF, TF	24P2E-A	PLSP0024JA-A	2,500/Reel

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