



SPN8457

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8457 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

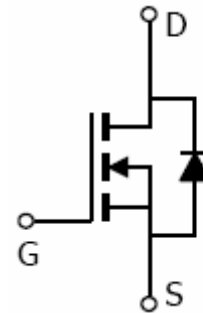
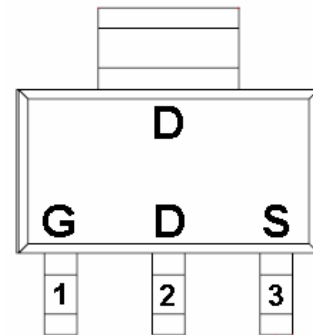
FEATURES

- ◆ 30V/5.5A, $R_{DS(ON)} = 58m\Omega @ V_{GS} = 10V$
- ◆ 30V/4.0A, $R_{DS(ON)} = 98m\Omega @ V_{GS} = 4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-223 package design

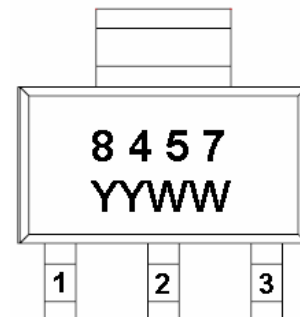
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- LCD Display inverter

PIN CONFIGURATION(SOT-223)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8457S223RG	SOT-223	8457

※ SPN8457S223RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V_{DS}	30	V	
Gate –Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	$T_A=25^{\circ}\text{C}$	5.8	A
		$T_A=70^{\circ}\text{C}$	4.2	
Pulsed Drain Current	I_{DM}	10	A	
Continuous Source Current(Diode Conduction)	I_S	1.25	A	
Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	2.8	W
		$T_A=70^{\circ}\text{C}$	1.2	
Operating Junction Temperature	T_J	150	$^{\circ}\text{C}$	
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$	
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	100	$^{\circ}\text{C}/\text{W}$	



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ELECTRICAL CHARACTERISTICS

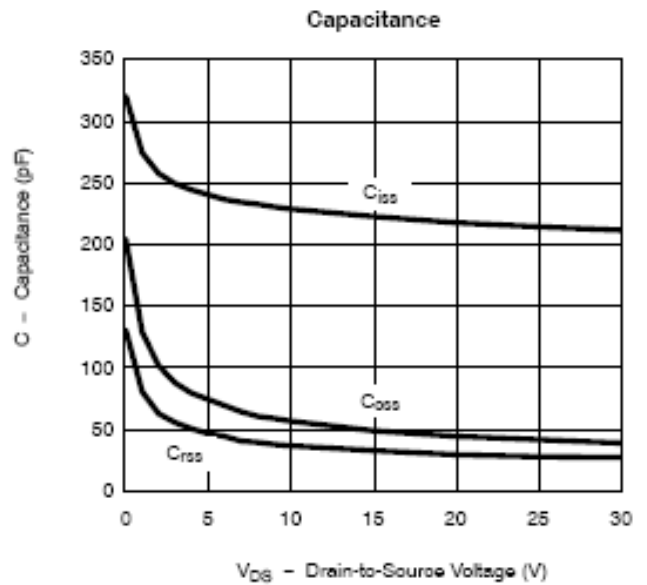
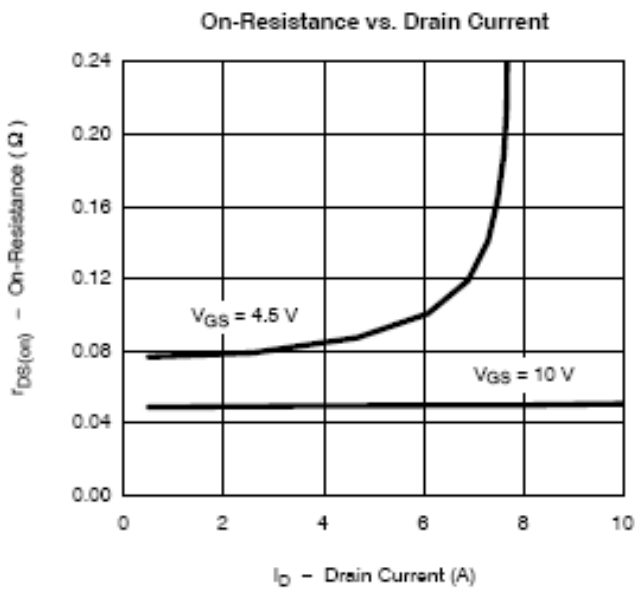
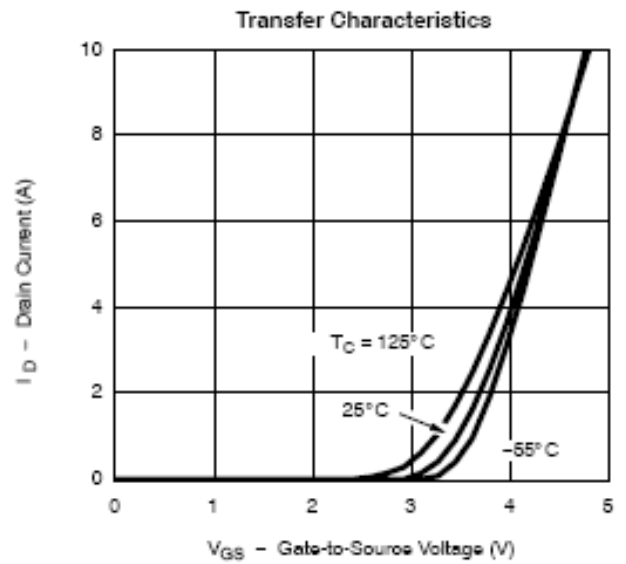
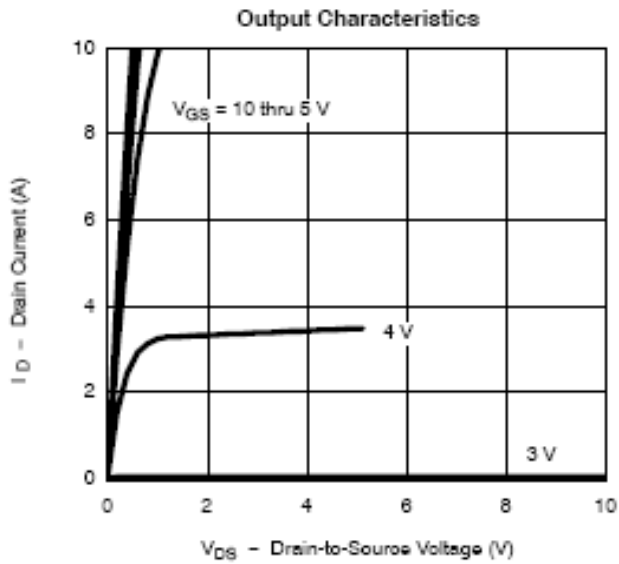
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=1.0V$			1	uA
		$V_{DS}=30V, V_{GS}=0.0V$ $T_J=55^\circ C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 4.5V, V_{GS}=10V$	6			A
		$V_{DS} \geq 4.5V, V_{GS}=4.5V$	4			
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D=5.5A$		0.050	0.058	Ω
		$V_{GS} = 4.5V, I_D=4.0A$		0.078	0.098	
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=2.5A$		4.6		S
Diode Forward Voltage	V_{SD}	$I_S=1.25A, V_{GS}=0V$		0.82	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=10V$ $I_D=2.5$		4.5	10	nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		240		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			17		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15$ $I_D=1.0A, V_{GEN}=10$ $R_G=6\Omega$		8	20	ns
	t_r			12	30	
Turn-Off Time	$t_{d(off)}$			17	35	
	t_f			8	20	



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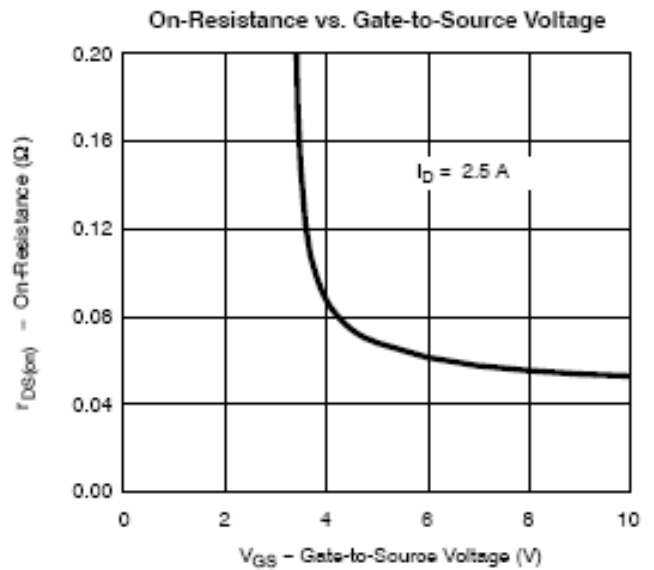
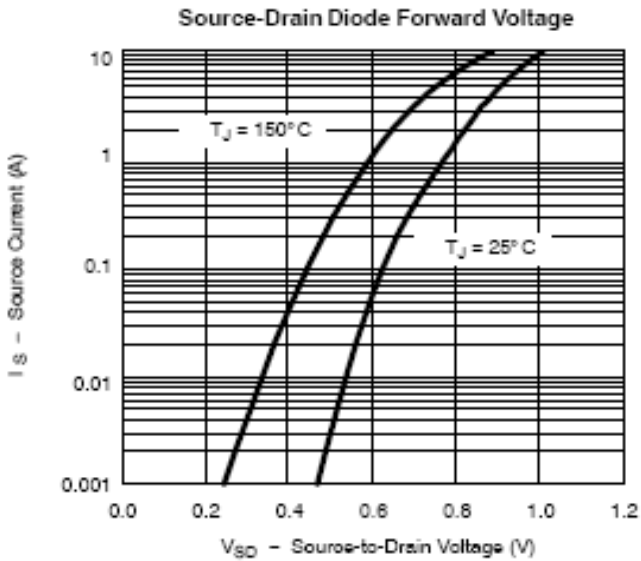
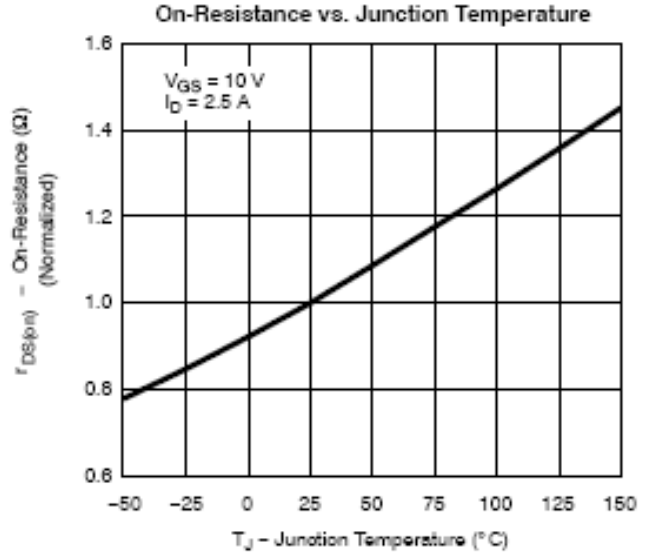
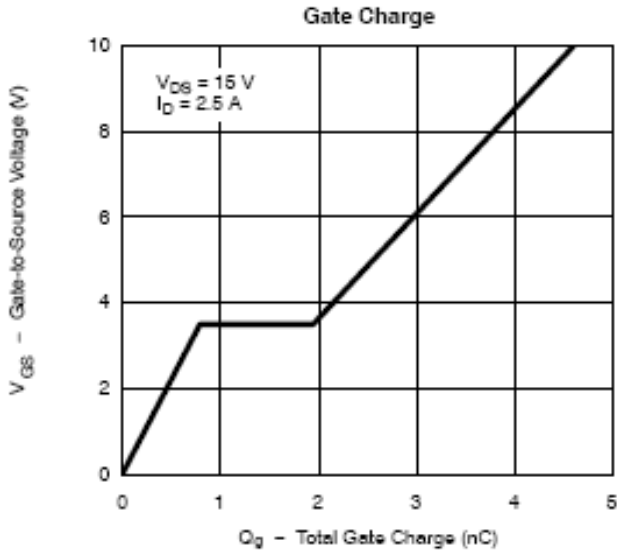
TYPICAL CHARACTERISTICS





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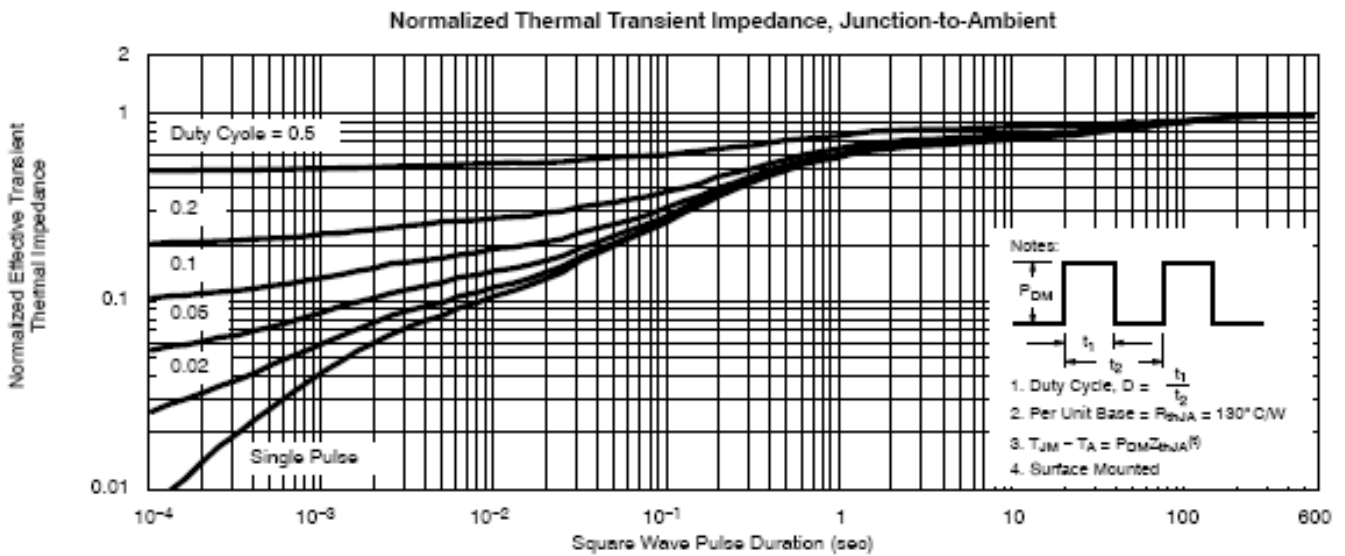
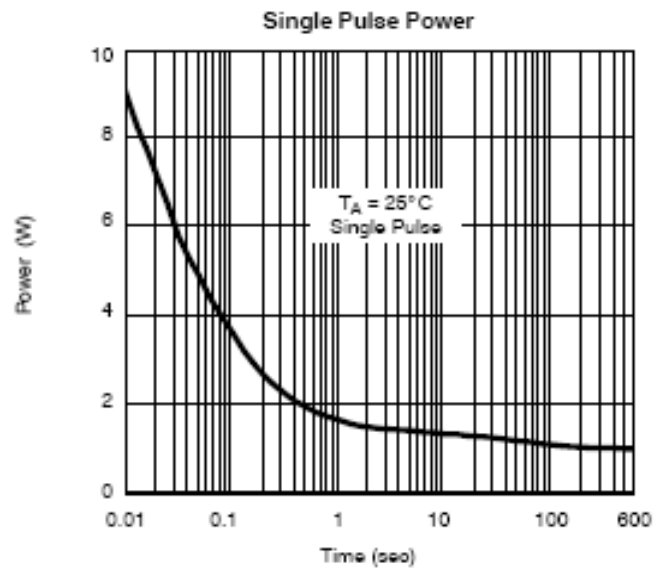
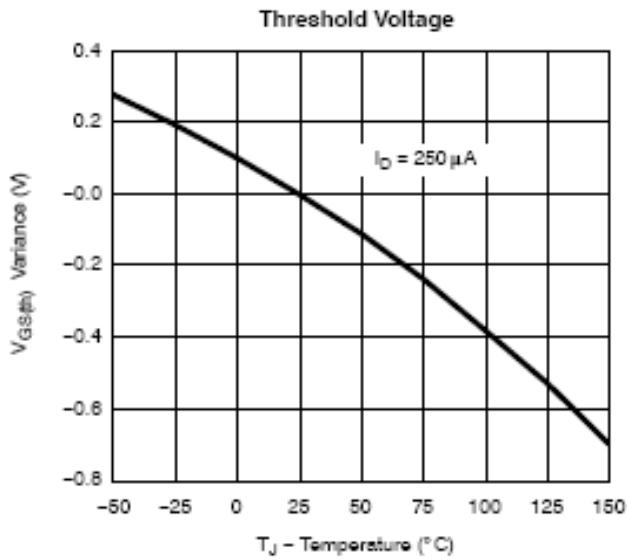




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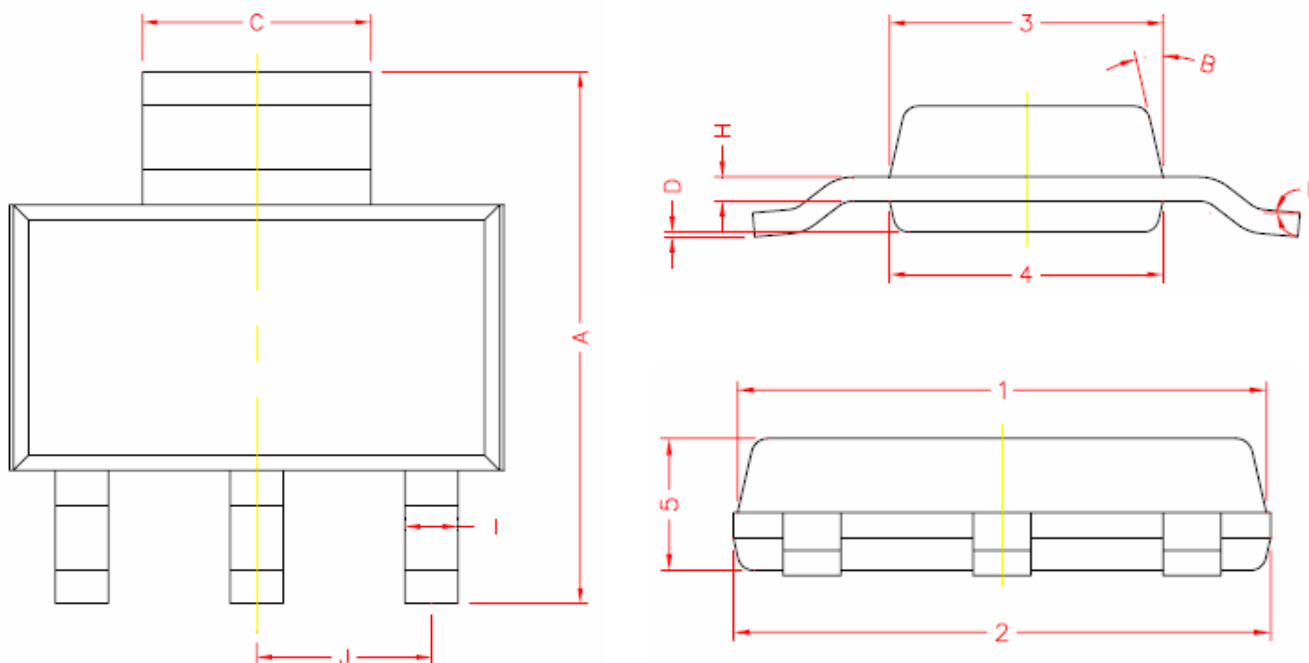




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SOT-233 PACKAGE OUTLINE



REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	6.70	7.30
C	2.90	3.10
D	0.02	0.10
E	0°	10°
I	0.60	0.80
H	0.25	0.35
B	13° TYP.	
J	2.30 REF.	
1	6.30	6.70
2	6.30	6.70
3	3.30	3.70
4	3.30	3.70
5	1.40	1.80



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