Low Capacitance ESD Protection Array For High Speed Data Interfaces

Features

- ESD Protect for 2 high-speed I/O channels
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 12A (8/20μs)
- 5V operating voltage
- Low capacitance : 2pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology

Applications

- USB2.0 Power and Data lines protection
- Notebook and PC Computers
- Monitors and Flat Panel Displays
- IEEE 1394 Firewire Ports
- Video Graphics Cards
- SIM ports

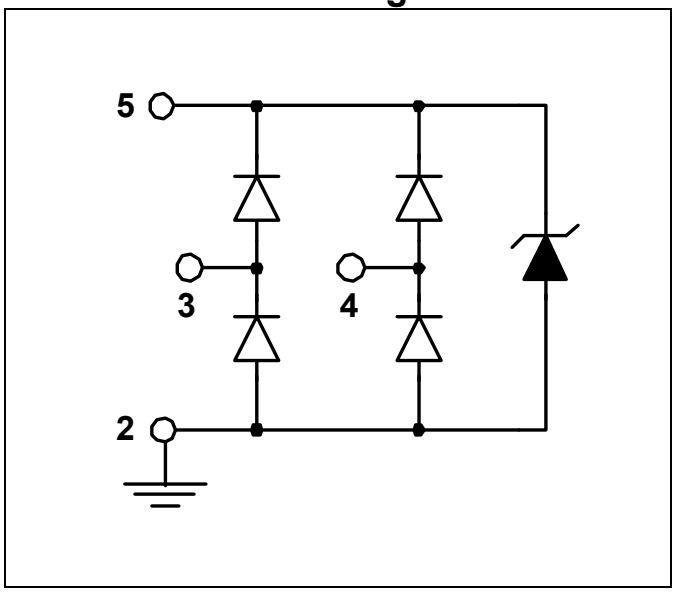
Description

SSEPAA5-02S is a high performance design which includes surge rated diode arrays to protect high speed data interfaces. The SSEPAA5-02S has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

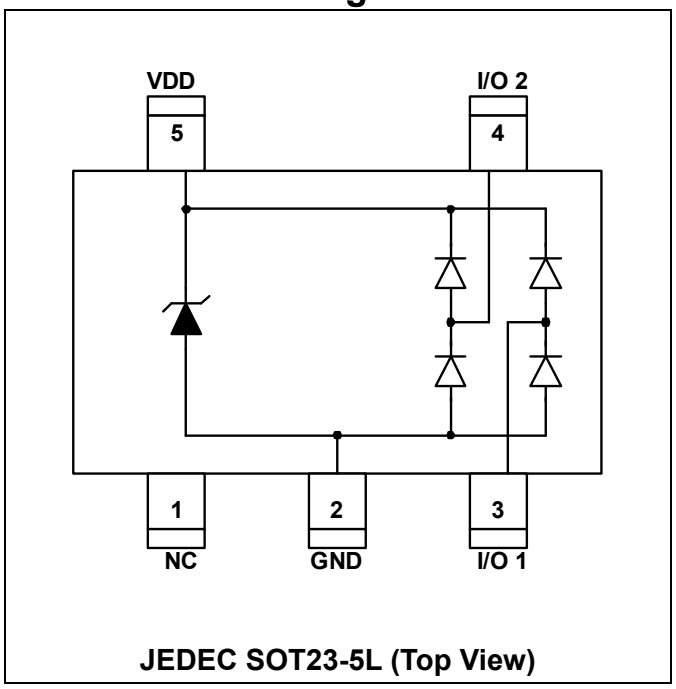
SSEPAA5-02S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

SSEPAA5-02S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



JEDEC SOT23-5L (Top View)

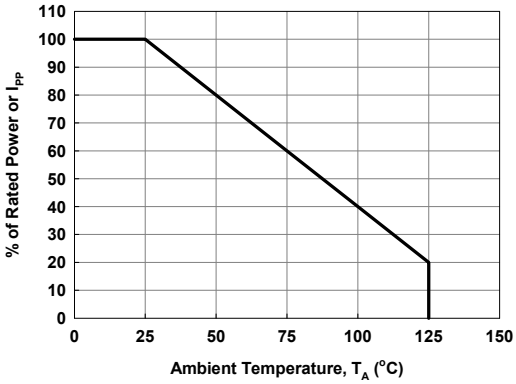
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	13	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	24 16	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +125	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

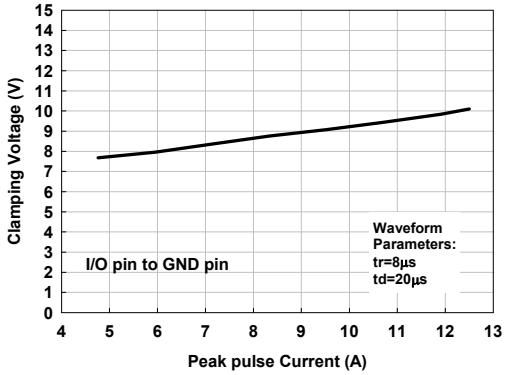
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to pin 2, T=25 °C			5	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, Pin 5 to pin 2			5	**μA**
Channel Leakage Current	I_{CH_Leak}	$V_{Pin\ 5}$ = 5V, $V_{Pin\ 2}$ = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C Pin 5 to Pin 2	6.1		9	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C Pin2 to Pin 5		0.7	1	**V**
Clamping Voltage	V_{CL}	I_{PP}=5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		7.8	8.5	**V**
ESD Holding Voltage	V_{hold}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		13		**V**
Channel Input Capacitance	C_{IN}	V_{pin5} = 5V, V_{pin2} = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C, Any Channel pin to Ground		2	3	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin5} = 5V, V_{pin2} = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C , Between Channel pins		0.08	0.15	**pF**
Variation of Channel Input Capacitance	$\triangle C_{IN}$	V_{pin5} = 5V, V_{pin2} = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C , Channel_x pin to Ground - Channel_y pin to Ground		0.03	0.06	**pF**

Typical Characteristics

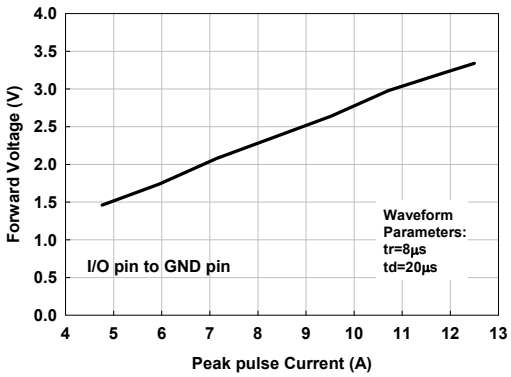
Power Derating Curve



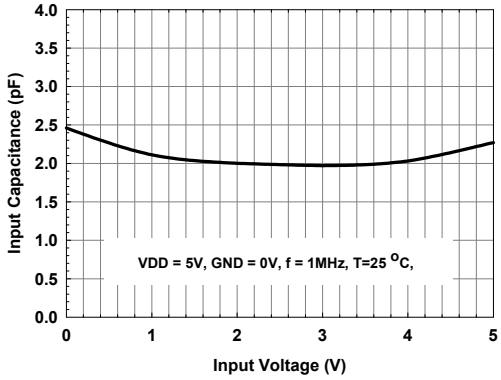
Clamping Voltage vs. Peak Pulse Current



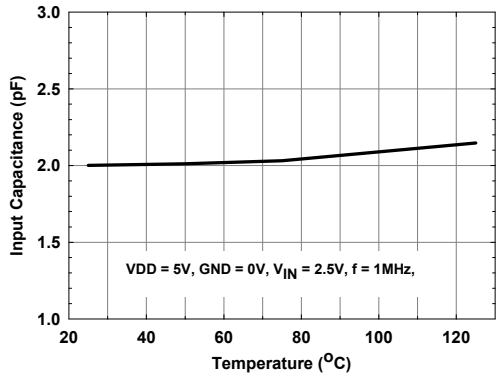
Forward Voltage vs. Forward Current



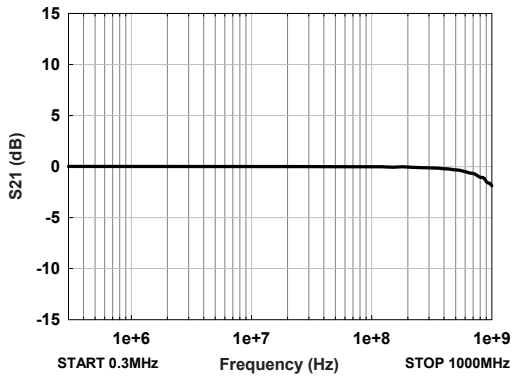
Typical Variation of C_{IN} vs. V_{IN}



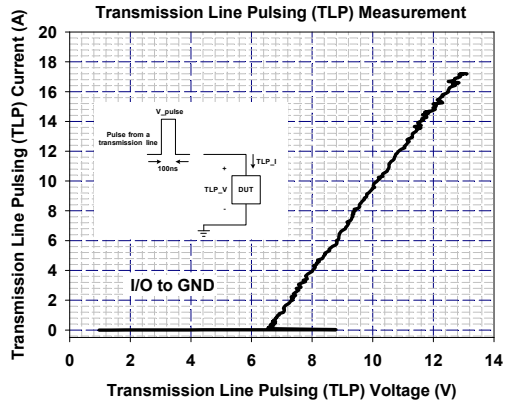
Typical Variation of C_{IN} vs. Temp



Insertion Loss S21



Transmission Line Pulsing (TLP) Measurement



Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or 30/(1x10-9). So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The SSEPAA5-02S has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

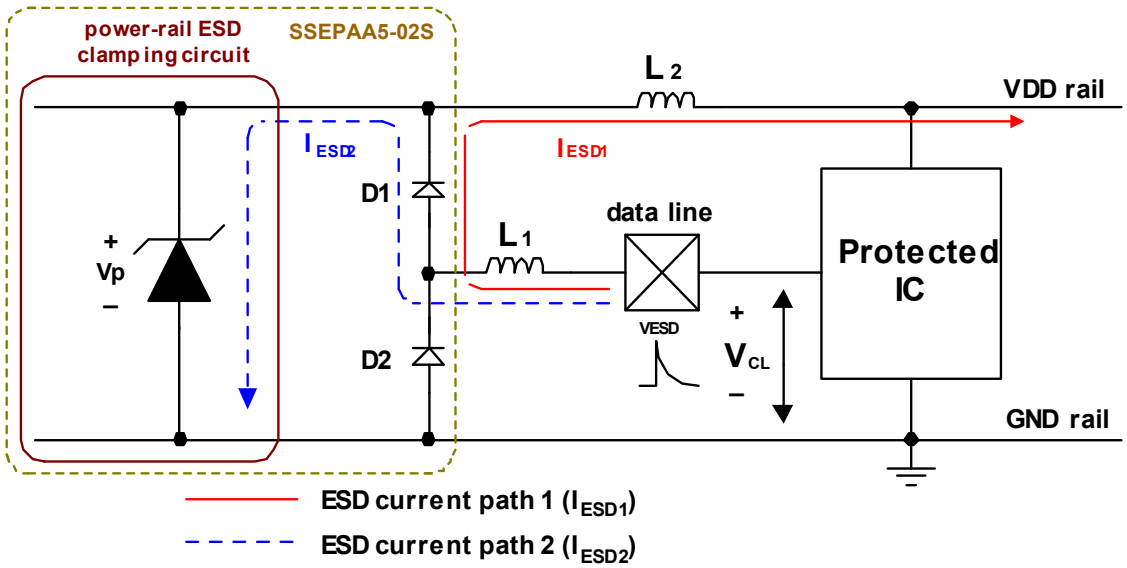


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The SSEPAA5-02S is designed to protect two data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of SSEPAA5-02S is shown in the Fig. 2. In Fig. 2, the two protected data lines are connected to the ESD protection pins (pin3 and pin4) of SSEPAA5-02S. The ground pin (pin2) of SSEPAA5-02S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of SSEPAA5-02S is a positive reference pin. This pin should directly connect to the VDD rail of PCB. When pin 5 of SSEPAA5-02S is connected to the VDD rail, the leakage current of ESD protection pin of SSEPAA5-02S becomes very small. Because the pin 5 of SSEPAA5-02S is directly connected to VDD rail, the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of SSEPAA5-02S.

SSEPAA5-02S can provide protection for 2 I/O signal lines simultaneously. If the number of I/O signal lines is less than 2, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the SSEPAA5-02S.

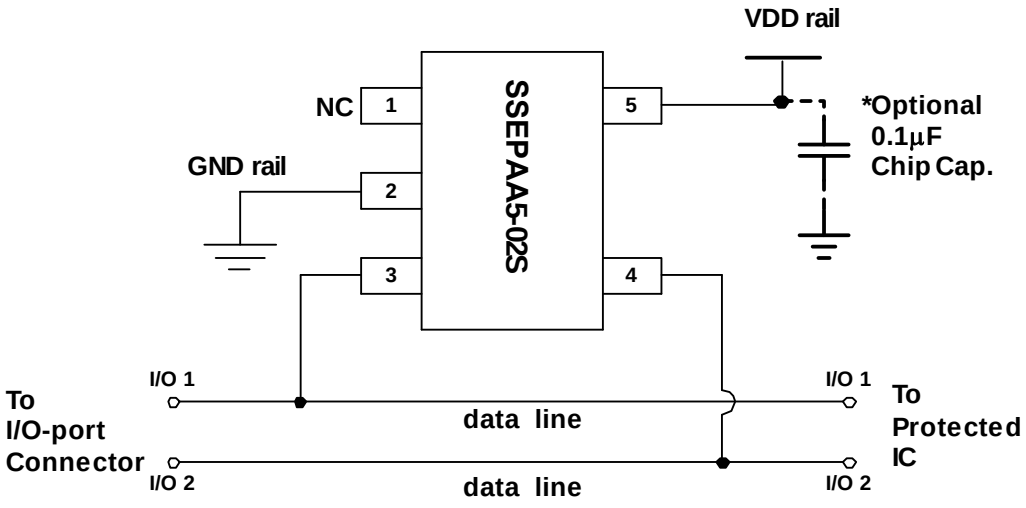


Fig. 2 Data lines and power rails connection of SSEPAA5-02S.

C. Applications

1. Universal Serial Bus (USB) ESD Protection

The SSEPAA5-02S can be used to protect the USB port on the monitors, computers, peripherals or portable systems. The ESD protection scheme for single USB ports is shown in Fig. 3. In the Fig.3,the voltage bus (V_{BUS}) of USB ports are connected to the power pin (pin 5) of SSEPAA5-02S. Each data line (D+/D-) of USB port is connected to the ESD protection pin of SSEPAA5-02S.

When ESD voltage pulse appears on the data line, the ESD pulse current will be conducted by SSEPAA5-02S away from the USB controller chip. In addition, the ESD pulse current also can be conducted by SSEPAA5-02S away from the USB controller chip when the ESD voltage pulse appears on the voltage bus (V_{BUS}) of USB port. Therefore, the data lines (D+/D-) and voltage bus (V_{BUS}) of two USB ports are complementally protected with an SSEPAA5-02S.

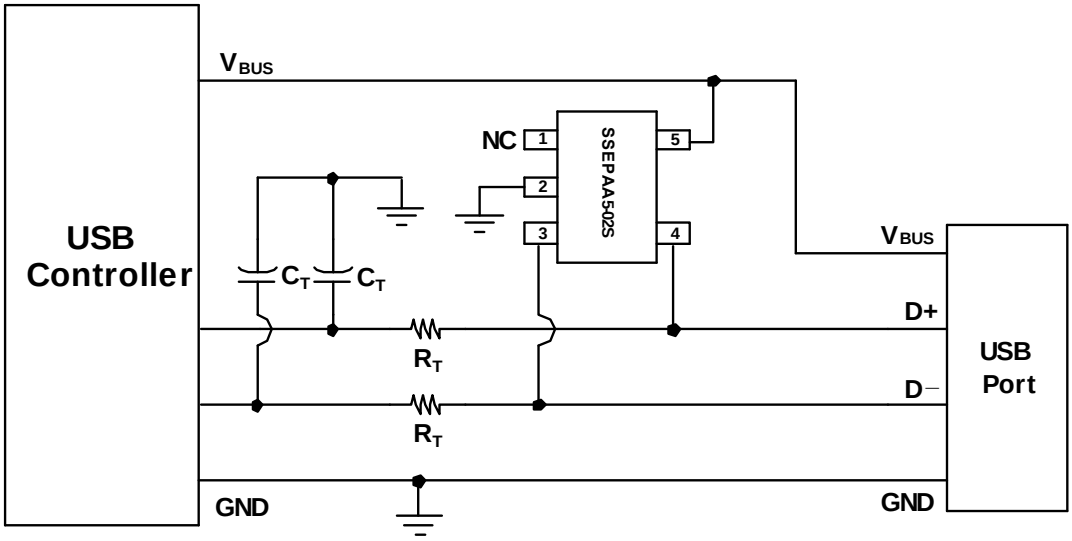


Fig. 3 ESD Protection scheme for single USB ports by using SSEPAA5-02S.

2. Audio Interface ESD Protection

For the audio interface, the Right/Left channels should be protected from the ESD stress. The SSEPAA5-02S can be used for the audio interface ESD protection. The ESD protection scheme for audio interface is shown in the Fig. 4. In the Fig. 4, the Right and Left channels of audio connector are connected to ESD protection pins (such as pin 3 and pin 4) of SSEPAA5-02S. For the power pin (pin 5) of SSEPAA5-02S, it should directly connect to the VDD power supply. As well, for the ground pin (pin 2) of SSEPAA5-02S, it should directly connect to the Ground plate.

When ESD voltage pulse appears on the Right/Left channel of audio connector, the ESD pulse current will be discharged by SSEPAA5-02S. Therefore, the Right/Left channels of audio chip are complementally protected with an SSEPAA5-02S.

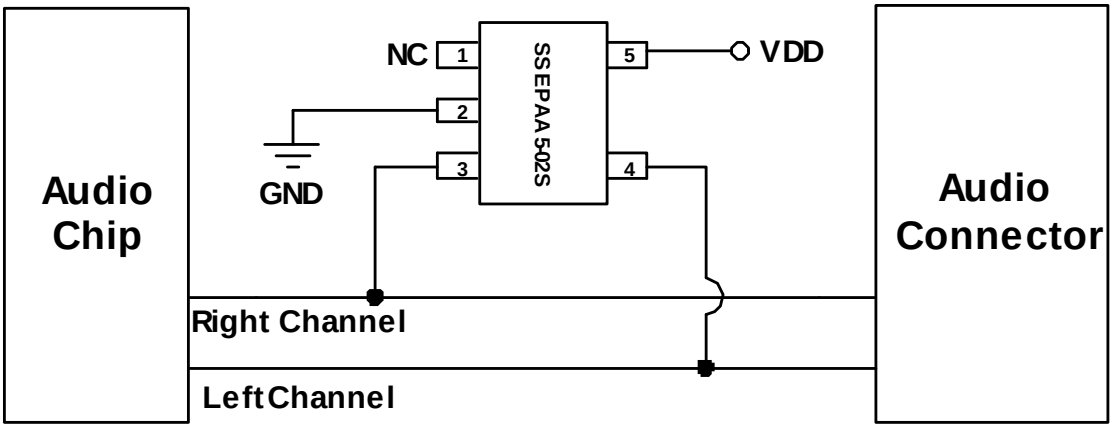


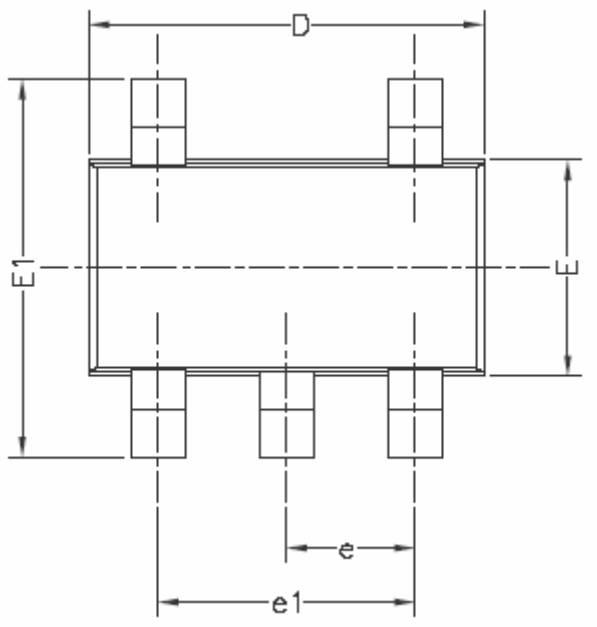
Fig. 4 ESD Protection scheme for audio interface by using SSEPAA5-02S.

Mechanical Details

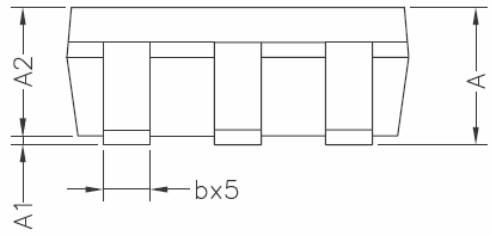
SOT23-5L

PACKAGE DIAGRAMS

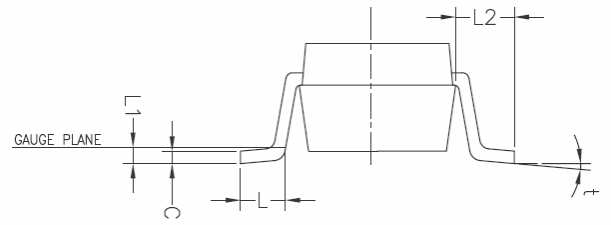
TOP VIEW



SIDE VIEW



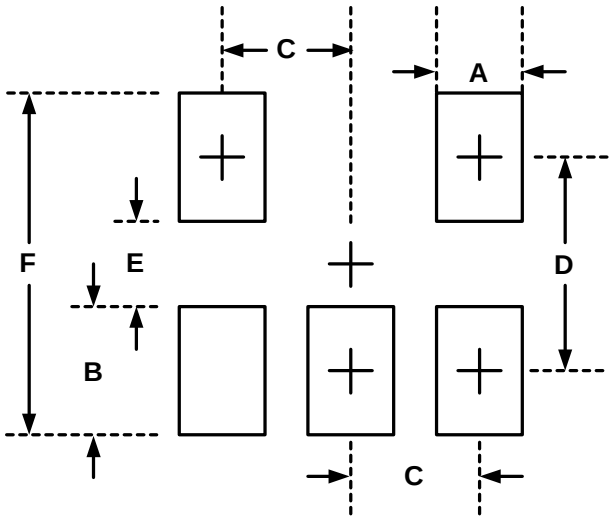
END VIEW



PACKAGE DIMENSIONS

Symbol	Milimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.95	1.45	.037	.057
A1	0.05	0.15	.002	.006
A2	0.90	1.30	.035	.051
b	0.35	0.50	.0137	.019
C	0.08	0.20	.0031	.0078
D	2.84	3.00	.1118	.118
E	1.50	1.70	.059	.0669
E1	2.60	3.00	.102	.118
e	0.95 BSC.		.0374 BSC.	
e1	1.90 BSC.		.0748 BSC.	
L	0.35	0.55	.0137	.0216
L1	0.10 BSC.		.0039 BSC.	
L2	0.60 REF.		.0236 REF.	
θ	0°	8°	0°	8°

LAND LAYOUT

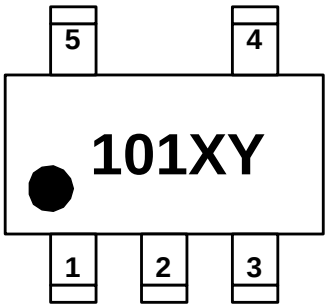


Dimensions		
Index	**Millimeter**	**Inches**
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
SSEPAA5-02S	101XY

101 = Device Code

X = Date Code

Y = Control Code

Revision History

Revision	Modification Description
Revision 2006/8/28	Original Release.
Revision 2007/02/05	1. Change the clamping cell symbol for easy understanding. 2. Change the expression of C_{IN} from @ V_{IN}=0V to @ V_{IN}=2.5V. 3. Add the TLP characterization. 4. Add the ESD holding voltage characterization under IEC 61000-4-2 +6kV contact mode at I/O channel to GND. 5. Update the clamping voltage to (typ=7.8V, max=9V). 6. Correct typos.
Revision 2007/02/27	Update the spec of V_F & V_{CL}.
Revision 2007/05/15	Update the Marking Code from 101X to 101XY.