HAT2165N

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Silicon N Channel Power MOS FET
Power Switching

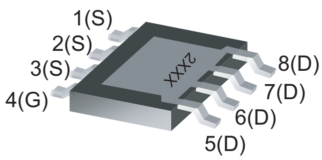
REJ03G1680-0300
Rev.3.00
May 27, 2008

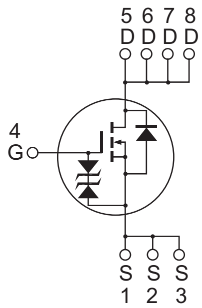
Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 2.8 mΩ typ. (at V_{GS} = 10 V)

Outline

RENESAS Package code: PTSP0008DC-A
(Package name: LFPAK-i)





1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	55	A
Drain peak current	$I_{D(pulse)}$ Note1	220	A
Body-drain diode reverse drain current	I_{DR}	55	A
Avalanche current	I_{AP} Note 2	30	A
Avalanche energy	E_{AR} Note 2	90	mJ
Channel dissipation	Pch Note3	30	W
Channel to case thermal resistance	θch-C	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. Tc = 25°C

Electrical Characteristics

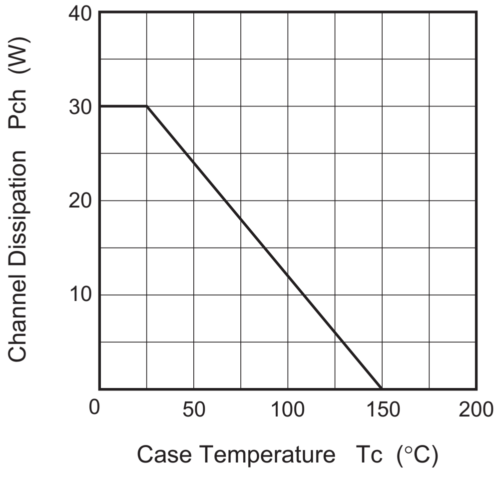
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	2.8	3.6	mΩ	I_D = 27.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	3.7	5.6	mΩ	I_D = 27.5 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	60	100	—	S	I_D = 27.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	5180	—	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	1200	—	pF	
Reverse transfer capacitance	Crss	—	380	—	pF	
Gate resistance	Rg	—	0.5	—	Ω	
Total gate charge	Qg	—	33	—	nc	V_{DD} = 10 V V_{GS} = 4.5 V I_D = 55 A
Gate to source charge	Qgs	—	15	—	nc	
Gate to drain charge	Qgd	—	7.1	—	nc	
Turn-on delay time	$t_{d(on)}$	—	13	—	ns	V_{GS} = 10 V, I_D = 27.5 A V_{DD} ≅ 10 V R_L = 0.36 Ω Rg = 4.7 Ω
Rise time	t_r	—	65	—	ns	
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	
Fall time	t_f	—	9.5	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.81	1.06	V	I_F = 55 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	40	—	ns	I_F = 55 A, V_{GS} = 0 di_F/ dt = 100 A/ µs

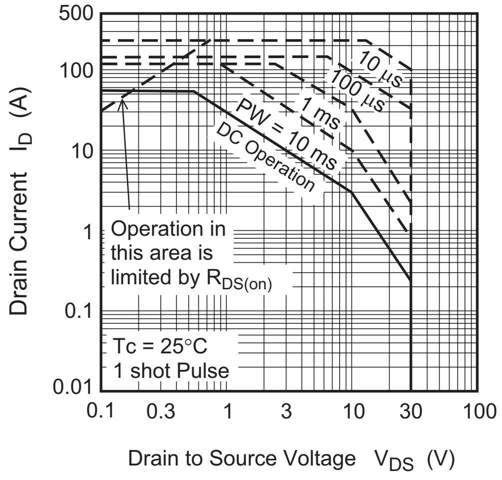
Notes: 4. Pulse test

Main Characteristics

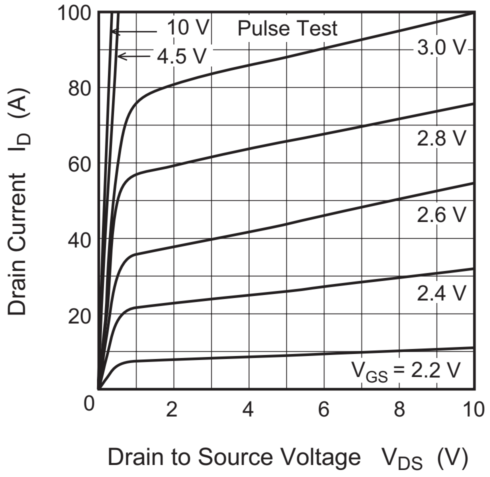
Power vs. Temperature Derating



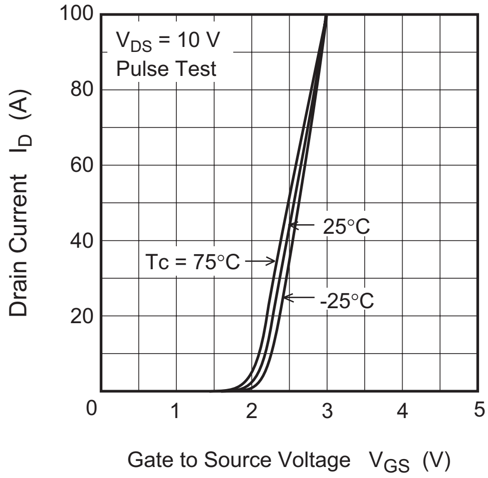
Maximum Safe Operation Area



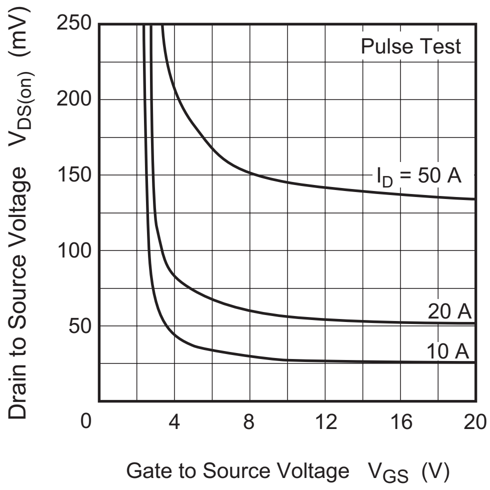
Typical Output Characteristics



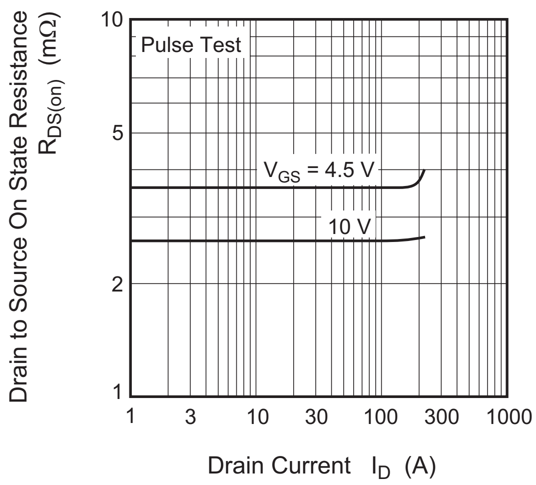
Typical Transfer Characteristics

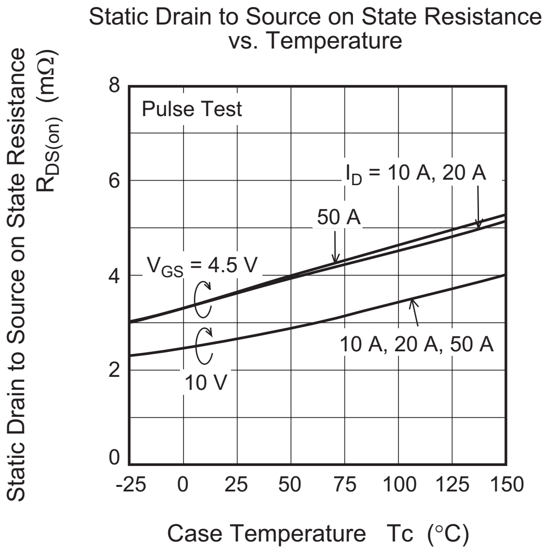


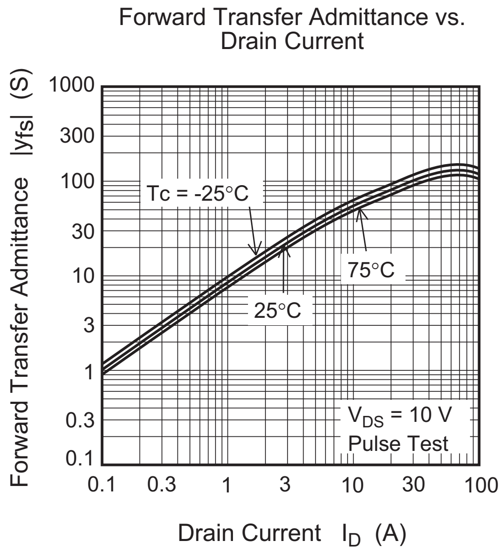
Drain to Source Saturation Voltage vs.
Gate to Source Voltage

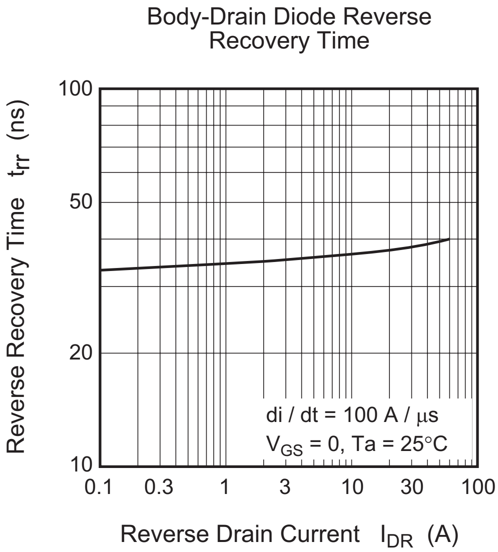


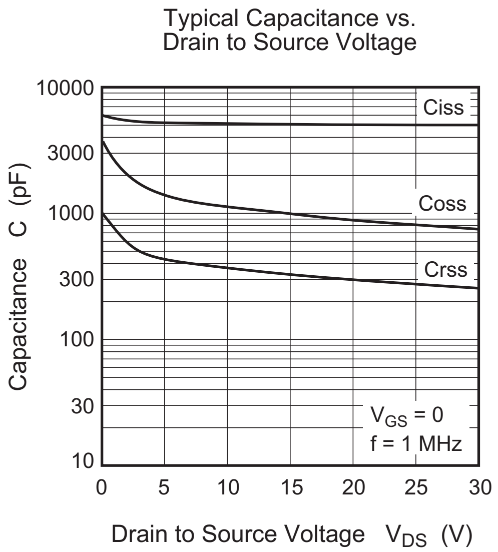
Static Drain to Source on State Resistance
vs. Drain Current

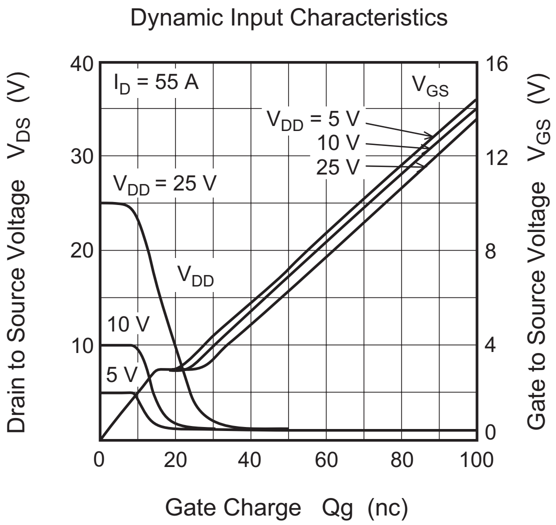


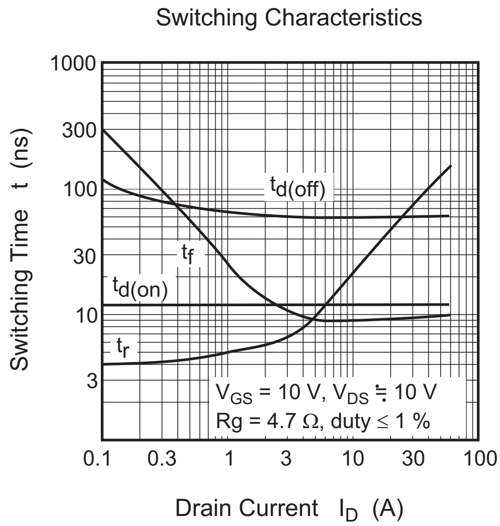

Static Drain to Source on State Resistance vs. Temperature
Static Drain to Source on State Resistance $R_{DS(on)}$ (mΩ)
Pulse Test
I_D = 10 A, 20 A
50 A
V_{GS} = 4.5 V
10 A, 20 A, 50 A
10 V
8
6
4
2
0
-25
0
25
50
75
100
125
150
Case Temperature Tc (°C)

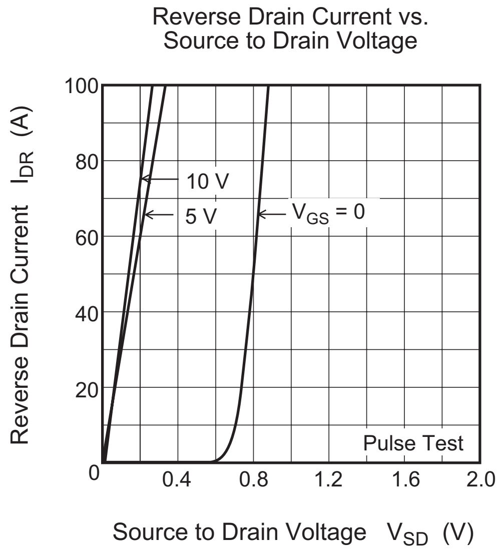

Forward Transfer Admittance vs. Drain Current
Forward Transfer Admittance |yfs| (S)
1000
300
100
30
10
3
1
0.3
0.1
Tc = -25°C
75°C
25°C
V_{DS} = 10 V
Pulse Test
0.1
0.3
1
3
10
30
100
Drain Current I_D (A)

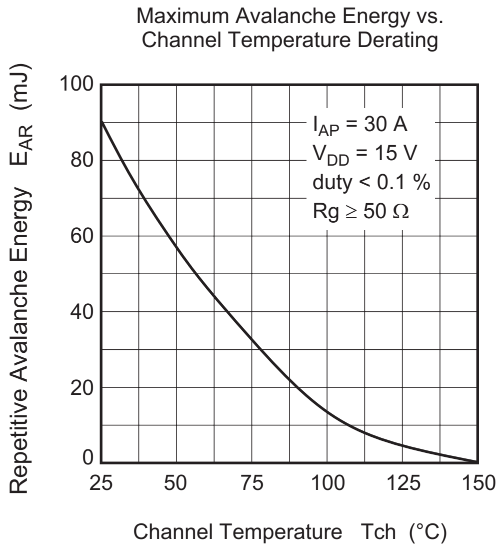

Body-Drain Diode Reverse Recovery Time
Reverse Recovery Time t_{rr} (ns)
100
50
20
10
di / dt = 100 A / μs
V_{GS} = 0, Ta = 25°C
0.1
0.3
1
3
10
30
100
Reverse Drain Current I_{DR} (A)

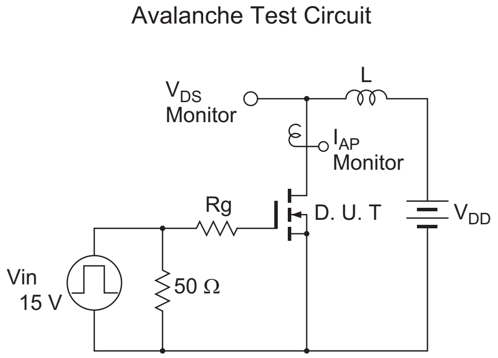

Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
10000
3000
1000
300
100
30
10
Ciss
Coss
Crss
V_{GS} = 0
f = 1 MHz
0
5
10
15
20
25
30
Drain to Source Voltage V_{DS} (V)

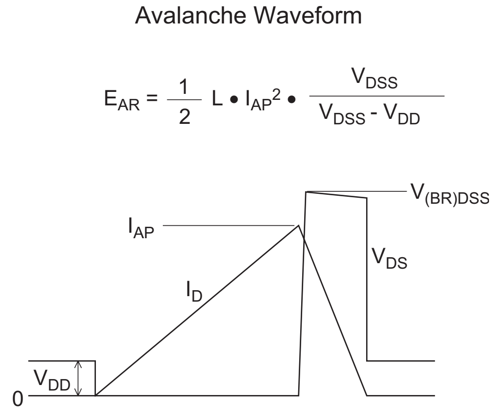

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
40
30
20
10
16
12
8
4
0
I_D = 55 A
V_{GS}
V_{DD} = 5 V
10 V
25 V
V_{DD} = 25 V
V_{DD}
10 V
5 V
0
20
40
60
80
100
Gate Charge Qg (nc)

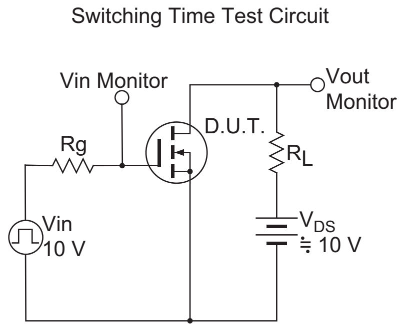

Switching Characteristics
Switching Time t (ns)
1000
300
100
30
10
3
$t_{d(off)}$
t_f
$t_{d(on)}$
t_r
V_{GS} = 10 V, V_{DS} ≒ 10 V
Rg = 4.7 Ω, duty ≤ 1 %
0.1
0.3
1
3
10
30
100
Drain Current I_D (A)

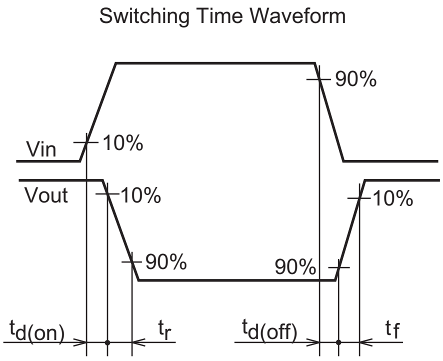

Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I_DR (A)
100
80
60
40
20
0
0.4
0.8
1.2
1.6
2.0
10 V
5 V
V_GS = 0
Pulse Test
Source to Drain Voltage V_SD (V)


Maximum Avalanche Energy vs.
Channel Temperature Derating
Repetitive Avalanche Energy E_AR (mJ)
100
80
60
40
20
0
25
50
75
100
125
150
I_AP = 30 A
V_DD = 15 V
duty < 0.1 %
Rg ≥ 50 Ω
Channel Temperature Tch (°C)


Avalanche Test Circuit
V_DS
Monitor
L
I_AP
Monitor
Rg
D. U. T
V_DD
Vin
15 V
50 Ω

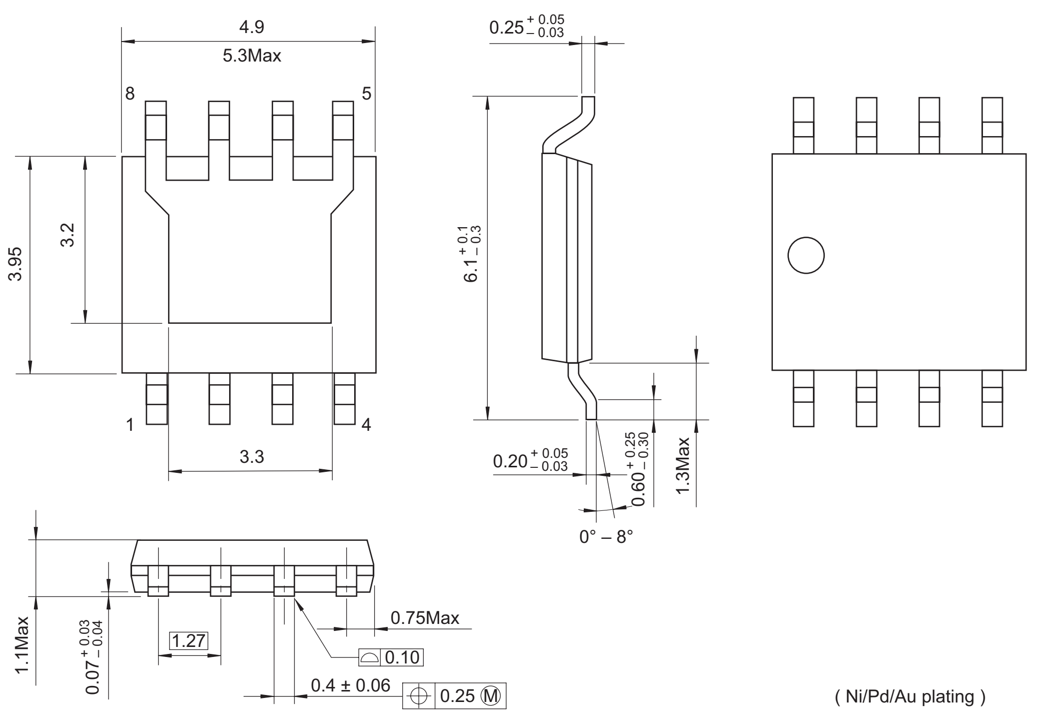

Avalanche Waveform
E_AR = 1/2 L • I_AP^2 • V_DSS / (V_DSS - V_DD)
V_(BR)DSS
I_AP
V_DS
I_D
V_DD
0


Switching Time Test Circuit
Vin Monitor
Vout
Monitor
D.U.T.
Rg
R_L
Vin
10 V
V_DS
≒ 10 V


Switching Time Waveform
90%
Vin
10%
Vout
10%
10%
90%
90%
td(on)
tr
td(off)
tf

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LFPAK-i	—	PTSP0008DC-A	LFPAK-iV	0.080g



Ordering Information

Part No.	Quantity	Shipping Container
HAT2165N-EL-E	2500 pcs	Taping

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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