800MHz TTL/CMOS Potato Chip

FEATURES:

. Patented technology
. Operating frequency up to 800MHz with 2pf load
. Operating frequency up to 600MHz with 5pf load
. Operating frequency up to 350MHz with 15pf load
. Operating frequency up to 120MHz with 50pf load
. Very low output pin to pin skew < 80ps
. Very low pulse skew < 250ps
. VCC = 1.65V to 3.6V
. Propagation delay < 2.0 ns max with 15pf load
. Low input capacitance: 3pf typical
. 1:10 fanout
. Available in 20pin 150mil wide QSOP package
. Available in 20pin 300mil wide SOIC package
. Available in 20pin 209mil wide SSOP package

DESCRIPTION:

Potato Semiconductor's PO49FCT3807B is designed for world top performance using submicron CMOS technology to achieve 800MHz output frequency with less than 80ps output skew.

PO49FCT3807B is a 1.65V to 3.6V CMOS 1 input to 10 Output Buffered Driver.
Typical applications are clock and signal distribution.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

Pin Configuration
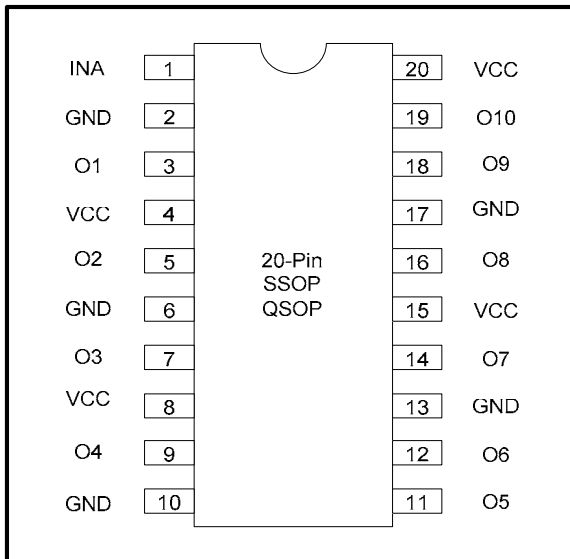
Logic Block Diagram
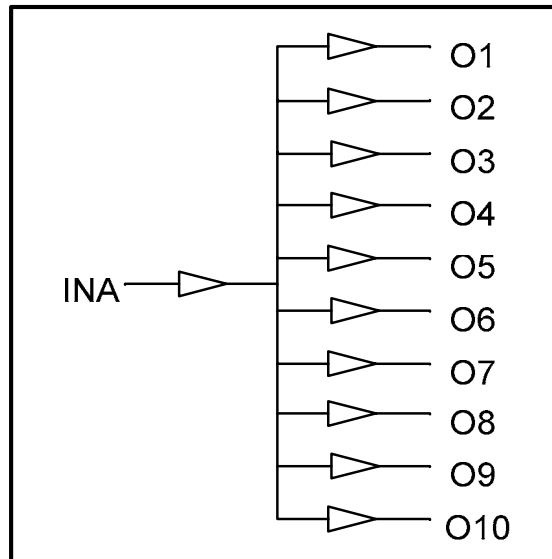
Pin Description

Pin Name	Description
INA	Input
O1 to O10	Outputs

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Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=V_{IH} or VIL, IOH= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=V_{IH} or VIL, IOH=12mA	-	0.4	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	5.5	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	50	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-50	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And I_{IN} = -18mA	-	-0.7	-1.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

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3.3V Dual 1:10 CMOS Clock Buffered Driver

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Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Max	Unit
C_{in}	Input Capacitance	Vin = 0V	3	4	pF
C_{out}	Output Capacitance	Vout = 0V	-	6	pF

Notes:
1 This parameter is determined by device characterization but not production tested.
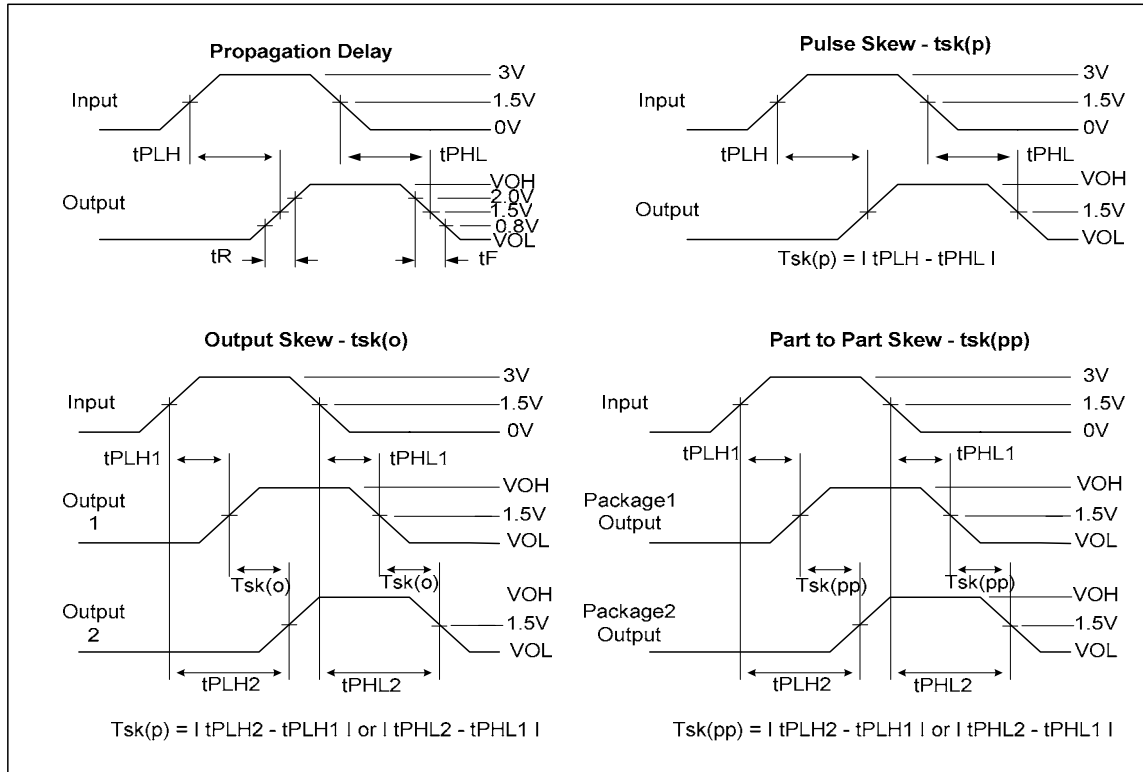
Switching Characteristics

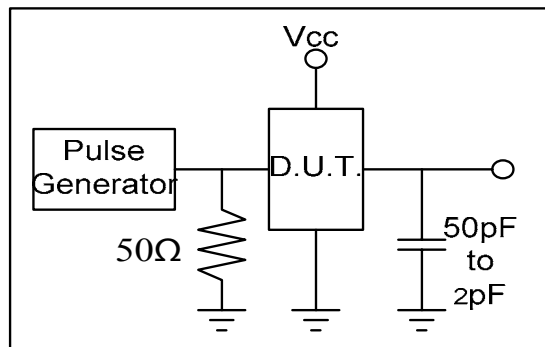| Symbol	Description	Test Conditions (1)	Max	Unit
t_{PLH}	Propagation Delay A to Bn	CL = 15pF	2.0	ns
t_{PHL}	Propagation Delay A to Bn	CL = 15pF	2.0	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
$t_{sk(p)}$	Pulse Skew (Same Package)	CL = 15pF, 125MHz	250	ps
$t_{sk(o)}$	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	80	ps
$t_{sk(pp)}$	Output Skew (Different Package)	CL = 15pF, 125MHz	400	ps
fmax	Input Frequency	CL = 50pF	120	MHz
fmax	Input Frequency	CL =15pF	350	MHz
fmax	Input Frequency	CL = 5pF	600	MHz
fmax	Input Frequency	CL = 2pF	800	MHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

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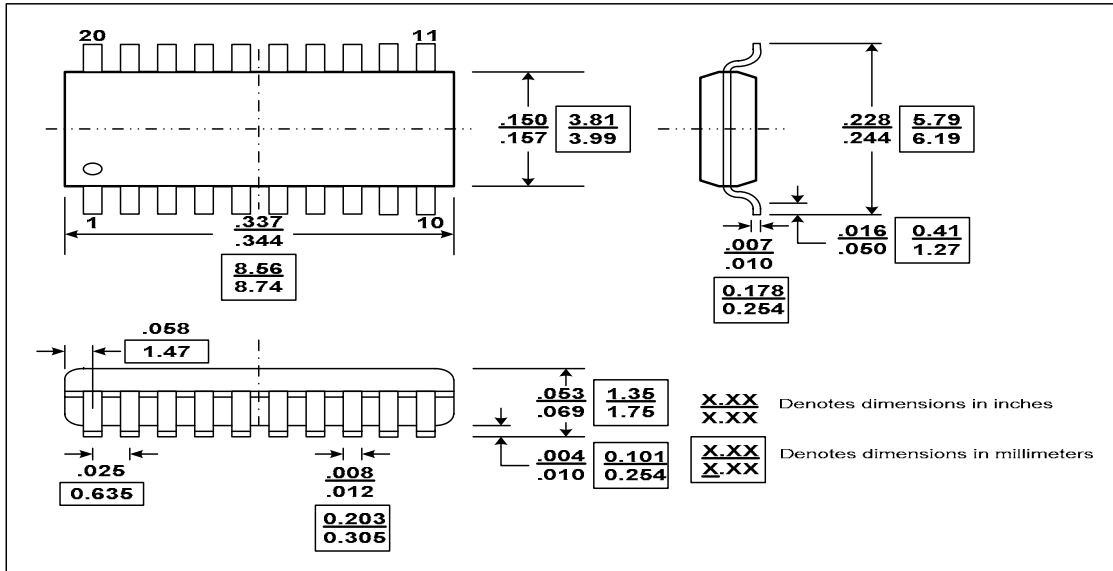
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Test Waveforms

Test Circuit

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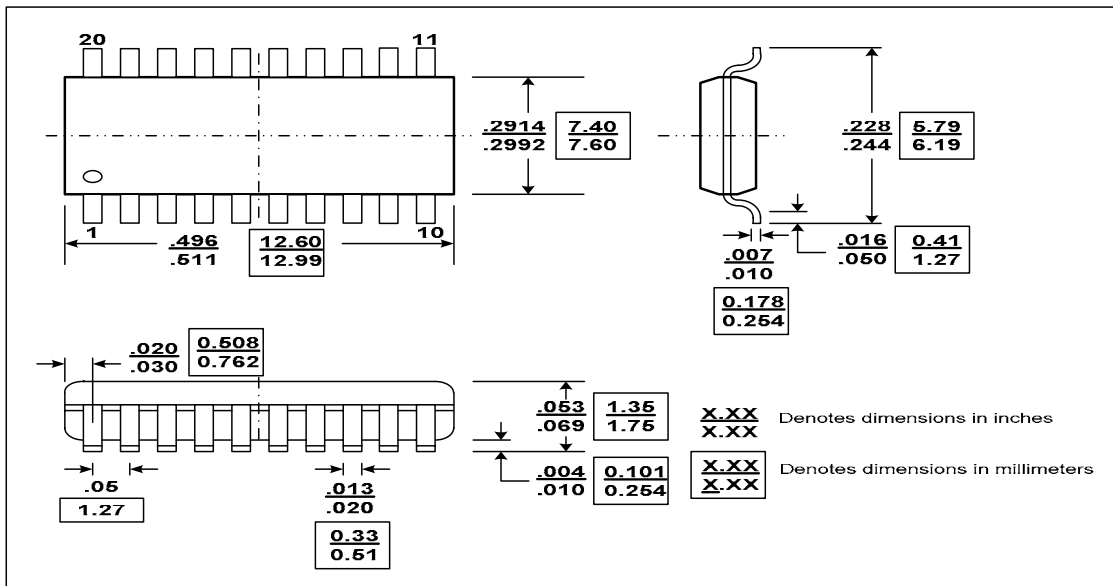
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Packaging Mechanical Drawing: 20 pin QSOP

Packaging Mechanical Drawing: 20 pin SOIC

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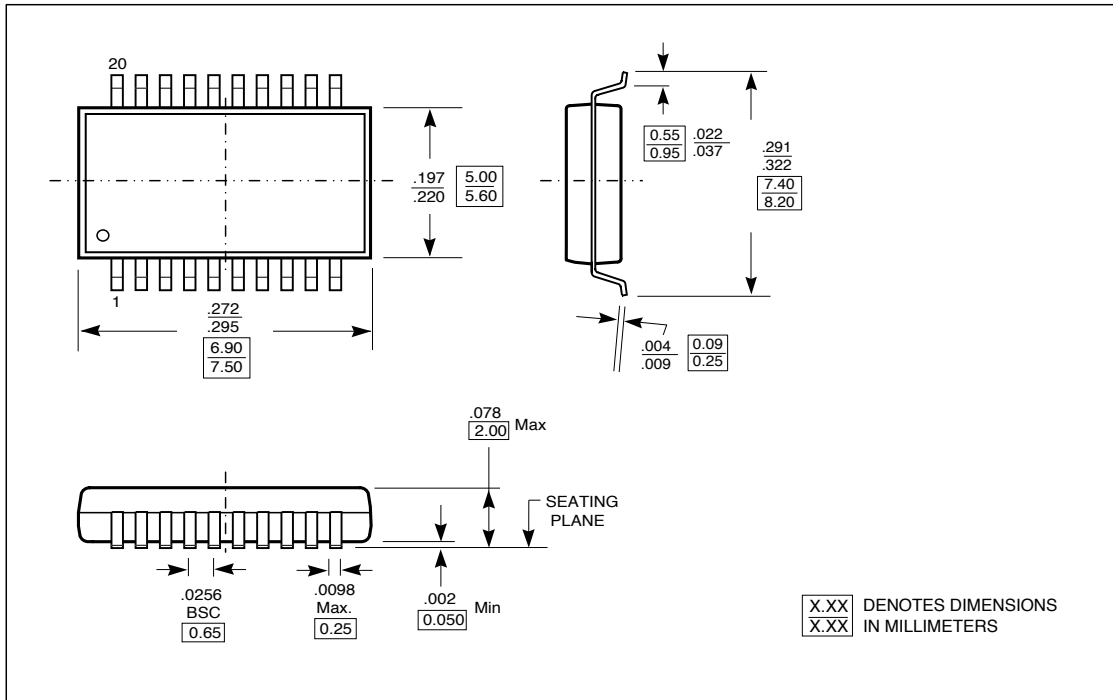
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Ordering Information

Ordering Code	Package			Top-Marking	T$_A$
PO49FCT3807BCU	20pin SOIC	Tube	Pb-free & Green	PO49FCT3807BC	-40°C to 85°C
PO49FCT3807BCR	20pin SOIC	Tape and reel	Pb-free & Green	PO49FCT3807BC	-40°C to 85°C
PO49FCT3807BQU	20-pin QSOP	Tube	Pb-free & Green	PO49FCT3807BQ	-40°C to 85°C
PO49FCT3807BQR	20-pin QSOP	Tape and reel	Pb-free & Green	PO49FCT3807BQ	-40°C to 85°C
PO49FCT3807BSU	20-pin SSOP	Tube	Pb-free & Green	PO49FCT3807BS	-40°C to 85°C
PO49FCT3807BSR	20-pin SSOP	Tape and reel	Pb-free & Green	PO49FCT3807BS	-40°C to 85°C