

2SJ553(L), 2SJ553(S)

Silicon P Channel MOS FET

REJ03G0900-0400
(Previous: ADE-208-650B)
Rev.4.00
Sep 07, 2005

Description

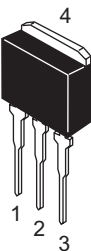
High speed power switching

Features

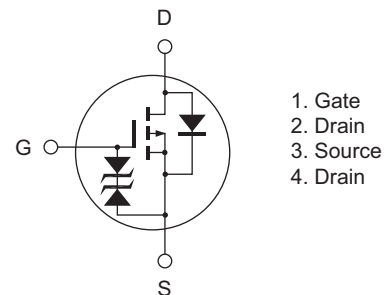
- Low on-resistance
 $R_{DS(on)} = 0.028 \Omega$ typ.
- Low drive current.
- 4 V gate drive devices.
- High speed switching.

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-30	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-120	A
Body to drain diode reverse drain current	I _{DR}	-30	A
Avalanche current	I _{AP} ^{Note 3}	-30	A
Avalanche energy	E _{AR} ^{Note 3}	77	mJ
Channel dissipation	P _{ch} ^{Note 2}	75	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_c = 25°C
 3. Value at T_{ch} = 25°C, R_g ≥ 50 Ω

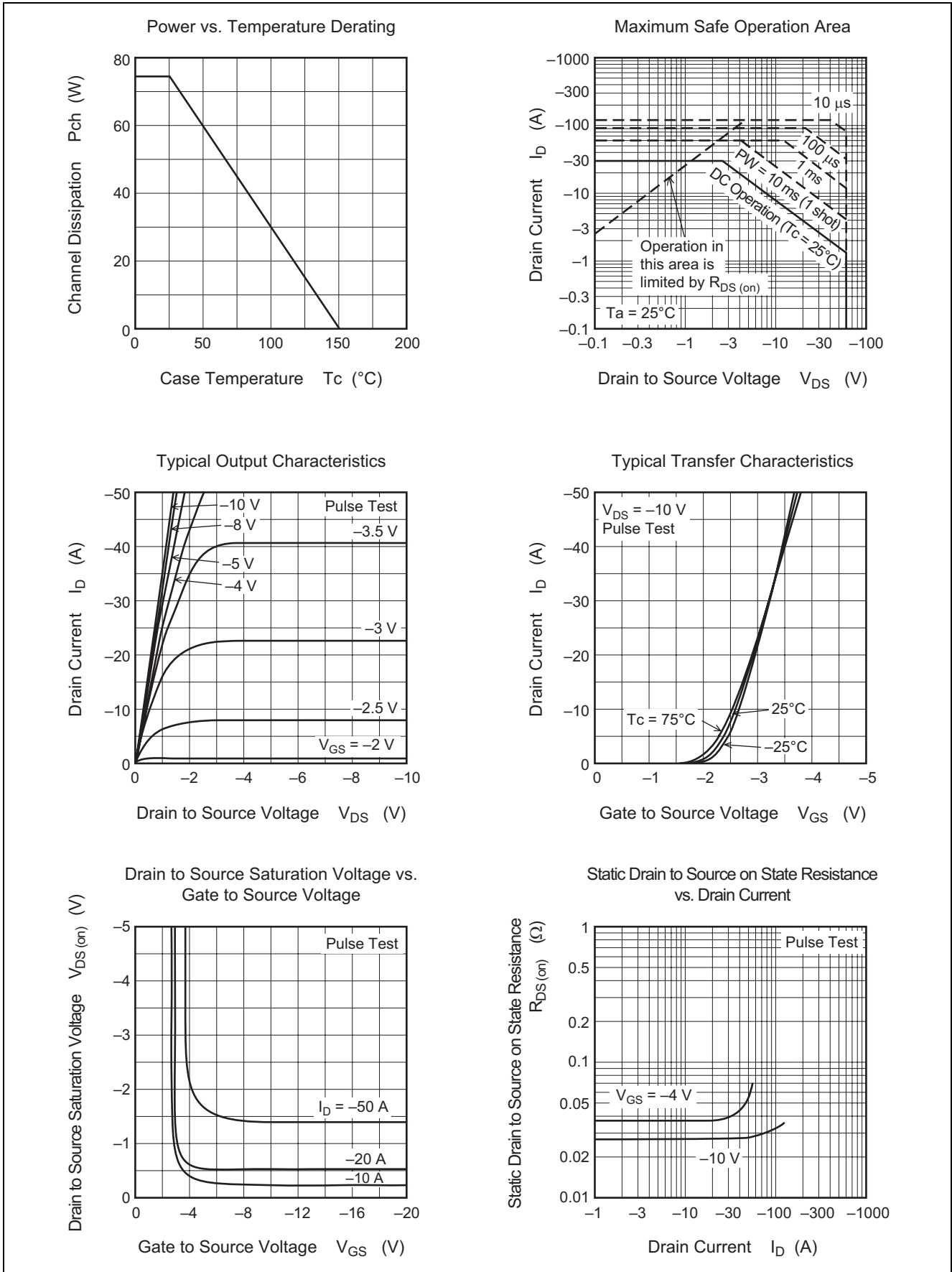
Electrical Characteristics

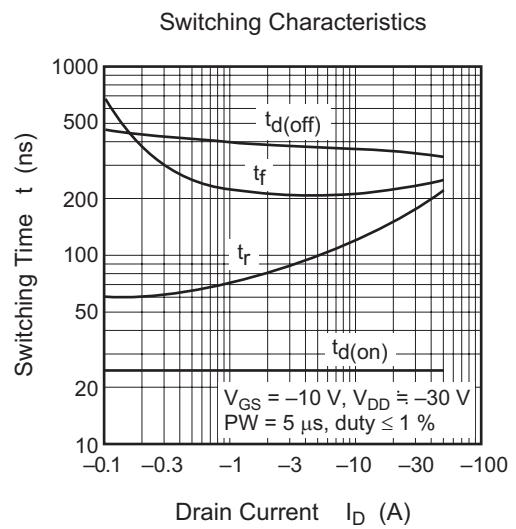
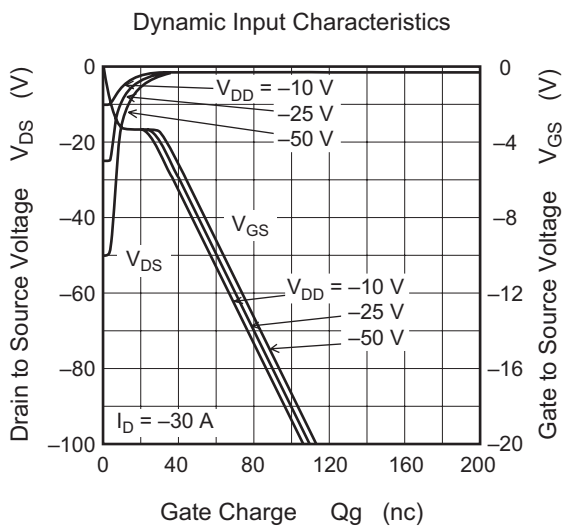
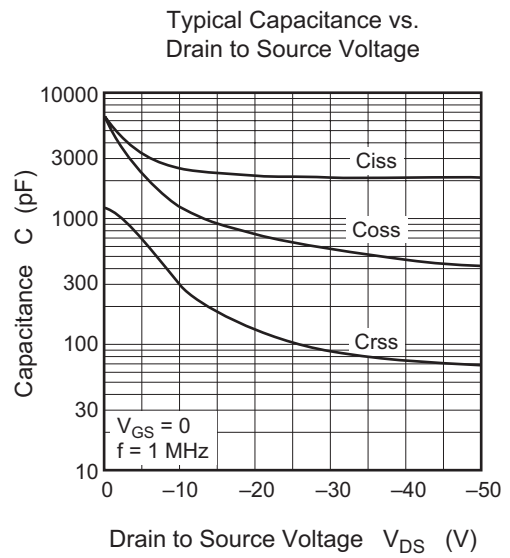
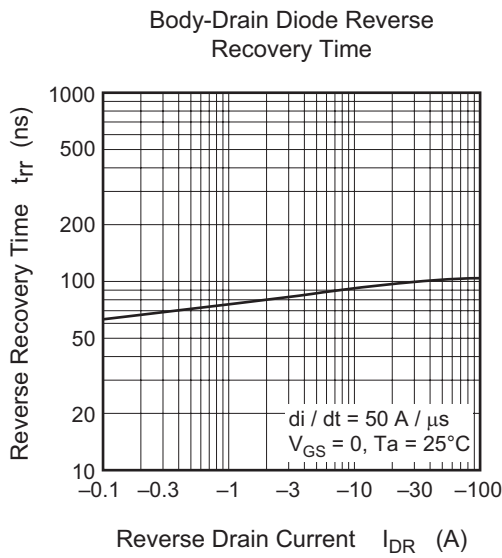
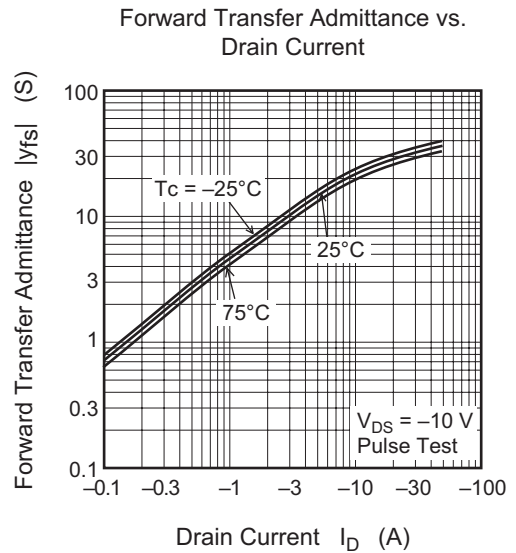
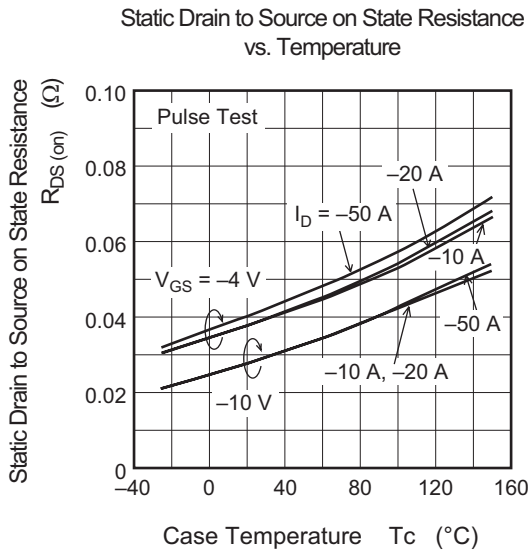
(Ta = 25°C)

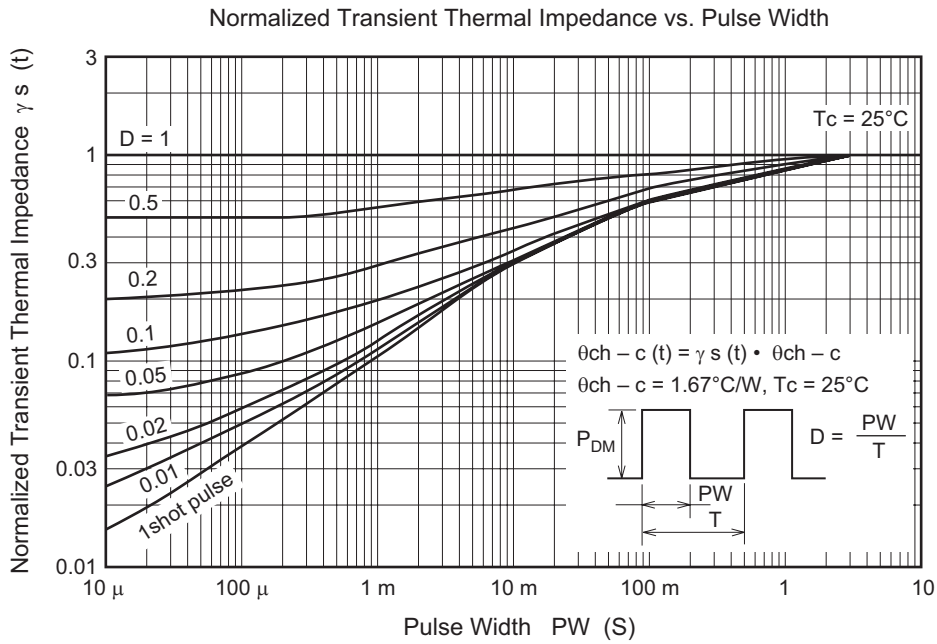
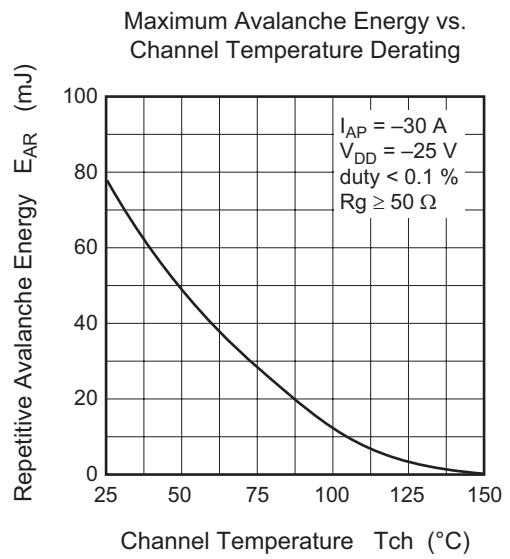
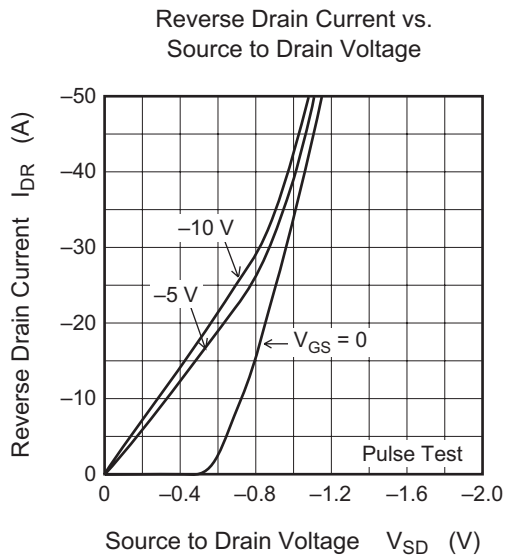
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-1.0	—	-2.0	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	0.028	0.037	Ω	I _D = -15 A, V _{GS} = -10 V ^{Note 4}
	R _{DS (on)}	—	0.038	0.055	Ω	I _D = -15 A, V _{GS} = -4 V ^{Note 4}
Forward transfer admittance	y _{fs}	15	25	—	S	I _D = -15 A, V _{DS} = -10 V ^{Note 4}
Input capacitance	C _{iss}	—	2500	—	pF	V _{DS} = -10 V
Output capacitance	C _{oss}	—	1300	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	300	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	25	—	ns	V _{GS} = -10 V
Rise time	t _r	—	150	—	ns	I _D = -15 A
Turn-off delay time	t _{d (off)}	—	350	—	ns	R _L = 2 Ω
Fall time	t _f	—	220	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-0.95	—	V	I _F = -30 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	100	—	ns	I _F = -30 A, V _{GS} = 0 di _F /dt = 50 A/μs

- Note: 4. Pulse test

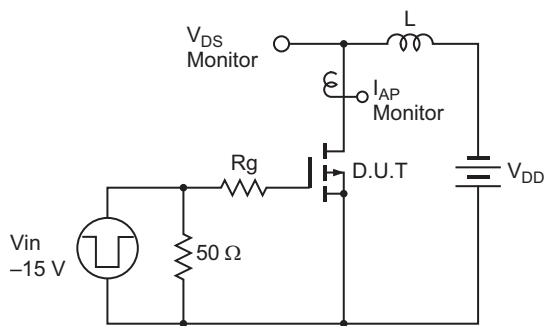
Main Characteristics





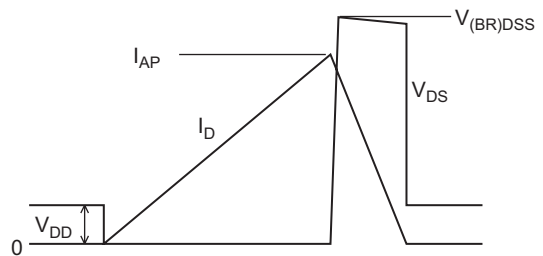


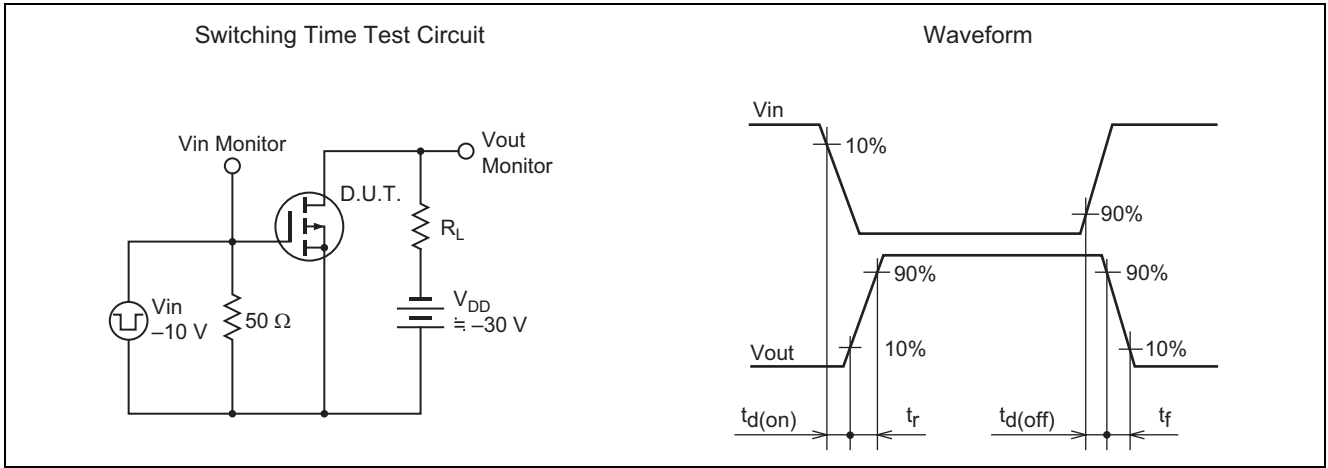
Avalanche Test Circuit



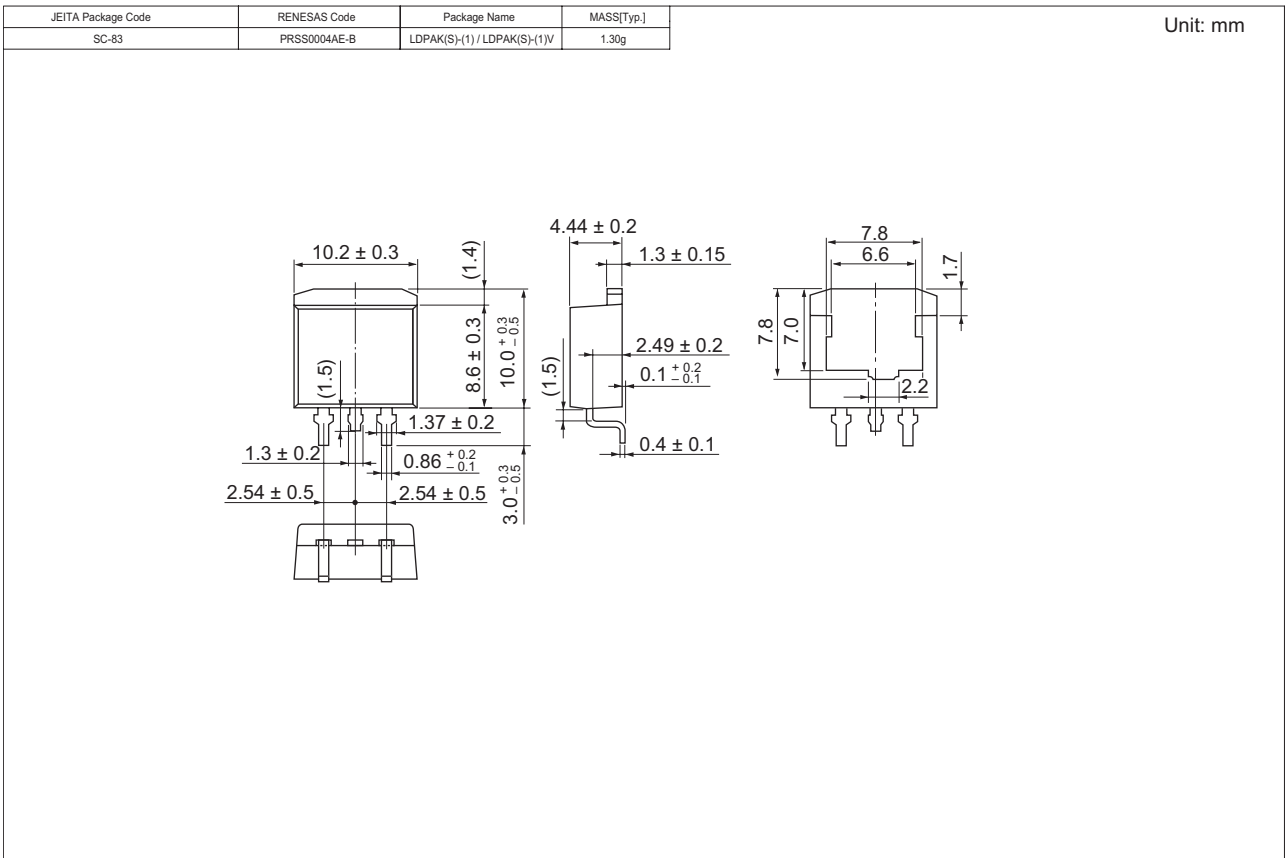
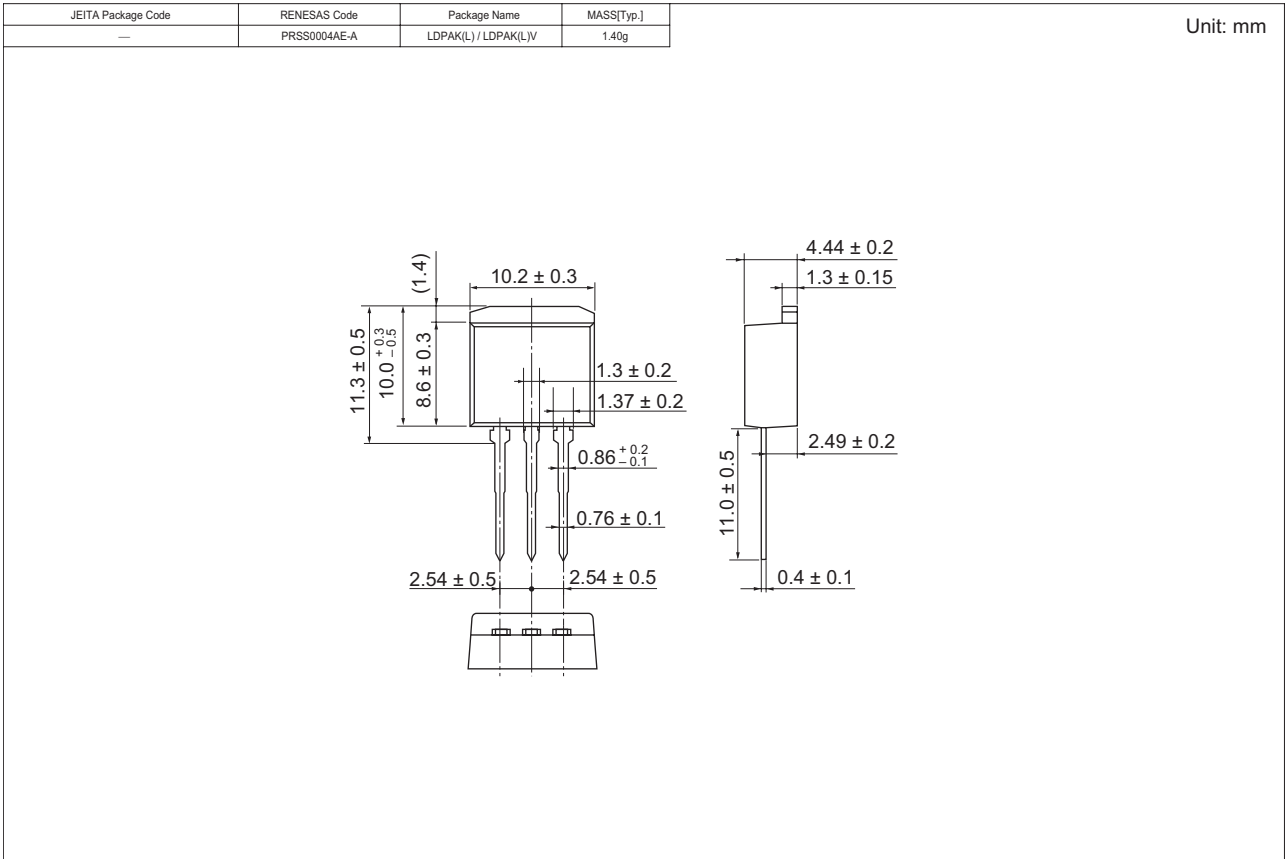
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ553L-E	500 pcs	Box (Sack)
2SJ553STL-E	1000 pcs	Taping

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