PI2122
Cool-ORing Series

12Amp Active ORing Solution With Load Disconnect

Description

The Cool-ORing PI2122 is a complete full-function Active ORing solution with a high-speed ORing MOSFET controller and a very low on-state resistance Dual MOSFETs designed for use in redundant power system architectures. The PI2122 Cool-ORing solution is offered in an extremely small, thermally enhanced LGA package and can be used in low voltage (≤ 5Vbus) high side Active ORing applications. The PI2122 enables extremely low power loss with fast dynamic response to fault conditions, critical for high availability systems. The PI2122 provide true bi-directional switch capabilities to protect against both power source and load fault conditions.

A load short circuit detection feature allows user definition of a short condition enabling minimum duty cycle into a short. The PI2122 has the added benefit of being able to protect against output load fault conditions that may induce excessive forward current and device over-temperature by turning off the back-to-back MOSFETs with an auto-retry programmable off-time. The back-to-back MOSFETs drain-to-drain voltage is monitored to detect normal forward, excessive forward, light load and reverse current flow. The status is reported via an active low fault flag output. A temperature sensing function turns off the MOSFETs and indicates a fault if the controller junction temperature exceeds 145°C.

Features

- Integrated High Performance 12A, 6mΩ back-to-back MOSFET
- Very-small, high density fully-optimized solution providing simple PCB layout.
- Fast Dynamic Response, with 140ns reverse & 170ns forward over-current turn-off delay time
- Accurate sensing capability to indicate system fault conditions
- Programmable under & over-voltage functions
- Over temperature shutdown
- Programmable over-current off time
- Programmable short circuit load detection
- Active low fault flag output

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- High-side Active ORing
- High current Active ORing (≤ 5Vbus)
- MicroTCA

Package

- 5mm x 7mm 17-pin Thermally Enhanced LGA Package

Typical Application:

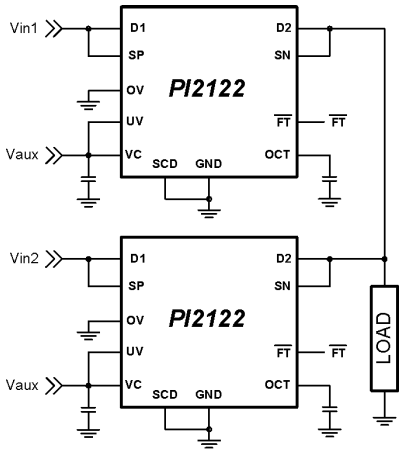


Figure 1: ***PI2122*** High Side Active ORing

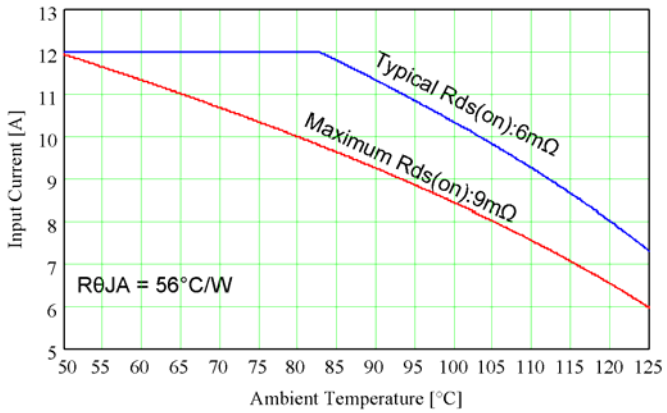
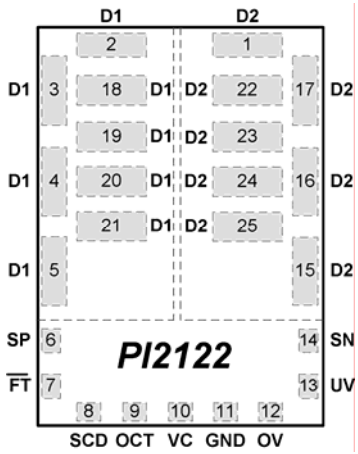


Figure 1: PI2122 input current de-rating based on

Pin Description

Pin Number	Pin Name	Description
1, 15, 16, 17, 22,23, 24, 25	**D2**	**Drain 2-** Drain 2 of the internal Dual N-channel MOSFETs, connect to the output load.
2, 3, 4, 5, 18,19,20, 21	**D1**	**Drain 1-** Drain 1 of the internal Dual N-channel MOSFETs, connect to the input voltage.
6	**SP**	**Positive Sense Input & Clamp:** Connect SP pin to the D1 pin. The polarity and magnitude of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFETs.
7	$\overline{FT}$	**Fault State Output:** This open collector output pulls low after the 40usec fault timer delay when a fault condition occurs. Fault logic inputs are VC Under-Voltage, input Under-Voltage, input Over-Voltage, Forward Over-Current, Reverse Current, Low Forward Current (or shorted switches) and Over-Temperature. Leave this pin open if unused.
8	**SCD**	**Short Circuit Detect Input:** This input pin is for setting the load voltage where a short circuit level is defined and detected. To enable slow MOSFET turn-on mode, connect SCD to VC. Connect to load point for minimum threshold (0.335V) or use resistor divider to increase threshold. Grounding pin enables the fast MOSFET turn on mode.
9	**OCT**	**Over Current Duty Cycle Input:** Connecting a capacitor (≤ 20nF) sets the gate off time once an over-current condition is detected. No capacitor on this pin will result in minimum off time; 40µs. Pulling this input low will disable Gate drive.
10	**VC**	**Controller Input Bias:** Provides power to the controller. Connect a 1µF capacitor between VC pin and ground. For high voltage applications connect a shunt resistor between VC and the input supply. Voltage on this pin is regulated to 15.5V in high voltage applications.
11	**GND**	**Ground:** This pin is ground for the control circuitry.
12	**OV**	**Input Over Voltage Input:** The OV pin detects when the input is greater than the Over-Voltage threshold resulting in a low Fault pin. OV "AND" a Forward Current condition turns the MOSFETs off. The input voltage OV threshold is programmable through an external resistor divider. Connect OV to GND to disable this function.
13	**UV**	**Input Under Voltage Input:** The UV pin detects when the input is less than the Under-Voltage threshold resulting in a low Fault pin. The input voltage UV threshold is programmable through an external resistor divider. During an Under-Voltage fault, the Gate is pulled low. Connect UV to VC to disable this function.
14	**SN**	**Negative Sense Input & Clamp-** Connect SN to D2 pin. The polarity and magnitude of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFETs.

Package Pin-out



17 Pin LGA (5mm x 7mm)
Top view

Absolute Maximum Ratings

D1 to D2 (V_{D1-D2}), D1 or D2 to GND	7V
Drain current (I_D) continuous	12A,
Drain current (I_D) pulsed (100µs)	60A
Thermal Resistance $\mathbf{R_{\theta JA}}$ (3)	56°C/W
VC	-0.3 to 17.3V/40mA
SP, SN, OV, OCT	-0.3 to 8.0V/ 10mA
UV, SCD, $\overline{FT}$	-0.3 to 17.3V/ 10mA
GND	-0.3V/ 5A peak
Storage Temperature	-65 °C to 150 °C
Operating Junction Temperature	-40°C to Thermal shutdown
Lead Temperature (Soldering, 20 sec)	250°C
ESD Rating (In accordance with JEDEC JESD 51-5)	2kV HBM

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{OCT} = 2nF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VC Supply						
Operating Supply Range(4)	V_{VC-GND}	4.5		13.2	V	No VC Limiting Resistors
Quiescent Current	I_{VC}		3.7	4.2	mA	Normal Operating Conditions No Faults
Clamp Voltage	V_{VC-CLM}	15	15.5	16	V	I_{VC}=10mA
VC Clamp Shunt Resistance	R_{VC}			7.5	Ω	Delta I_{VC}=10mA
VC Under-voltage Rising Threshold	V_{VCUVR}		4.3	4.5	V	
VC Under-voltage Falling Threshold	V_{VCUVF}	4.0	4.15		V	
VC Under-voltage Hysteresis	V_{VCUVHS}		150		mV	
Internal Dual N-Channel MOSFETs						
D1 to D2 Breakdown Voltage	V_{D1-D2}	6			V	In off state I=10uA; Tj=25°C; Figure 12, page 11
D1 to GND or D2 to GND		6				In OFF state I=10uA; Tj=25°C
Drain Current Continuous	I_{D1-D2}			12	A	In ON state; Tj=25°C
D1 to D2 On Resistance	R_{DSon}		6	9	mΩ	In on state, I_D=10A; Tj=25°C VC-V(D2) ≥ 4.0V
FAULT						
Under-Voltage Rising Threshold	V_{UVR}		500	540	mV	
Under-Voltage Falling Threshold	V_{UVF}	440	475		mV	
Under-Voltage Threshold Hysteresis	V_{UVHS}		25		mV	
Under-voltage Bias Current	I_{UV}	-1		1	µA	
Over-voltage Rising Threshold	V_{OVR}		500	540	mV	
Over-voltage Falling Threshold	V_{OVF}	440	475		mV	

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{OCT} = 2nF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
FAULT Continued						
Over-voltage Threshold Hysteresis	V_{OV-HS}		25		mV	
Over-voltage Bias Current	I_{OV}	-1		1	µA	
Fault Output Low Voltage	V_{FTL}		200	500	mV	I_{FT}=2mA, VC>4.5V
Fault Output High Leakage Current	I_{FT-LC}			10	µA	V_{FT}=14V
Fault Delay Time	t_{FT-DEL}	20	40	60	µs	Includes output glitch filter
Over Temperature Fault (1)	T_{FT}		145		°C	
Over Temperature Fault Hysteresis(1)	T_{FT-HS}		-10		°C	
DIFFERENTIAL AMPLIFIER AND COMPARATORS						
Common mode input voltage	V_{CM}	-0.1		5.5	V	V_{CM} =SP & SN w/respect to Gnd
VC to SN differential(1)	V_{VC-SN}	3.5			V	
Differential operating Input Voltage	V_{SP-SN}	-50		125	mV	SP-SN
SP Input Bias Current	I_{SP}		3.5		µA	V_{CM} =1.25V
SN Input Bias Current	I_{SN}		-37		µA	V_{CM} =1.25V
SN (SP) Voltage	V_{SN}			5.5	V	SP=0V (SN=0)
Reverse Comparator Off Threshold	V_{RVS-TH}	-10	-6	-2	mV	V_{CM} =3.3V
Reverse Comparator Hysteresis	V_{RVS-HS}	2	3	5	mV	V_{CM} =3.3V
Reverse Turn-off Delay	$t_{F\&RDLY}$		140	180	ns	V_{SP-SN} = ± 50mV step
Forward Comparator On Threshold	V_{FWD-TH}	2	5	9	mV	V_{CM} =3.3V
Forward Comparator Hysteresis	V_{FWD-HS}	-5	-3	-2	mV	V_{CM} =3.3V
Forward Over Current Comparator Threshold	V_{OC-TH}	83	90	97	mV	V_{CM} =3.3V
Forward Over Current Comparator Hysteresis	V_{OC-HS}	-8	-6	-4	mV	V_{CM} =3.3V
Forward Over Current to Turn-off Delay	$t_{FOC-DLY}$		170	200	ns	V_{SP-SN} = ± 50mV step
Over Current Timer: OCT						
OCT Charging Source Current	I_{SL}		-10		µA	V_{OCT} = 1.25V
OCT Clamp Voltage	V_{OCT-CL}	2.0	3.0	4.2	V	No Fault
OCT Threshold Voltage High	V_{OCT-Hi}		1.75		V	SP=3.3V, SN=0V
OCT Threshold Voltage Low	V_{OCT-Lo}		0.875		V	SP=3.3V, SN=0V
OCT OFF Time	$T_{OCT-OFF}$		350		µs	FOC fault condition
OCT MOSFET Disable	V_{OCT-Lo}			500	mV	I_{OCT} = -100uA
OCT Discharge Current	I_{OCTSK}	5	10		mA	V_{OCT} =2.25V SP-SN=100mV

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{OCT} = 2nF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
SCD						
SCD bias current	I_{scd}	-1		1	µA	V_{SCD}=0V
SCD threshold voltage high	V_{ThSCDR}	300	340	380	mV	V_{SP-SN}=20mV
SCD threshold voltage low	V_{ThSCDF}		310		mV	
SCD Hysteresis	V_{ThSCDR} - V_{ThSCDF}	25	50	75	mV	V_{SP-SN}=20mV

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Thermal resistance characterized on PI2122-EVAL1 evaluation board with 0 LFM airflow.

Note 4: Refer to the *Auxiliary Power Supply* section in the *Application Information* section for details on the VC requirement to fully enhance the internal MOSFET.

Functional Description:

The PI2122 integrated Cool-ORing product takes advantage of two different technologies combining 2 3mΩ on-state resistance (Rds(on)) N-channel MOSFETs with high density control circuitry. The product can function as an ideal ORing diode in the high-side of a redundant power system and a load disconnect switch, significantly reducing power dissipation and eliminating the need for heatsinking.

The PI2122 has two internal MOSFETs in a back-to-back configuration that has the ability to block current in both directions. This configuration protects the load and the input source, by turning off the MOSFETs, during Reverse Current, Forward Over-Current, Under-Voltage, Over-Voltage and Over-Temperature faults.

Differential Amplifier:

The PI2122 integrates a high-speed low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high resolution. The amplifier output is connected to three comparators: Reverse comparator, Forward comparator, and Forward over-current comparator.

Reverse Current Comparator: RVS

The reverse current comparator provides the most critical function in the controller, detecting negative voltage caused by reverse current. When the SN pin is 6mV higher than the SP pin, the reverse comparator will turn off the MOSFETs in typically 140ns.

The reverse comparator has typically 3mV of hysteresis referenced to SP-SN.

Forward Current Comparator: FWD

The FWD comparator detects when a forward current condition exists and SP is 5mV (typical) positive with respect to SN. When SP-SN is less than 5mV it will indicate a fault condition on the $\overline{FT}$ pin during a light load while maintaining gate drive to the MOSFETs. The PI2122 will initiate a gate shutdown if the Forward "AND" the over-voltage (OV) condition are true.

Over-Current Timer: OCT

OCT off-time is set by the capacitor value connected to this pin as shown in Figure 4.

The OCT block will control the off-time of the MOSFETs after a FOC fault condition has occurred. The equivalent block diagram is shown in Figure 3. As the Set input at the OCT timer goes high, $\overline{Out}$ will go low, pulling MOSFETs Gate low. At the same time a one shot of 40µs discharges the OCT capacitor; then begins charging the capacitor again. $\overline{Out}$ and MOSFETs Gate stay low until the OCT pin reaches the OCT high threshold (V_{OCT-Hi}), then $\overline{Out}$ goes high and the MOSFETs starts to turn on. As soon as the MOSFETs reaches sufficient gate voltage for Rds(on) the Clamp Detector asserts and turns MOSFETs on. If $\overline{FOC}$ is still low then the MOSFETs Gate will be pulled low and will start a new off-time cycle of the Over-Current timer.

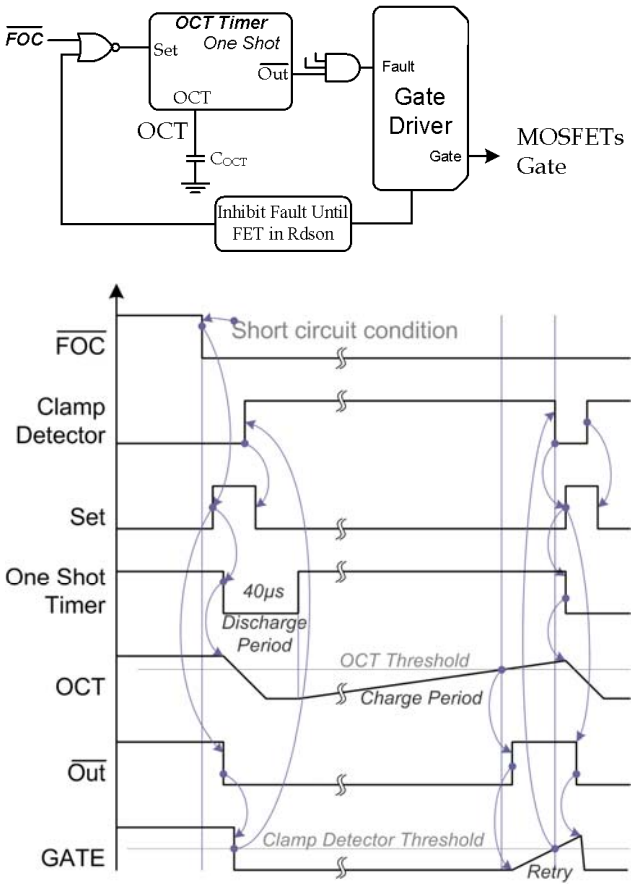


Figure 3: **OCT block and timing diagram**

Short Circuit Detect: SCD

This comparator block input can be connected to the load directly or programmed to a higher voltage with a resistor divider. The function allows the user to define the (Hard Short) voltage level expected if a non-ideal short circuit occurs at the load. To prevent damage of the MOSFETs under this condition (V_{SCD}<335mV) the gate charge current is increased by a factor of approximately 5 times resulting in a duty cycle that is approximately 5 times lower, as determined by the OCT function. This feature enables distinguishing between a faulted load versus powering capacitive and low resistive loads

without entering the OCT mode. The pin can be grounded to provide a low duty cycle mode or pulled to VC for lower gate current to drive highly capacitive loads with resulting higher duty cycle mode under the fault condition. In either case if the resulting temperature rise of the MOSFET and controller reach thermal shutdown the thermal time constant of the package will set a low frequency burst like duty cycle condition and protect the MOSFETs.

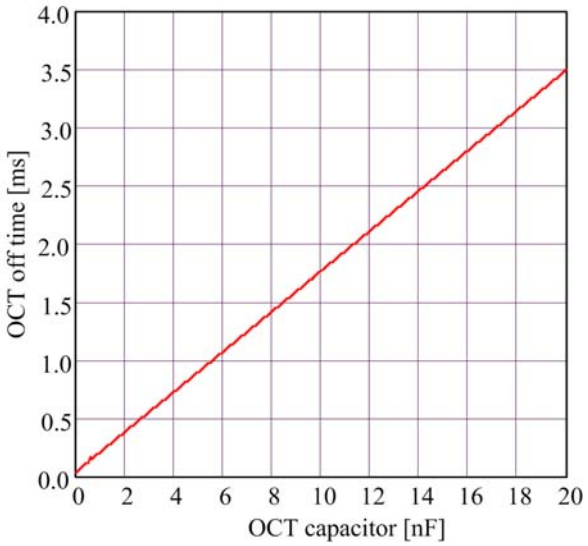


Figure 4: *OCT Off time vs. OCT capacitor value*

VC and Internal Voltage Regulator:
The PI2122 has a separate input (VC) that provides power to the control circuitry and the internal gate driver. An internal regulator clamps the VC voltage to 15.5V.

For high side applications, the VC input should be 4V above the bus voltage to properly enhance the internal N-channel MOSFET.

The internal regulator circuit has a comparator to monitor VC voltage and initiates a FAULT condition when VC is lower than the VC Under-Voltage Threshold.

UV:
The Under Voltage (UV) input trip point can be programmed through an external resistive divider to monitor the input voltage. When UV falls below the Under-Voltage Falling Threshold, UV comparator initiates a fault condition and pulls the FT pin low and turns off the MOSFETs.

OV:
The Overvoltage (OV) input trip point can be programmed through an external resistive divider to monitor the input voltage. The OV comparator initiates a fault condition and pulls the $\overline{FT}$ pin low when OV rises above the Overvoltage Rising Threshold. The PI2122 will turn the MOSFETs off if the OV and the Forward Current conditions are both true. The low resistance redundant paths of an Active ORing system tend to force all the input sources to the same voltage making it difficult to identify the noncompliant source. By ANDing OV with the Forward Current Threshold the noncompliant source is identified and disconnected from the system.

Over-Temperature Detection:

The internal Over-Temperature block monitors the junction temperature of the controller. The Over-Temperature threshold is set to 145°C with -10°C of hysteresis. When the controller temperature exceeds this threshold, the Over-Temperature circuit turns the MOSFETs off and initiates a fault condition and pulls the $\overline{FT}$ pin low. This function will protect the MOSFETs from thermal runaway conditions.

Fault:

The fault circuit output is an open collector with 40µs delay to prevent any false triggering. The $\overline{FT}$ pin will be pulled low when any of the following faults occurs:

- Reverse Current
- Forward Over-Current “AND” clamp detector is cleared
- Forward Low Current “AND” clamp detector is cleared
- Over Temperature
- Input Under-Voltage
- Input Over-Voltage “AND” nominal Forward Current
- VC pin Under-Voltage

The Forward Current fault condition occurs when the MOSFETs gates are high but are not conducting a significant level of forward current or may indicate the MOSFETs are shorted either internally or externally ($V_{D1\text{-}D2}$ < 5mV).

A gate voltage detector prevents FOC or FWD from initiating a fault when the MOSFET is in an OFF condition.
The gate to SN voltage has to reach sufficient voltage to establish the Rds(on) condition before these faults are detected.

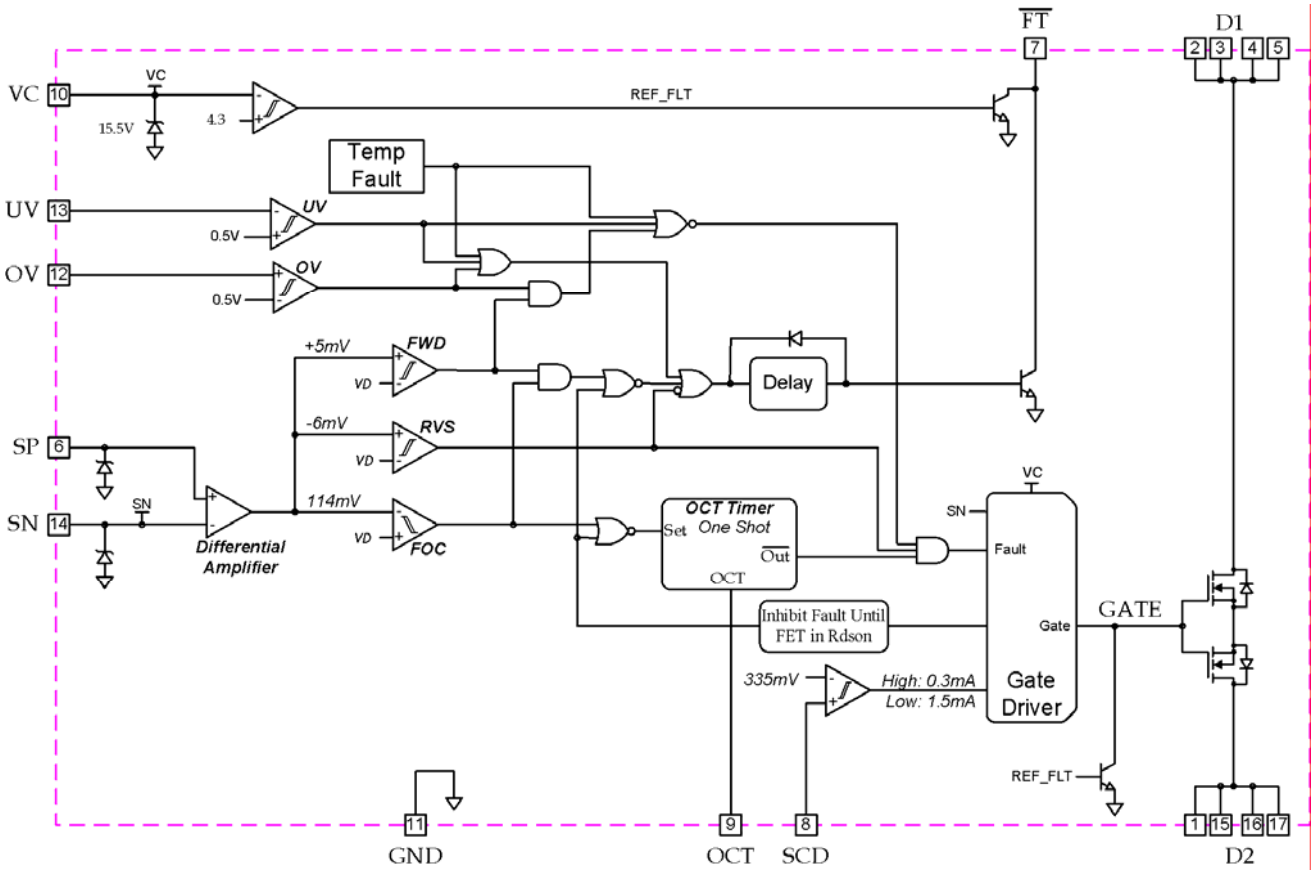


Figure 5: **PI2122** Functional Block Diagram

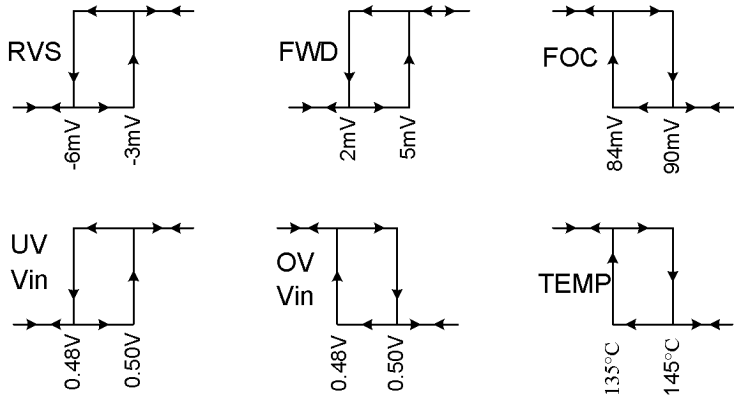


Figure 6: Typical comparators thresholds and hysteresis values.

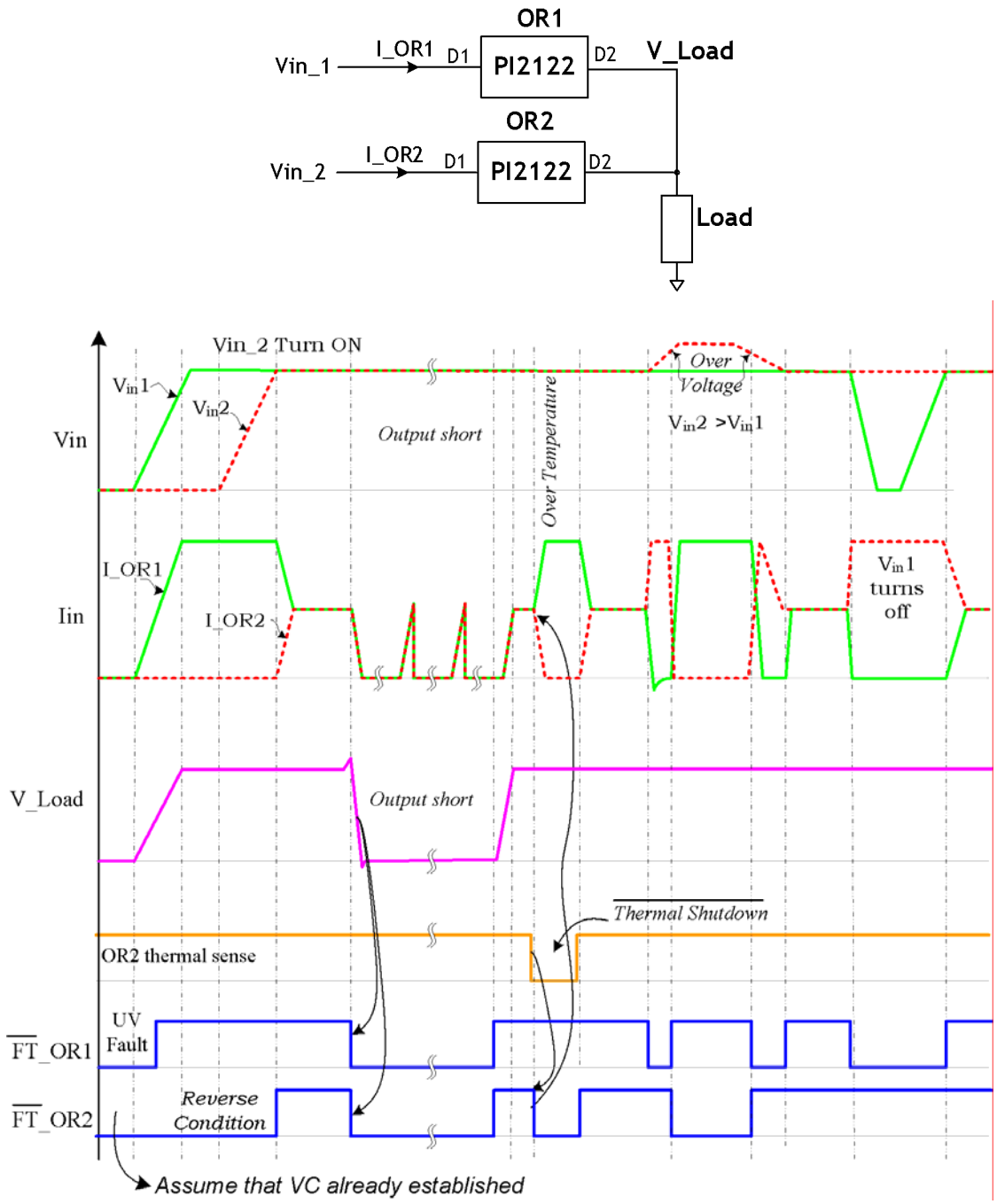


Figure 7: PI2122 Timing diagram for two ORing controllers application

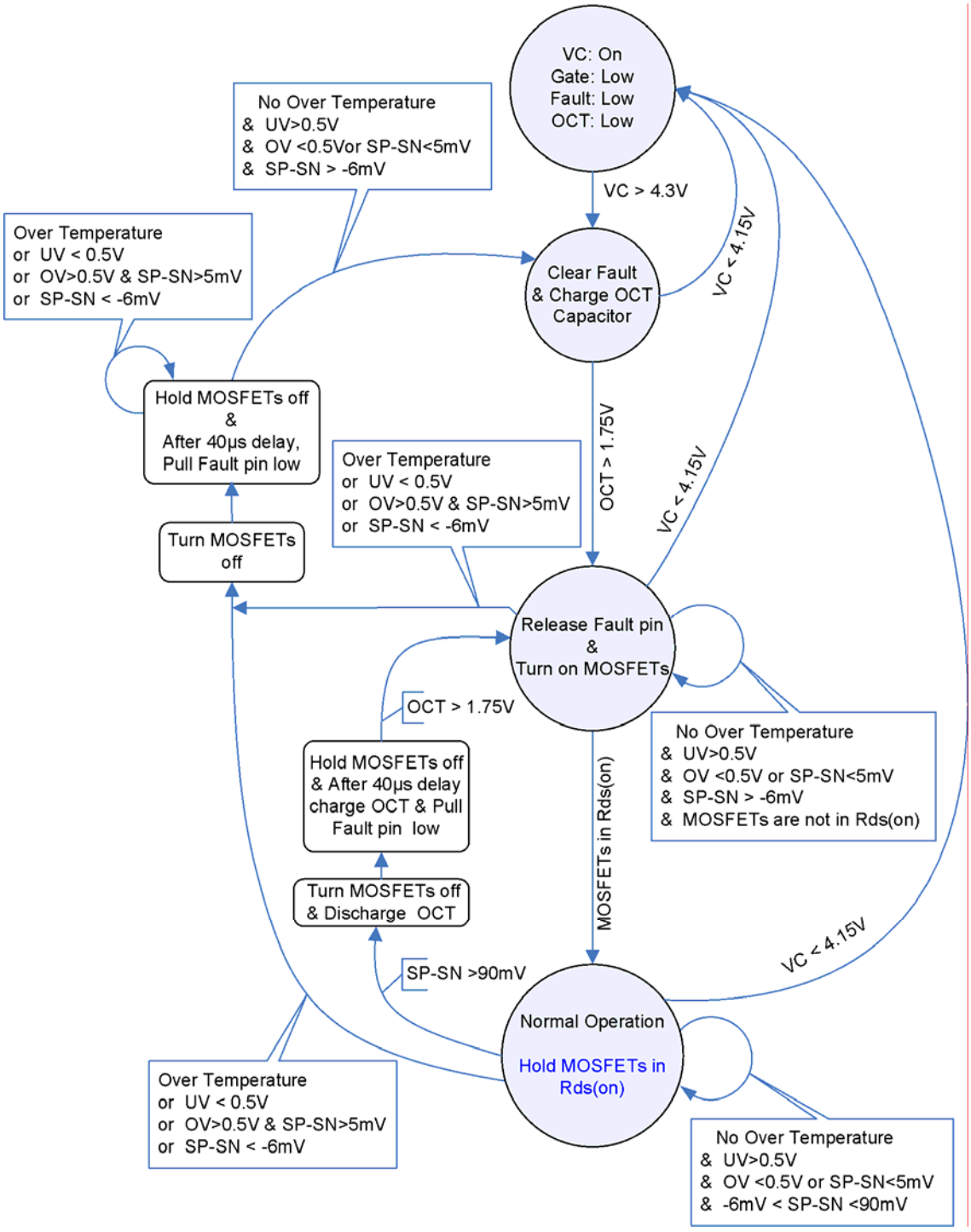


Figure 8: PI2122 State diagram.

Typical Characteristics:

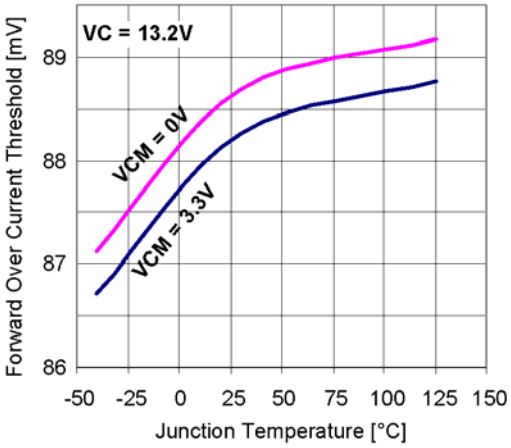


Figure 9: FOC comparator threshold vs. temperature.
VCM: *Common Mode Voltage*.

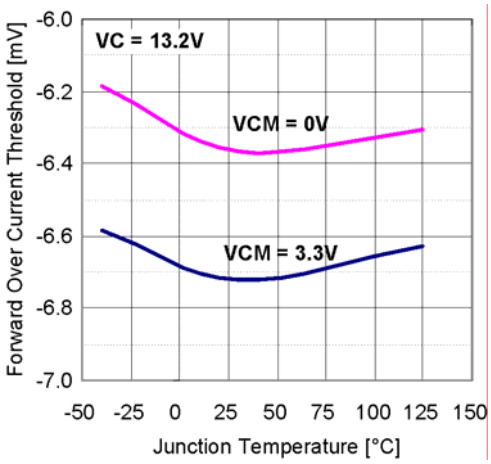


Figure 10: Reverse comparator threshold vs. temperature.
VCM: *Common Mode Voltage*.

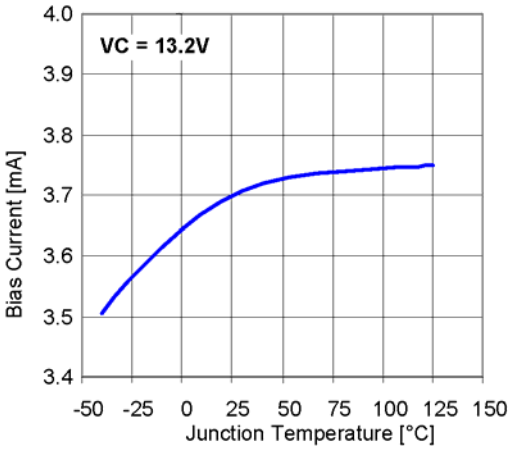


Figure 11: Controller bias current vs. temperature.

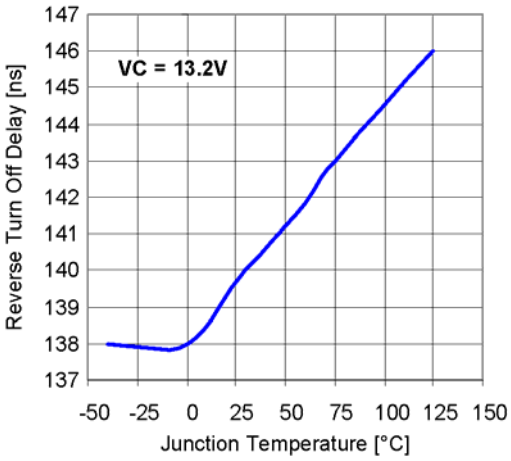


Figure 12: Reverse condition turn-off delay time vs. temperature.

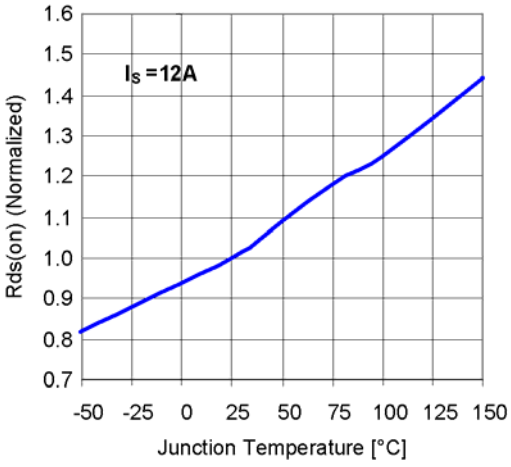


Figure 13: Internal MOSFETs on-state resistance vs. temperature.

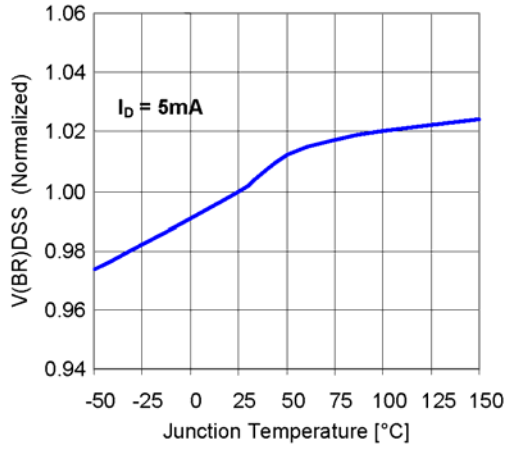


Figure 14: Internal MOSFETs drain to source breakdown voltage vs. temperature.

Thermal Characteristics:

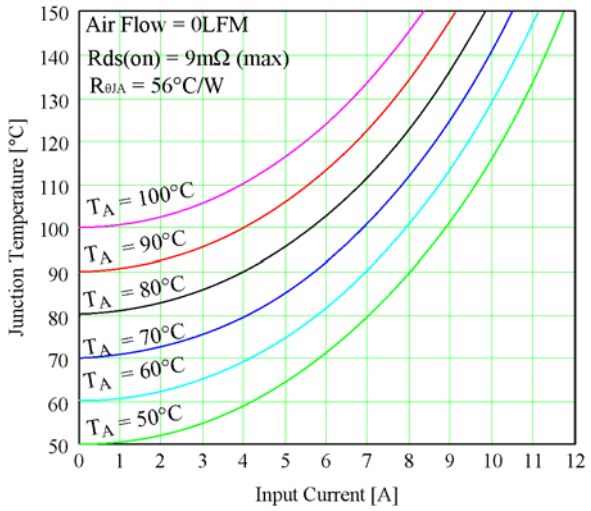


Figure 15: Junction Temperature vs. Input Current (0LFM)

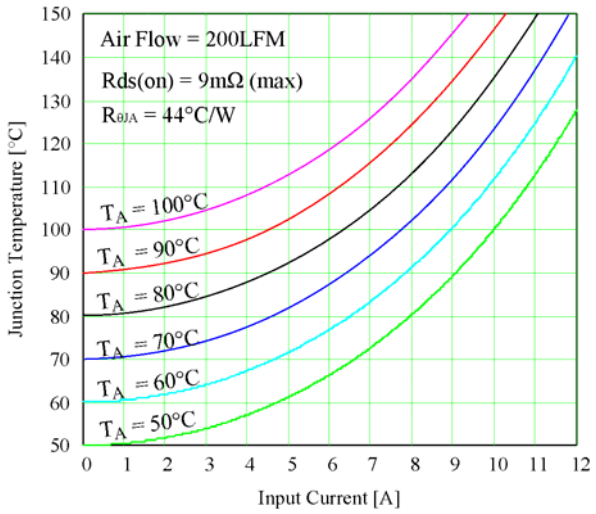


Figure 16: Junction Temperature vs. Input Current (200LFM)

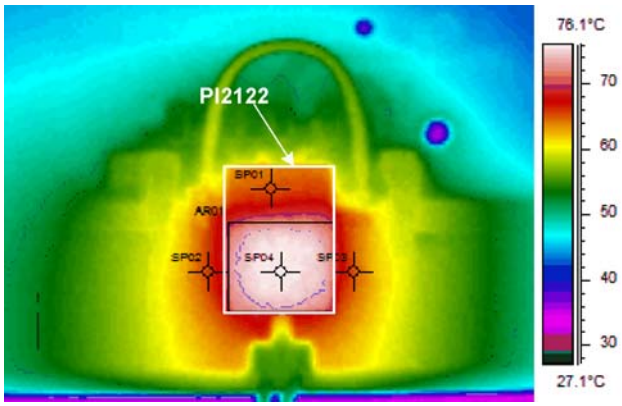


Figure 17: PI2122 mounted on PI2122-EVAL1 Thermal Image picture, Iout=12A, T_A=25°C, Air Flow=0LFM

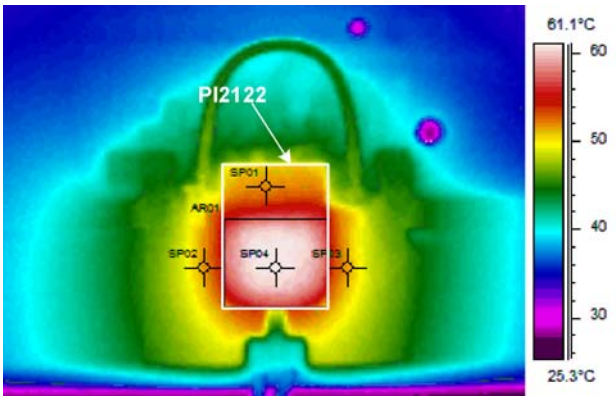


Figure 18: PI2122 mounted on PI2122-EVAL1 Thermal Image picture, Iout=12A, T_A=25°C, Air Flow=200LFM

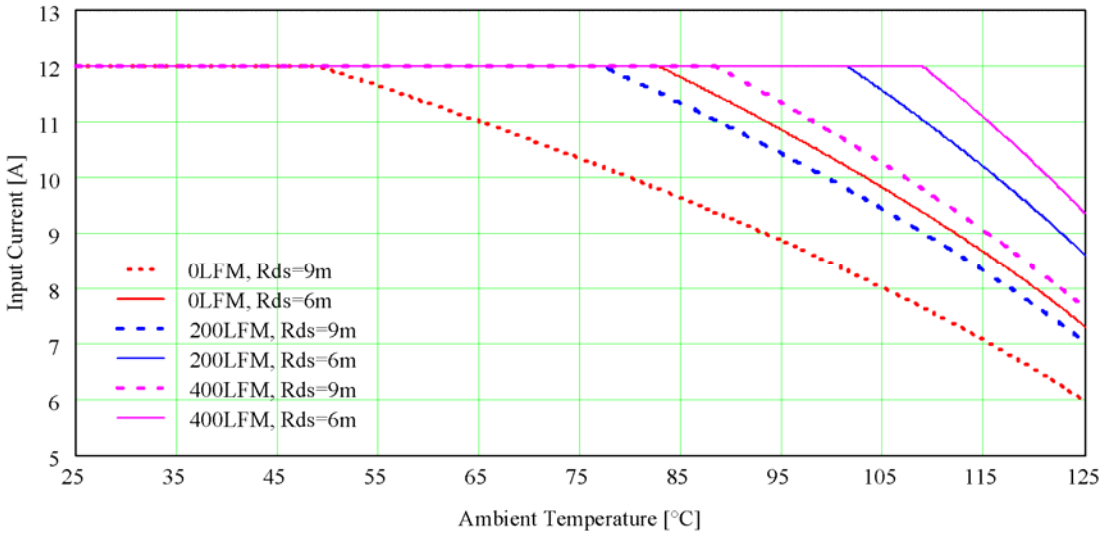


Figure 19: PI2122 input current de-rating based on maximum T_J=150°C vs. ambient temperature

Application Information:

The PI2122 is designed to replace ORing diodes and load disconnect switchs in high current redundant power architectures. Replacing a traditional diode with a PI2122 will result in significant power dissipation reduction as well as board space reduction, efficiency improvement, input power source and output protection plus additional protection features. This section describes in detail the procedure to follow when designing with the PI2122 Active ORing solution. A design example is presented for Active ORing with load disconnect.

Fault Indication:

$\overline{FT}$ output pin is an open collector and should be pulled up to the logic voltage or to the controller VC via a resistor (10KΩ)

Over-Current Timer: OCT

Connect a capacitor, in the range of 1nF to 20nF to set the off time after over-current shutdown (see Figure 4).

Short Circuit Detect: SCD

Connect SCD pin to VC to avoid high inrush current into a capacitive load, or connect SCD to GND pin for fast turn on. The internal MOSFETs gate drive current has two levels based on the SCD voltage level.

Auxiliary Power Supply (Vaux):

Vaux is an independent power source required to supply power to the VC input. The Vaux voltage should be 4V higher than Vin (redundant power source output voltage) to fully enhance the internal MOSFETs.

A bias resistor (Rbias) is required if the bias supply (Vaux) is higher than 15V. Rbias should be connected between the VC pin and Vaux to limit the current into the internal shunt regulator.

Minimize the resistor value for low Vaux voltage levels to avoid a voltage drop that may reduce the VC voltage lower than required to drive the gate of the internal MOSFETs.

Select the value of Rbias using the following equations:

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}}$$

Rbias maximum power dissipation:

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clamp})^2}{Rbias}$$

Where:

$Vaux_{\min}$: Vaux minimum voltage

$Vaux_{\max}$: Vaux maximum voltage

VC_{Clamp} : Controller clamp voltage, 15.5V

$IC_{\max}$: Controller maximum bias current, use 4.2mA

Example: Vaux 20V to 30V

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}} = \frac{20V - 15.5V}{4.2mA} = 1.07K\Omega$$

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clamp})^2}{Rbias} = \frac{(30V - 15.5V)^2}{1.07K\Omega} = 196mW$$

Internal N-Channel MOSFET BVdss:

In an application when the MOSFETs are turned off due to a fault, the series parasitic elements in the circuit may contribute to the MOSFET being exposed to a voltage higher than its voltage rating. It is critical to follow best layout practice to minimize parasitic inductance in the PCB layout especially in the high current path.

In Active ORing applications when one of the input power sources is shorted, a large reverse current is sourced from the circuit output through the MOSFETs. Depending on the output impedance of the system, the reverse current may reach over 60A in some conditions before the MOSFET is turned off. Such high current conditions will store energy even in a small parasitic element. For example: a 1nH parasitic inductance with 60A reverse current will generate 1.8μJ (½Li^2). When the MOSFETs are turned off, the stored energy will be released and produce a high negative voltage ringing at D1. At the same time the energy stored at D2 of the internal MOSFETs will be released and produce a voltage higher than the load voltage. This event will create a high voltage difference between the drain and source of the MOSFET. To reduce the magnitude of the ringing voltage, add a ceramic capacitor very close to D1 that can react to the voltage ringing frequency and another capacitor close to D2. Recommended values for the ceramic capacitors are 1μF; refer to C5 and C7 in Figure 24.

Note:

Since the two MOSFETs are connected in to back-to-back configuration, the maximum breakdown voltage is BVdss of one MOSFET plus one diode forward voltage.

OV and UV resistor selection:

The UV and OV comparator inputs are used to monitor the input voltage and will indicate a fault condition when this voltage is out of range. The UV and OV pins can be configured in two different ways, either with a divider on each pin, or with a three-resistor divider to the same node, enabling the

elimination of one resistor. Under-Voltage is monitored by the UV pin input and Over-Voltage is monitored with the OV pin input.

The Fault pin ($\overline{FT}$) will indicate a fault (active low) when the UV pin is below the threshold or when the OV pin is above the threshold. The UV and OV thresholds are 0.50V typical with 25mV hysteresis and their input current is less than ±1µA. It is important to consider the maximum current that will flow in the resistor divider and maximum error due to UV and OV input current. Set the resistor current to 100µA or higher to maintain 1% accuracy for UV and OV due to the bias current.

The three-resistor voltage divider configuration for both UV and OV to monitor the same voltage node is shown in Figure 20:

$$Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

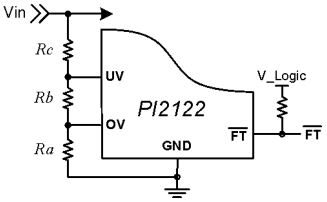


Figure 20: UV & OV three-resistor divider configuration.

$$Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

Set Ra value based on system allowable current I_{Ra} $Ra = \frac{V(OV_{TH})}{I_{Ra}}$

$$Rb = Ra\left(\frac{V(OV)}{V(UV)} - 1\right)$$

$$Rc = (Ra + Rb)\left(\frac{V(UV)}{V_{TH}} - 1\right)$$

Where:

$V(UV_{TH})$: UV threshold voltage

$V(OV_{TH})$: OV threshold voltage

$V(UV)$: UV voltage

I_{Ra} : Ra current.

Alternatively, a two-resistor voltage divider configuration can be used and is shown in (Figure 21).

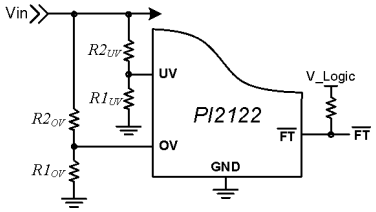


Figure 21: Two-resistor divider configuration

The UV resistor voltage divider can be obtained from the following equations:

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{UV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{UV} = R1_{UV}\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

Where:

$V(UV_{TH})$: UV threshold voltage

I_{RUV} : $R1_{UV}$ current

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{OV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{OV} = R1_{OV}\left(\frac{V(OV)}{V(OV_{TH})} - 1\right)$$

Where:

$V(OV_{TH})$: OV threshold voltage

I_{ROV} : $R1_{OV}$ current

Typical Application Example 1:

Requirement:
Redundant Bus Voltage = 5.0V
Load Current = 8A (assume through each redundant path)
Maximum Ambient Temperature = 70°C, no air flow
Auxiliary Voltage = 12V (10V to 14V)

Solution:
A single PI2122 for each redundant 5V power source should be used, configured as shown in the circuit schematic in Figure 22.

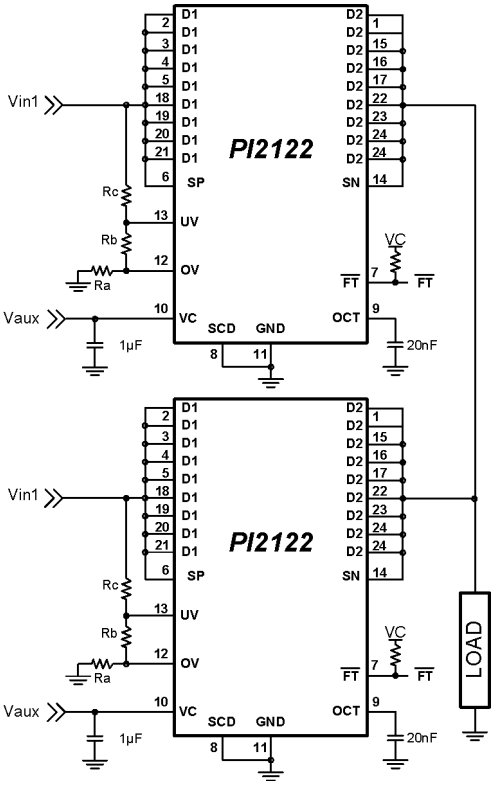


Figure 22: Two PI2122 in High Side ORing configuration

Vaux:

Since the Vaux voltage does not exceed the VC pin clamp voltage, connect the Vaux directly to the VC pin

SP and SN pins:

Connect each SP pin to the D1 pins and each SN pin to the D2 pins

$\overline{FT}$ **pin**:

Connect to the supervisor logic input and to the logic power supply via a 10KΩ resistor.

OCT pin:

Connect an 18nF capacitor between the OCT pin and the GND pin to achieve the maximum off time after a forward over-current condition occurs.

SCD pin:
Connect the SCD pin to the GND pin for fast MOSFET enhancement.

Program UV and OV to monitor input voltage:
Program UV at 4.6V and OV at 5.4V
Use the three-resistor divider configuration:

$$I_{Ra} = 200\mu A$$

$$Ra = \frac{500mV}{200\mu A} = 2.5k\Omega \text{ or } 2.49k\Omega \text{ 1\%}$$

$$Rb = 2.49k\Omega\left(\frac{5.4V}{4.6V} - 1\right) = 433\Omega \text{ or } 432\Omega \text{ 1\%}$$

$$Rc = (2.49k\Omega + 432\Omega)\left(\frac{4.6V}{500mV} - 1\right) = 23.96k\Omega$$

or 24.0kΩ 1%

Power Dissipation and Junction Temperature:
First use Figure 15 (Junction Temperature vs. Input Current) to find the final junction temperature for 8A load current at 70°C ambient temperature. In Figure 15 (illustrated in Figure 23) draw a vertical line from 8A to intersect the 70°C ambient temperature line. At the intersection draw a horizontal line towards the Y-axis (Junction Temperature). The Junction Temperature at full load current (8A) and 70°C ambient is 110°C, assuming the typical θ_{JA}=56°C/W.

Rds(on) is 9.0mΩ maximum at 25°C and will increase as the Junction temperature increases. From Figure 11, at 110°C Rds(on) will increase by ~29%, then

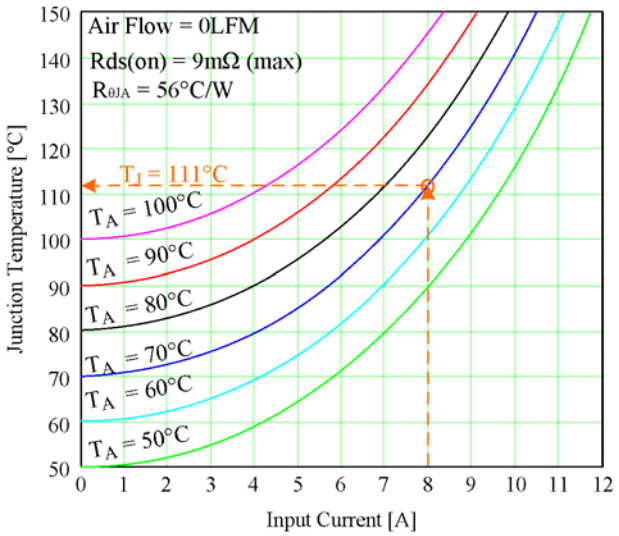


Figure 23: Example 1 final junction temperature at 8A/70°C T_A

$Rds(on) = 9m\Omega * 1.29 = 11.61m\Omega$ maximum at 111°C

Maximum power dissipation is:

$$Pd_{\max} = Iin^2 * Rds(on) = (8A)^2 * 11.61m\Omega = 743mW$$

Recalculate T_J:w

$$T_{J\max} = 70°C + \left(\frac{56°C}{W} * (8A)^2 * 11.61m\Omega\right) = 111.6°C$$

Reverse Current Threshold:

The following procedure demonstrates how to calculate the minimum required reverse current in the internal MOSFETs to generate a reverse fault condition and turn off the internal Misfits at room temperature (25°C) and typical Rds(on):

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{6m\Omega} = -1.0A$$

Forward Over-Current threshold\:

The following procedure demonstrates how to calculate typical forward current in the internal MOSFETs to generate a forward over-current fault condition and turn off the internal MOSFETs at room temperature (25°C) and typical Rds(on):

$$I_{FOC} = \frac{V_{FOC-TH}}{Rds(on)} = \frac{90mV}{6m\Omega} = 15A$$

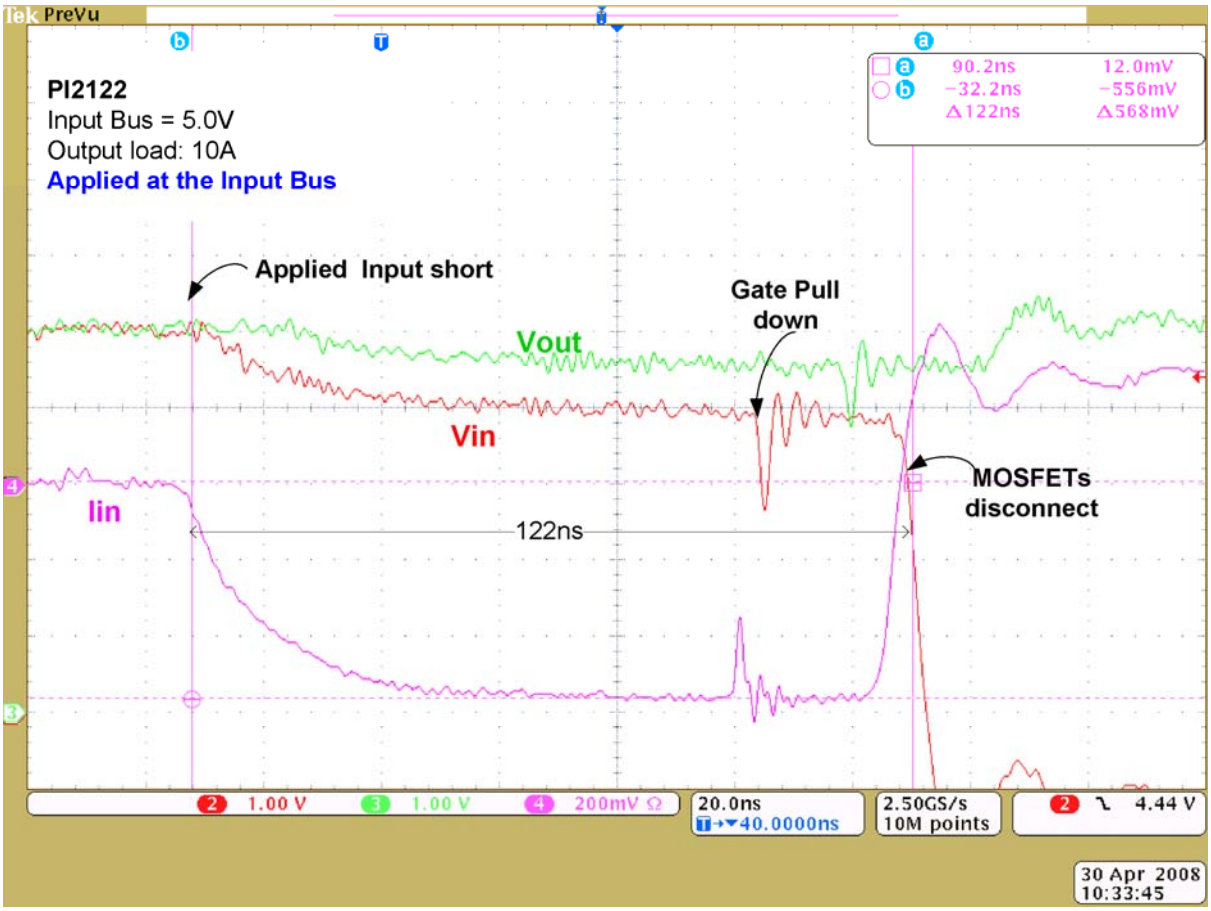


Figure 24: Plot of PI2122 response time to reverse current detection (Example 1, Figure 22)

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for the PI2122 is shown in Figure 25:

- Make sure to have a solid ground (return) plane to reduce circuit parasitic.
- Connect all D1 pads together with a wide trace to reduce trace parasitics to accommodate the high current input, and also connect all D2 pads together with a wide trace to accommodate the high current output.
- Connect the SP pin to the D1 pins and connect the SN pin to D2 pins.
- Use 1oz of copper or thicker if possible to reduce trace resistance and reduce power dissipation.
- The VC bypass capacitor should be located as close as possible to the VC and GND pins. Place the PI2122 and bypass capacitor on the same layer of the board. The VC pin and C_{VC} (shown as C2 in Figure 25) PCB trace should not contain any vias or connect to the ground plane close to the GND pin.
- Keep the power source very close to the D1 input pins, any parasitic inductance in the trace connecting the power source and D1 pins will have inductive kick when there is high current dv/dt in the trace when the MOSFETs turn off due to reverse current fault conditions. The inductive kick will produce a high voltage across the MOSFET. If it is not possible to connect the power source and D1 pins with a very short trace or common point, connect a capacitor (shown as C5 in figure 25), recommended value 1µF, close to the D1 pins and return (ground). Also for the same reason use C7 in figure 25 at the output.

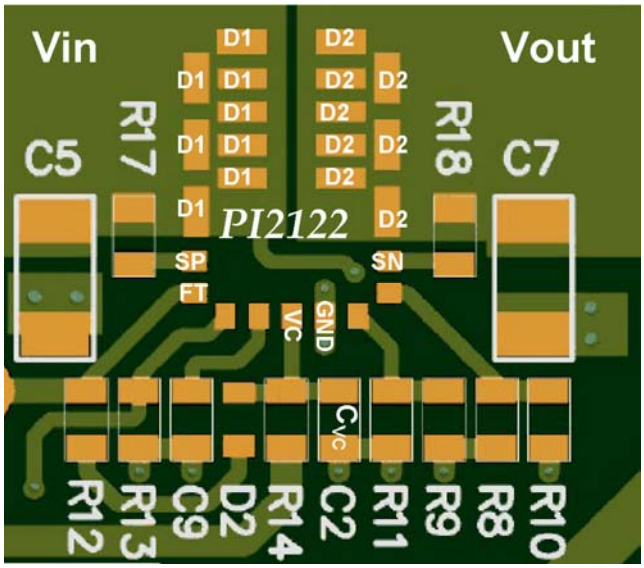


Figure 25: PI2122 layout recommendation

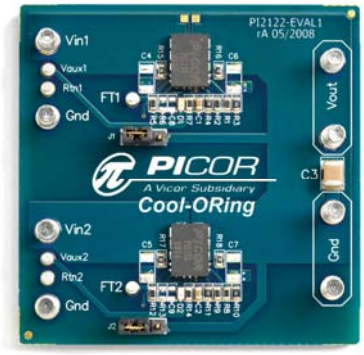
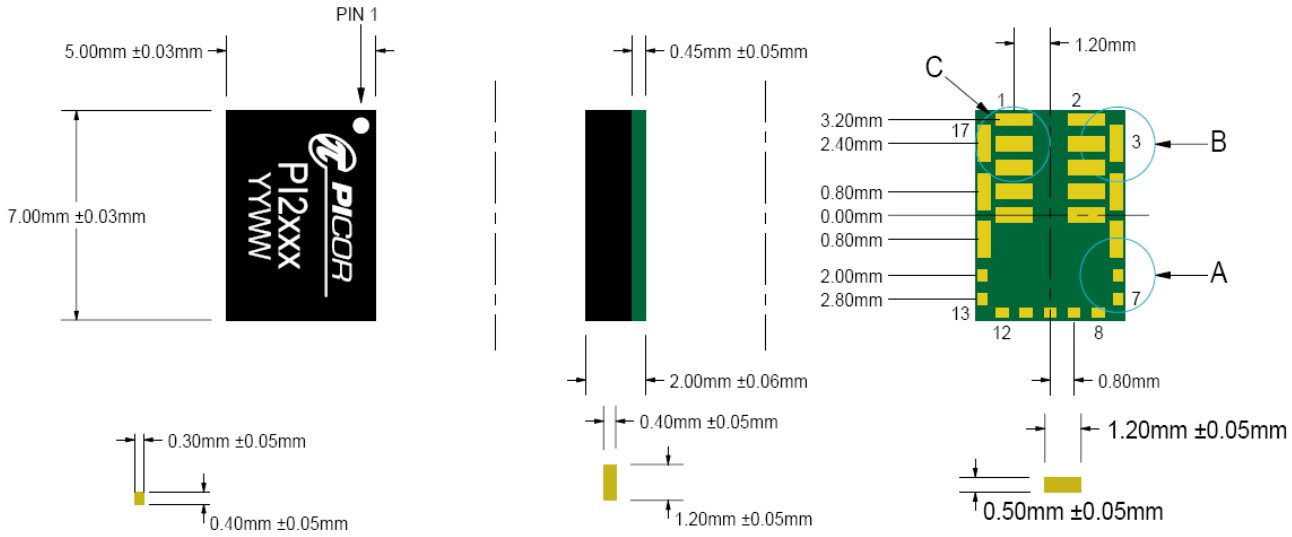


Figure 26: PI2122 Mounted on PI2122-EVAL1
Please visit www.picorpower.com for information on PI2122-EVAL1

Package Drawing



A: I/O Pads (Pins 6 - 14)
Copper Defined

B: Power Pads (Pins 1 - 5, 15 - 17)
Soldermask Defined

C: Internal Power Pads
Soldermask Defined (8 Places)

Thermal Resistance Ratings			
Parameter	**Symbol**	**Typical**	**Unit**
Maximum Junction-to-Ambient (2)	θ_{JA}	56	°C/W
Maximum Junction-to-PCB	θ_{JC}	14	°C/W

Note 2: In accordance with JEDEC JESD 51-5

Ordering Information

Part Number	Package	Temperature range	Transport Media
PI2122-00-LGIZ	5x7mm 17-pin LGA	-40°C to 125°C	T&R

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