

**Versatile EMI Reduction IC**

**Features**

- FCC approved method of EMI attenuation
- Provides up to 20dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- Optimized for 25MHz to 60MHz input frequency range
- Internal loop filter minimizes external components and board space
- 4 selectable spread ranges
- SSON control pin for spread spectrum enable and disable options
- Low Cycle-to-cycle jitter
- 3.3V or 5.0V operating voltage
- Low power CMOS design
- Available in 8 pin SOIC and TSSOP Packages

which provides system wide reduction of EMI of all clock dependent signals. The P2041A allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The P2041A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

The P2041A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics. This result in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called “spread spectrum clock generation”.

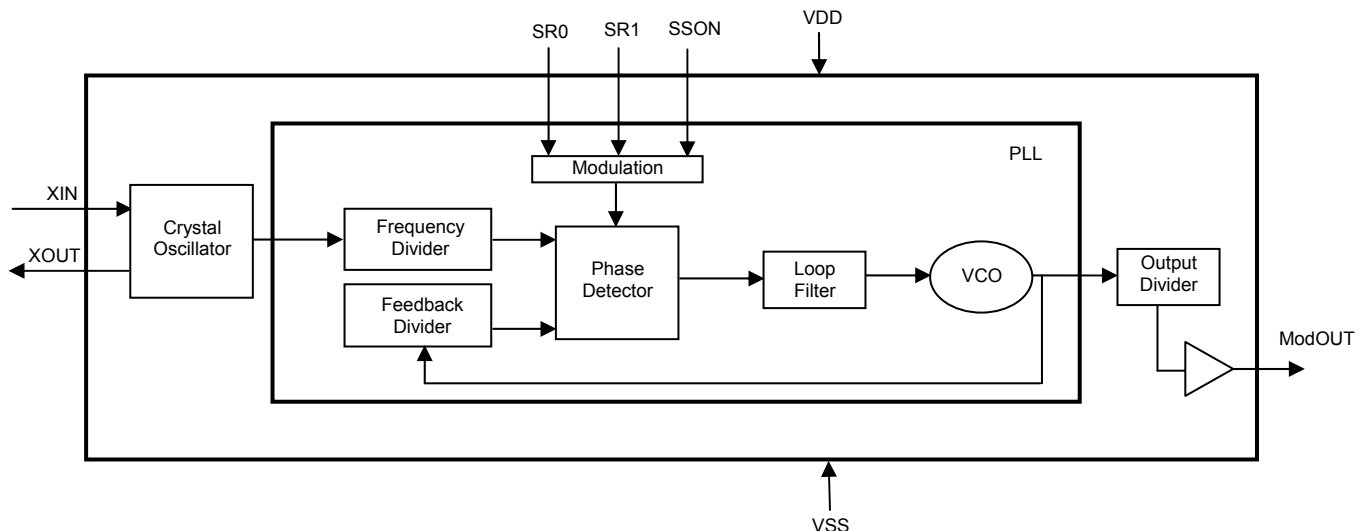
**Product Description**

The P2041A is a selectable spread spectrum frequency modulator designed specifically for PC peripheral and embedded controller markets. The P2041A reduces electromagnetic interference (EMI) at the clock source

**Applications**

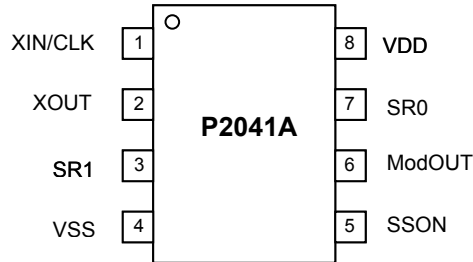
The P2041A is targeted towards the embedded controller market and PC peripheral markets including scanners, MFP’s, printers, PDA, IA , and GPS devices.

**Block Diagram**



rev 0.2

Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLK	I	Connect to crystal or externally generated clock signal.
2	XOUT	I	Connect to crystal. No connect if externally generated clock signal is used.
3	SR1	I	Digital logic input used to select Spreading Range (see Table 1). This pin has an internal pull-up resistor.
4	VSS	P	Ground Connection. Connect to system ground.
5	SSON	I	Digital logic input used to enable Spread Spectrum function (Active Low). Spread Spectrum function enable when low. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread Spectrum Clock Output.
7	SR0	I	Digital logic input used to select Spreading Range (see Table 1). This pin has an internal pull-up resistor.
8	VDD	P	Connect to +3.3V or +5.0V

Spread Range Selection

SR1	SR0	Spreading Range	Modulation rate
0	0	+/- 1.50%	(Fin/40)*34.72 KHz
0	1	+/- 2.50%	(Fin/40)*34.72 KHz
1	0	+/- 0.50%	(Fin/40)*34.72 KHz
1	1	+/- 1.00%	(Fin/40)*34.72 KHz

rev 0.2

**Spread spectrum selection**

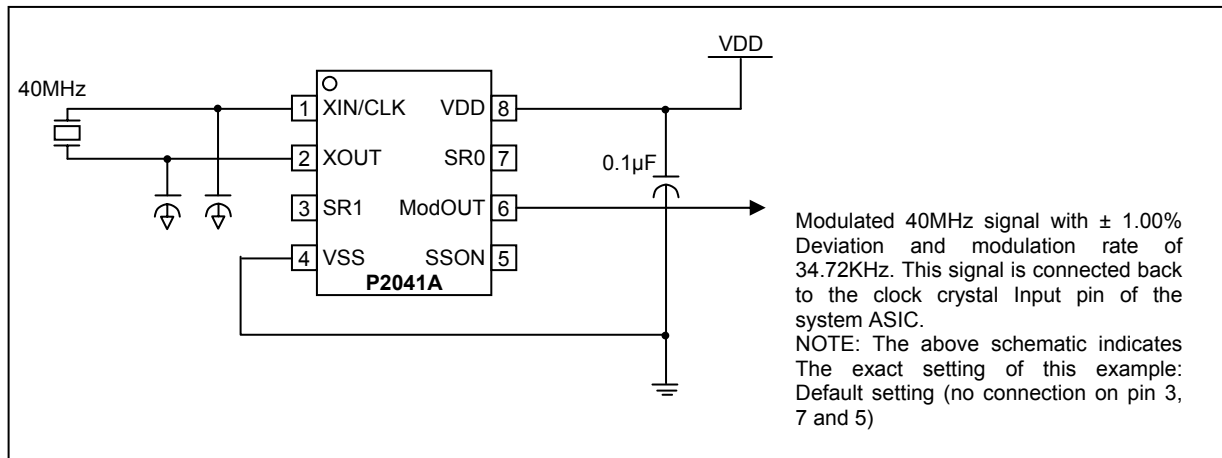
Table 1 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency ( Note: the center frequency is the frequency of the external reference input on XIN/CLK, Pin 1).

**Example of a typical printer or scanner application that operates on a clock frequency of 40MHz:**

A spreading selection of SR1=1 and SR0=1 provides a percentage deviation of +/-1.00%\* (see Table 1) of Center Frequency. This results in the frequency on ModOUT being swept from 40.40MHz to 39.60MHz at a modulation rate of  $(40/40)*34.72 = 34.72\text{KHz}$  (see Table 1). This particular example (see Figure below) given here is a common EMI reduction method for scanners and has already been implemented by most of the leading manufacturers.

**NOTE:** Spreading range selection varies from different system manufacturers and their designs. The spreading range of P2041A can be set to +/-2.5% when working with certain scanner model.

**P2041A Application Schematic for Flat-Bed Scanner**



**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Unit
VDD, V <sub>IN</sub>	Voltage on any pin with respect to Ground	-0.5 to +7.0	V
T <sub>STG</sub>	Storage temperature	-65 to +125	°C
T <sub>A</sub>	Operating temperature	-40 to +85	°C
T <sub>s</sub>	Max. Soldering Temperature (10 sec)	260	°C
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

**DC Electrical Characteristics**

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated)

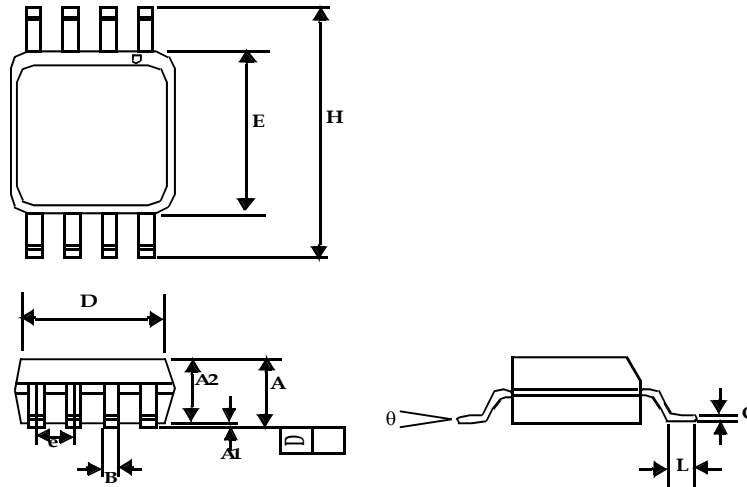
Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>IL</sub>	Input low Voltage	( For 3.3V Supply Voltage)	VSS -0.3	-	0.8	V
		( For 5V Supply Voltage)	-	-	1.5	
V <sub>IH</sub>	Input low Voltage	( For 3.3V Supply Voltage)	2.0	-	VDD + 0.3	V
		( For 5V Supply Voltage)	3.5	-	-	
I <sub>IL</sub>	Input Low Current (pull-up resistor on inputs SR0, SR1)	( For 3.3V Supply Voltage)	-	-	-35	µA
		( For 5V Supply Voltage)	-	-	-100	
I <sub>IH</sub>	Input High Current (pull-down resistor on input SSON )	( For 3.3V Supply Voltage)	-	-	35	µA
		( For 5V Supply Voltage)	-	-	100	
I <sub>XOL</sub>	XOUT Output Low Current (V <sub>XOL</sub> @ 0.4V, VDD = 3.3V)	-	3	-	mA mA	
I <sub>XOH</sub>	XOUT Output High Current ( V <sub>XOH</sub> @ 2.5V, VDD = 3.3V)	-	3	-		
V <sub>OL</sub>	Output Low Voltage	(VDD=3.3V, I <sub>OL</sub> = 20 mA)	-	-	0.4	V
		(VDD=5V, I <sub>OL</sub> = 20 mA)	-	-	0.5	
V <sub>OH</sub>	Output High Voltage	(VDD=3.3V, I <sub>OH</sub> = 20 mA)	2.5	-	-	V
		(VDD=5V, I <sub>OH</sub> = 20 mA)	4.5	-	-	
I <sub>DD</sub>	Static Supply Current	-	1.0	-	mA	
I <sub>CC</sub>	Dynamic Supply Current	3.3V and 15pF loading	-	-	22	mA
		5V and 15pF loading	-	-	35	
VDD	Operating Voltage	2.7	3.3	5.5	V	

**AC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>IN</sub>	Input Frequency	25	40	60	MHz
t <sub>LH</sub> *	Output rise time ( Measured at 0.8V to 2.0V )	0.7	1.0	1.3	nS
t <sub>HL</sub> *	Output fall time ( Measured at 2.0 to 0.8V )	0.6	0.8	1.0	nS
t <sub>JC</sub>	Jitter (Cycle to cycle)	-	360	-	pS
t <sub>D</sub>	Output duty cycle	45	50	55	%

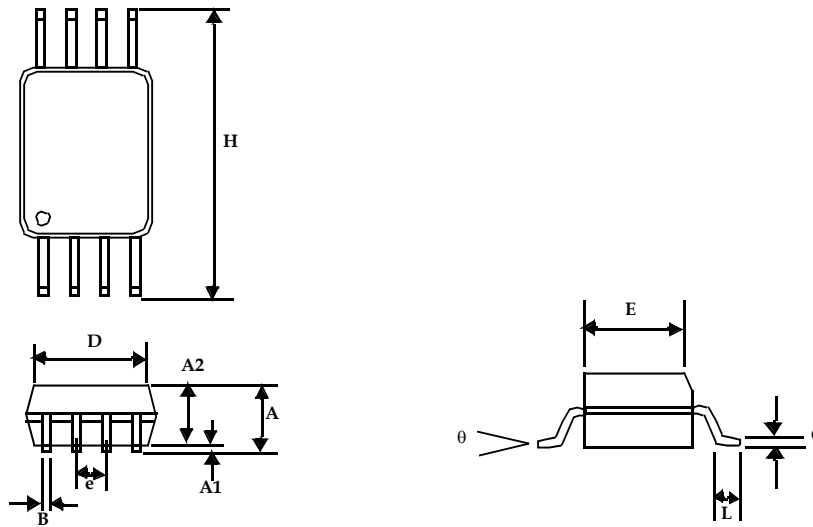
\*t<sub>LH</sub> and t<sub>HL</sub> are measured into a capacitive load of 15pF

8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
theta	0°	8°	0°	8°

8-lead TSSOP (4.40-MM Body)

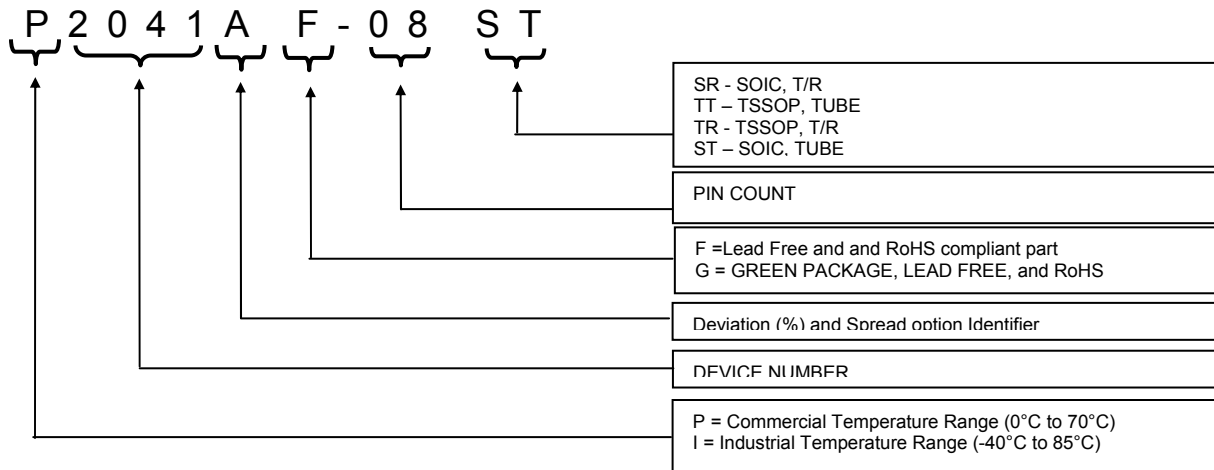


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

**Ordering Information**

Part number	Marking	Package Configuration	Temperature Range
P2041AF-08ST	P2041AF	8-Pin SOIC, Tube, Pb Free	Commercial
P2041AF-08SR	P2041AF	8-Pin SOIC, Tape and Reel, Pb Free	Commercial
P2041AF-08TT	P2041AF	8-Pin TSSOP, Tube, Pb Free	Commercial
P2041AF-08TR	P2041AF	8-Pin TSSOP, Tape and Reel, Pb Free	Commercial
P2041AG-08ST	P2041AG	8-Pin SOIC, Tube, Green	Commercial
P2041AG-08SR	P2041AG	8-Pin SOIC, Tape and Reel, Green	Commercial
P2041AG-08TT	P2041AG	8-Pin TSSOP, Tube, Green	Commercial
P2041AG-08TR	P2041AG	8-Pin TSSOP, Tape and Reel, Green	Commercial
I2041AF-08ST	I2041AF	8-Pin SOIC, Tube, Pb Free	Industrial
I2041AF-08SR	I2041AF	8-Pin SOIC, Tape and Reel, Pb Free	Industrial
I2041AF-08TT	I2041AF	8-Pin TSSOP, Tube, Pb Free	Industrial
I2041AF-08TR	I2041AF	8-Pin TSSOP, Tape and Reel, Pb Free	Industrial
I2041AG-08ST	I2041AG	8-Pin SOIC, Tube, Green	Industrial
I2041AG-08SR	I2041AG	8-Pin SOIC, Tape and Reel, Green	Industrial
I2041AG-08TT	I2041AG	8-Pin TSSOP, Tube, Green	Industrial
I2041AG-08TR	I2041AG	8-Pin TSSOP, Tape and Reel, Green	Industrial

**Device Ordering Information**



Licensed under US patent Nos 5,488,627 and 5,631,920.



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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