FX802
DVSR CODEC

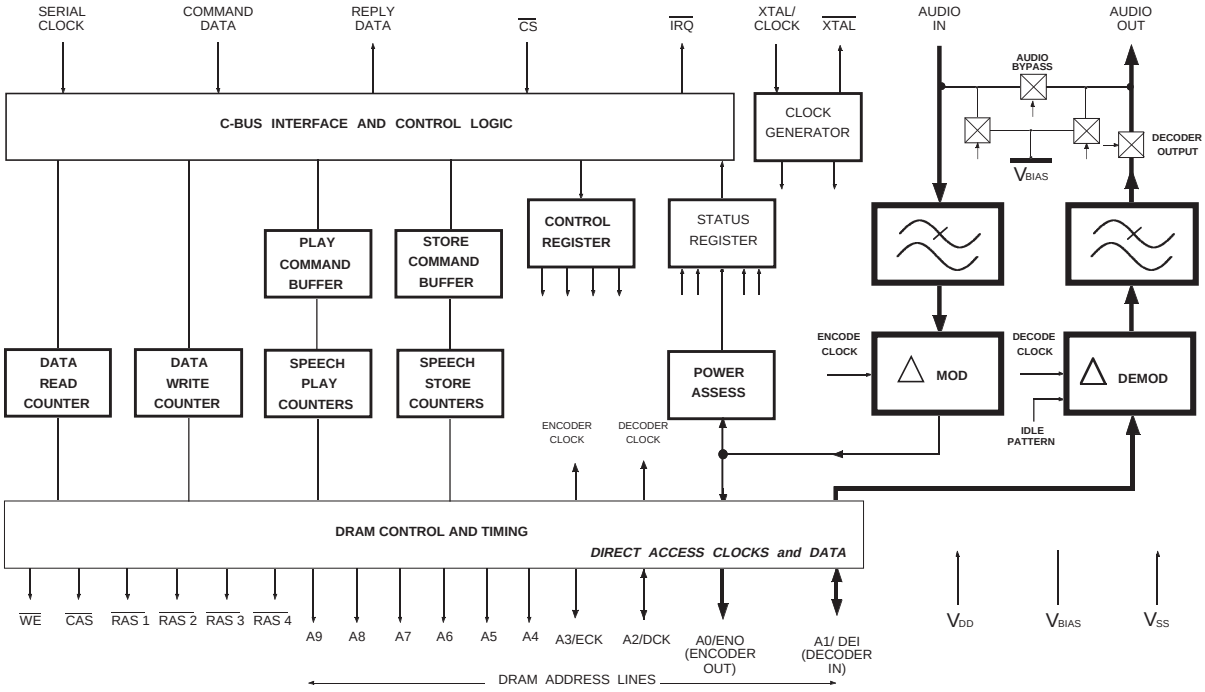

Fig.1 FX802 DVSR Codec

Brief Description

The FX802 DVSR Codec contains:

A Continuously Variable Slope Delta Modulation (CVSD) encoder and decoder.

Control and timing circuitry for up to 4Mbits of external Dynamic Random Access Memory (DRAM).

"C-BUS" µProcessor interface and control logic.

When used with external DRAM, the FX802 has four primary functions:

- **Speech Storage**
  Speech signals present at the Audio Input may be digitized by the CVSD encoder, and the resulting bit stream stored in DRAM. This process also provides readings of input power level for use by the system µController.
- **Speech Playback**
  Previously digitized speech data may be read from DRAM and converted back into analogue form by the CVSD decoder.
- **Data Storage**
  Digital data sent over the "C-BUS" from the system µController may be stored in DRAM.
- **Data Retrieval**
  Digital data may be read from DRAM and sent over "C-BUS" to the system µController.

Speech storage and playback may be performed concurrently with data storage or retrieval.

The FX802 may also be used without DRAM (as a "stand-alone" CVSD Codec), in which case direct access is provided to the CVSD Codec digital data and clock signals.

All functions are controlled by "C-BUS" commands from the system µController.

The Storage, Recovery and Replay functions of the FX802 can be used for:

- Answering Machine applications, where an incoming speech message is stored for later recall.
- Busy Buffering, an outgoing speech message is stored temporarily until the transmit channel becomes free.
- Automatic transmission of pre-recorded 'Alarm' or status announcements.
- Time Domain Scrambling of speech messages.
- VOX control of transmitter functions.
- Temporary Data Storage applications, such as buffering of over-air data transmissions.

On-chip the Delta Codec is supported by input and output analogue switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control and refresh signals to interface to external DRAM.

The FX802 DVSR Codec is a low-power 5-volt CMOS LSI device.

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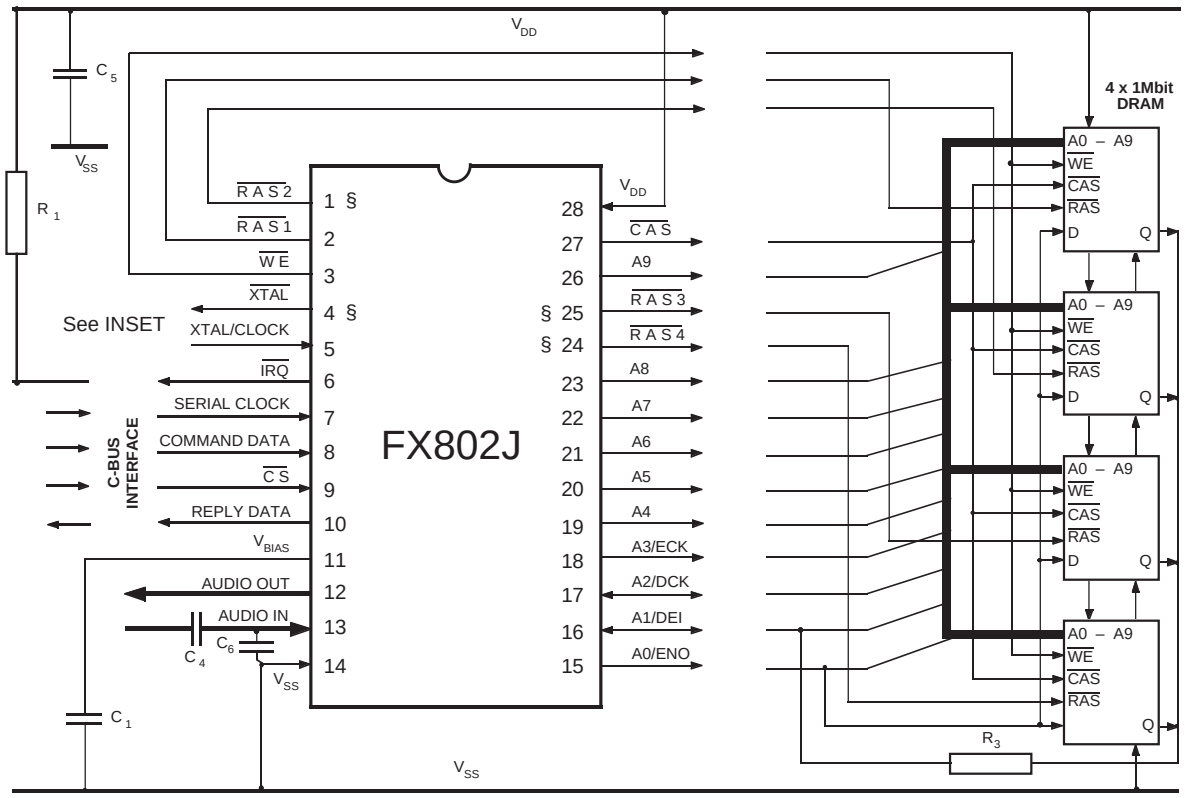
Pin Number Function

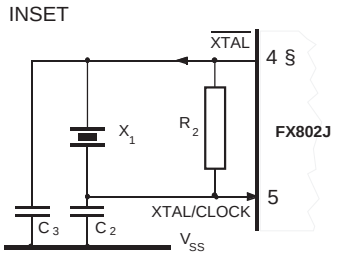
FX802 J	FX802 LG/LS	
1		**$\overline{\text{Row Address Strobe 2}}$ ($\overline{\text{RAS2}}$):** Should be connected to the Row Address Strobe input of the second 1Mbit DRAM chip (if fitted).
2	1	**$\overline{\text{Row Address Strobe 1}}$ ($\overline{\text{RAS1}}$):** Should be connected to the Row Address Strobe input of the first DRAM chip.
3	2	**$\overline{\text{Write Enable}}$ ($\overline{\text{WE}}$):** The DRAM Read/Write control pin.
4		**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal is employed. A Xtal cannot be used with the 24-pin version.
5	3	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here, see Figure 2. This clock provides timing for on-chip elements, filters etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device, see Table 3 for the sampling clock rate variations.
6	4	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. The pin has a low-impedance pulldown to logic "0" when active and a high impedance when inactive. Conditions indicated by this function are: Power Reading Ready, Play Command Complete, Store Command Complete.
7	5	**Serial Clock:** The "C-BUS," serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the DVSR Codec. See Timing Diagrams and System Support Document, Document 2. The clock-rate requirements vary for differing FX802 functions.
8	6	**Command Data:** The "C-BUS," serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams and System Support Document, Document 2.
9	7	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** The "C-BUS", data transfer control function, this input is provided by the µController. Command Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagrams and System Support Document, Document 2.
10	8	**Reply Data:** The "C-BUS," serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams and System Support Document, Document 2.
11	9	**V_{BIAS}:** The output of the on-chip analogue circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by a capacitor C_1, See Figure 2.
12	10	**Audio Out:** The analogue signal output.
13	11	**Audio In:** The audio (speech) input. The signal to this pin must be a.c. coupled by a capacitor C_4 and decoupled to V_{SS} by an HF bypass capacitor C_6. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.
14	12	**V_{SS}:** Negative supply rail (GND).

Pin Number Function

FX802 J	FX802 LG/LS	
15	13	**DRAM Data In/A0/ (Direct Access – Encoder Out (ENO)):** Connected to the DRAM data input and address line A0. With no DRAM employed this output is available (in Direct Access mode) as the Delta Encoder digital data output. Direct Access control is achieved by Control Register byte 1 – bit 6.
16	14	**DRAM Data Out/ A1/ (Direct Access – Decoder In (DEI)):** Connected to the DRAM data output and address line A1. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Decoder digital data input. Direct Access control is achieved by Control Register byte 1 – bit 6.
17	15	**DRAM A2/ (Direct Access – Decoder Clock (DCK)):** DRAM address line A2. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Decoder Clock input. Direct Access control is achieved by Control Register byte 1 – bit 6.
18	16	**DRAM A3/ (Direct Access – Encoder Clock (ECK)):** DRAM address line A3. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Encoder Clock output. Direct Access control is achieved by Control Register byte 1 – bit 6.
19	17	**DRAM A4:** DRAM address line A4.
20	18	**DRAM A5:** DRAM address line A5.
21	19	**DRAM A6:** DRAM address line A6.
22	20	**DRAM A7**: DRAM address line A7.
23	21	**DRAM A8:** DRAM address line A8.
24		**Row Address Strobe 4 ($\overline{\text{RAS4}}$):** Should be connected to the Row Address Strobe input of the fourth 1Mbit DRAM chip (if fitted).
25		**Row Address Strobe 3 ($\overline{\text{RAS3}}$):** Should be connected to the Row Address Strobe input of the third 1Mbit DRAM chip (if fitted).
26	22	**DRAM A9:** DRAM address line A9. This pin is not connected when a 256kbit DRAM is employed. **Note:** To simplify PCB layout, the DRAM address inputs A0 – A8 may be connected in any physical order to the DVSR Codec output pins A0 – A8.
27	23	**Column Address Strobe ($\overline{\text{CAS}}$):** The DRAM Column Address Strobe pin. Should be connected to the CAS pins of all DRAM chips.
28	24	$\mathbf{V_{DD}}$: Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the DVSR Codec are dependant upon this supply.

External Components





Component		Value
R_1	=	22.0kΩ
R_2		1.0MΩ
R_3		1.0kΩ
C_1		1.0µF
C_2		33.0pF
C_3		33.0pF

C_4	=	1.0µF
C_5		1.0µF
C_6		1.0nF
X_1		4.00MHz
	or	4.032MHz
	or	4.096MHz

Tolerance: R = ±10% C = ±20%

Fig.2 Recommended Component and DRAM Connections

Notes

1. Xtal circuitry shown INSET is in accordance with CML Application Note D/XT/2 December 1991.

2. External Xtal circuitry is not applicable to the 24-pin/lead versions of this device, only a clock pulse input can be used.

3. Functions whose pins are marked § above are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.

4. Table 3 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.

5. R_1 is used as the DBS 800 system common-pullup for the "C-BUS" Interrupt Request ($\overline{IRQ}$) line, the optimum value will depend upon the circuitry connected to the $\overline{IRQ}$ line. Up to 8 peripherals may be connected to this line.

6. Recommended DRAM Parameters:
   256kbit x 1 or 1Mbit x 1 Dynamic Random Access Memory with 'CAS before RAS' refresh mode, maximum Row Address Access time = 200nsec.

   Example DRAM types:
   256kbit (262,144bits)
   - Texas Instruments TMS4256–20
   - Hitachi HM51256–15

   1Mbit (1,048,576bits)
   - Texas Instruments TMX4C1024–15
   - Hitachi HM511000–15

7. Figure 2 (above) shows connections to 4 x 1Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0 to A8 may be connected in any order to the FX802 DVSR Codec output pins A0 to A8. Connections to 256kbit DRAM are similar, but A9 unconnected.

8. When using the FX802 "stand-alone (Direct Access)," no DRAM should be connected.

Controlling Protocol

Control of the functions of the FX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions or data to and from the system µController (see Figure 5). The use and content of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	+	Data Byte/s
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	60	0 1 1 0 0 0 0 0	+	2 byte Instruction to Control Register
Read Status Register	61	0 1 1 0 0 0 0 1	+	1 byte Reply from Status Register
Store 'N' pages. Start page 'X'	62	0 1 1 0 0 0 1 0	+	2 bytes Command – Immediate
Store 'N' pages. Start page 'X'	63	0 1 1 0 0 0 1 1	+	2 bytes Command – Buffered
Play 'N' pages. Start page 'X'	64	0 1 1 0 0 1 0 0	+	2 bytes Command – Immediate
Play 'N' pages. Start page 'X'	65	0 1 1 0 0 1 0 1	+	2 bytes Command – Buffered
Write Data. Start page 'P'	66	0 1 1 0 0 1 1 0	+	2 bytes 'P' + Write data
Read Data. Start page 'P'	67	0 1 1 0 0 1 1 1	+	2 bytes 'P' + Read data
Write Data – Continue	68	0 1 1 0 1 0 0 0	+	Write data
Read Data – Continue	69	0 1 1 0 1 0 0 1	+	Read data

Table 1 "C-BUS" Address/Commands

Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data, or
(ii) a Status or data Reply.

Control and configuration is by writing instructions from the µController to the Control Register (60_H).
Reporting of FX802 configurations is by reading the Status Register (61_H). Instructions and data are transferred, via "C-BUS," in accordance with the timing information given in Figures 5 and 6.
A complete list of DBS 800 "C-BUS" Address locations is published in the System Support Document.

Speech

The delta encoder and decoder sampling rates are independently set, via the Control Register (Table 4), to (nominally) 16, 25, 32, 50 or 64kbits/s (see Tables 2 and 3), allowing the user to choose between speech-quality and storage-time, whilst providing for time-compression or expansion of the speech signals.

The DVSR Codec can handle from 256kbits to 4Mbits of DRAM, giving, in the case of 32kbit/s sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into 'pages' of 1024 bits each, corresponding to 32ms at a 32kbit/s sampling rate.

A 256kbit DRAM contains	256 pages.
A 1Mbit DRAM contains	1024 pages.
4Mbit of DRAM contains	4096 pages.

The Delta Codec may be used without DRAM, when the decoder sampling rate (8 to 64 kbits/s) is determined by an external clock source applied to the Decoder Clock pin.

Operation with DRAM

The FX802 can operate with up to 4Mbits of DRAM. When used with DRAM the DVSR Codec performs four main functions under the control of commands received over the "C-BUS" interface from the µController:

Stores Speech by digitally encoding the analogue input signal and writing the resulting digital data into the associated Dynamic RAM (DRAM).

Plays stored speech by reading the digital data stored in the DRAM and decoding it to provide an analogue output signal.

Writes data sent over the "C-BUS" from the µController to DRAM.

Reads data from DRAM, sending it to the µC over the "C-BUS".

'Data' is directed to and from DRAM by the on-chip DRAM Controller.

Store and Play Speech Commands
Speech storage and playback may take place simultaneously.

These commands are transmitted, via "C-BUS," to the FX802, in the form:

STORE or PLAY 'N' (1024-bit) pages (of encoded speech data) starting at page 'X.'

'N' is any number from 1 to 16 (pages) and **'X'** from (page) 0 to 4095 (4Mbit DRAM), as illustrated below.
Preceded by the A/C, this command writes 16-bits (byte 1 (first) and byte 0) of data from the µC to the FX802 Store or Play Command Buffer.

MSB Byte 1								Byte 0							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
'N'								**'X'**							

Controlling Protocol .....

Store and Play Speech

Speech Store Commands

62_H STORE 'N' PAGES – START PAGE 'X' (immediate).

63_H STORE 'N' PAGES – START PAGE 'X' (buffered).

The digitised speech from the Delta Encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete 'pages' stored since the start of execution of the command.
As soon as the command has terminated the following events take place:

(1) The "Store Command Complete" bit in the Status Register (Table 6) is set.

(2) An "Interrupt Request" ($\overline{IRQ}$) is sent (if enabled) to the μC.

(3) The next Speech Store command (if present) is immediately taken from the Store Command Buffer and execution of the new command commences.

The $\overline{IRQ}$ output is cleared by reading the Status Register.

61_H READ STATUS REGISTER (Table 6).

To provide continuity of speech commands, both Store and Play commands can be presented to the FX802 in one of two formats; *Immediate or Buffered.*

An *Immediate* command will be started on completion of its loading, irrespective of the condition of the current command.

A *Buffered* command will be acted upon on the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps, even though the μController may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the Status Register will be cleared.

Speech Playback is controlled by similar commands:

64_H PLAY 'N' PAGES – START PAGE 'X' (immediate).

65_H PLAY 'N' PAGES – START PAGE 'X' (buffered).

using the Speech Play Counters and Play Command Buffer.

As soon as the Play Command has completed, the "Play Command Complete" bit in the Status Register is set and an Interrupt Request generated (if enabled).

If no 'next' command is waiting in the Play Command Buffer when a speech Play command finishes, a continuous idle code (0101.....0101) will be fed to the Delta Decoder.

Speech "data" is stored or recovered at the selected Encode or Decode sample rate (Table 3).
Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play command received from the μC, or by a General Reset command.

Store/Play Speech Synchronization – (Table 4)

This facility is provided, primarily, for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

No Speech Sync Set; Store and Play operations may take place completely independently.

Store after Play; The next "buffered" Store command will start *on completion of a Play operation*, whilst the next Play command (if any) sequence continues normally.

Play after Store; The next "buffered" Play command will start *on completion of a Store operation*, whilst the next Store command (if any) sequence continues normally.

These actions will continue whilst 'Speech Sync' bits remain set.

DRAM Speech Capacity

28-pin/lead versions of the FX802 may be used with a single 256kbit DRAM or with up to 4 x 1Mbit DRAM.
24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different Encode and Decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 2 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reverse sequence, see Control Register for details.

DRAM Size	Available Bits	"Speech Pages"	Nominal Sample Rates (kbits/s) 16	25	32	50	64
256kbits	262144	256	16.0	10.0	8.0	5.0	4.0
1024k	1048576	1024	65.0	42.0	32.0	20.0	16.0
2Mbits	2097152	2048	131.0	84.0	65.0	42.0	32.0
3M	3145728	3072	196.0	126.0	98.0	63.0	49.0
4M	4194304	4096	262.0	168.0	131.0	84.0	65.5
			Store and Play Times (seconds)				

Table 2 Sampling Clock Rates vs Speech Storage/Playback Times

Controlling Protocol .....

Data Operations

Data Storage and Recovery

For the purpose of storing data sent via “C-BUS” from the µC, the memory (DRAM) is divided into ‘data-pages’ of 64-bits (8-bytes).

A single 256kbit DRAM contains 4096 data-pages.
A single 1Mbit DRAM contains 16384 data-pages.
4Mbit DRAM contains 65536 data-pages.

In accordance with “C-BUS” timing specifications, data is handled 8-bits (1-byte) at a time although any number of 8-bit blocks of data may be written-to or read-from the DRAM by a single command.

The data transfer action is terminated by the Chip Select line being taken to a logic “1.

“C-BUS” Data Transfer Limitations

For those commands which transfer data over the “C-BUS” between DRAM and the µController (Write and Read Data) the “C-BUS” Serial Clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing Store and Play commands.

250kHz if no speech Store or Play commands are active.

All other commands and replies (Control, Status, General Reset) may use a maximum clock rate of 500kHz. See Figure 5.

Read and Write Data actions are explained below

Read Data

67_H READ DATA – START PAGE “P”

Sets the Data Read Counter to “P” page and then reads data bytes from successive DRAM locations, sending them to the µC as Reply Data bytes incrementing the Data Read Counter by 1 for each bit read.

69_H READ DATA – CONTINUE

Reads data bytes from successive DRAM locations determined by the Data Read Counter incrementing the counter by 1 for each bit read.

Write Data

66_H WRITE DATA – START PAGE “P”

Sets the Data Write Counter to “P” page and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the “C-BUS.”

The Start Page “P,” is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data-page addresses from 0 to 65535 (4Mbits DRAM).

68_H WRITE DATA – CONTINUE

Writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the “C-BUS.”

Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 3 shows the range of sampling rates available for differing Xtal/clock input frequencies, and the counter ratios used to produce them.
If different “Store and Play” sampling rates are used in a single operation, only combinations of 25kb/s with 32kb/s or 50kb/s with 64kb/s will give correct output levels in accordance with current specifications. Consideration should be given to the effect of differing Xtal/clock frequencies upon the audio frequency performance of the device.

				Xtal/clock Frequency (MHz)		
Control Register *Byte 0, Bits* **5 2**	**4 1**	**3 0**	**Dec. Enc.**	**Internal Counter Division Ratio**	**4.0**	**4.032**	**4.096**
					Sampling Rate (kbits/s)		
0	1	1		256	15.625	15.75	16.0
1	0	0		160	25.0	25.20	25.60
1	0	1		128	31.25	31.50	32.0
1	1	0		80	50.0	50.4	51.20
1	1	1		64	62.50	63.0	64.0

Table 3 Sampling Clock Rates Available

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use it should be noted that:
(a) a 4.032MHz Xtal/clock input will produce an accurate 1200 baud rate for the FX809 FFSK Modem
(b) a 4.096MHz Xtal/clock input will generate exactly 16kb/s and 32kb/s Codec sampling clock rates.

"Write to Control Register" – Address/Command 60_H, followed by 2 bytes of Command Data

Setting	*Function*
Byte 1	***First Byte for Transmission***
(MSB) Bit 7	Not used – Set to "0"
6	**Direct Access**
1	– Encoder Data Out to A0/ENO – Encoder Clock to A3/ECK – Decoder Input from A1/DEI – Decoder Clock from A2/DCK
0	Normal DVSR Operation
5	**Play Counter**
1	Decrement
0	Increment
4	**DRAM Control**
1	Disable DRAM
0	Enable DRAM
3	**Codec Powersave**
1	Powersave Delta Codec
0	Enable Delta Codec
2	**Store Command Interrup**t
1	Enable Interrupt
0	Disable
1	**Play Command Interrup**t
1	Enable Interrupt
0	Disable
0	**Power Reading Interrupt**
1	Enable Interrupt
0	Disable
Byte 0	***Last Byte for Transmission***
(MSB) 7 6	**Store/Play Speech Sync**
0 0	No Sync
0 1	No Sync
1 0	Sync – Play after Store
1 1	Sync – Store after Play
5 4 3	**Decoder Control**
0 0 0	Idle (32kbit/s); Aud O/P via L.P.F.
0 0 1	Idle (32kbit/s); Aud By-Pass
0 1 0	Idle (32kbit/s); Aud O/P at High Z
0 1 1	On – Sampling Rate 16kbit/s
1 0 0	On – " 25kbit/s
1 0 1	On – " 32kbit/s
1 1 0	On – " 50kbit/s
1 1 1	On – " 64kbit/s
2 1 0	**Encoder Control**
0 0 0	I/P at V_{BIAS} – F/Idle (32kbit/s)
0 0 1	I/P at High Z – F/Idle (32kbit/s)
0 1 0	I/P at High Z – F/Idle (32kbit/s)
0 1 1	On – Sampling Rate 16kbit/s
1 0 0	On – " 25kbit/s
1 0 1	On – " 32kbit/s
1 1 0	On – " 50kbit/s
1 1 1	On – " 64kbit/s

Table 4 Control Register

General Reset

Upon Power-Up the "bits" in the FX802 registers will be random (either "0" or "1"). A General Reset command (01_H) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX802:

Control Register Set as 00_H
Status Register Set as 00_H
Clear Store and Play Command Buffers

Direct Access

Allows external circuitry "Direct Access" to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the FX802 to be used as a "stand-alone" delta modulation voice encoder and decoder.

Input Audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

The following points, with respect to Control Register settings, should be considered. Analogue output switching remains under the control of the Control Register, but the Decoder sampling clock rate (8kbit/s to 64kbit/s) must be provided from an external source to the Decoder Clock (DCK) pin. To ensure correct filter setting, Decoder Control bits (Byte 0, Bits 5, 4, 3) should be set to (binary) 1, 1, 1, where the required rate approximates to a multiple of 16kb/s, or (binary) 1, 1, 0, where the required rate approximates to a multiple of 25kb/s.

Both the Encoder internal sampling clock rate and input switching (Table 5) remain under the control of the Control Register. The sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

Play Counter

The Play Counter direction may be set to run backwards as well as forwards. This can be used in a scrambling system by replaying speech data in reverse order.

DRAM Control

A logic "1" will disable the DRAM Control timing circuits and associated counters. The "C-BUS" Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic "1" when the FX802 is used in the Direct Access mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to a logic "1."

Codec Powersave

A logic "1" puts the Delta Codec and filters into a Powersave mode, with V_{BIAS} maintained.

The Clock Generator, "C-BUS" Interface and DRAM Control and Timing remain active.

Command Interrupt Enable

A logic "1" set at the relevant bit will enable Interrupt Requests to the µController when that command operation is complete.

Store and Play Speech Synchronization

Intended, primarily, for Time Domain Scrambling.

Decoder and Encoder Control

Sets individually, decoder and encoder sampling clock rates and the source of the Audio Output.

Encoder and Decoder Control

Analogue Input and Output Switching

The Control Register, Byte 0 – bits 0 to 5, are used, in conjunction with the codec Powersave Bit (Byte 1 – bit 3) to control codec input/output conditions and sample rates. Figure 3 shows the codec functional situation.

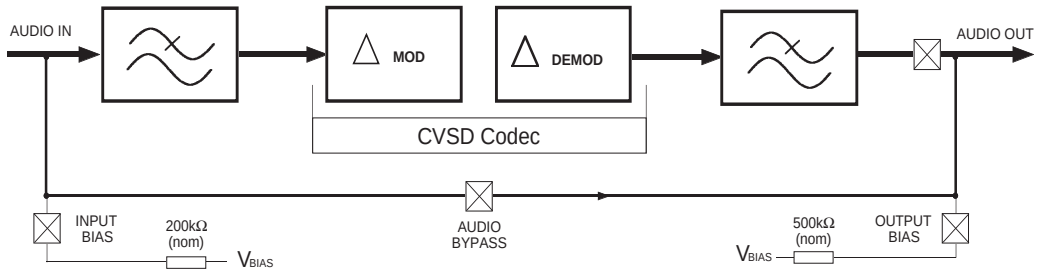


Fig.3 Analogue Control – with reference to Fig.1

Control Register				Circuit Switches			OFF = Switch Open ON = Switch Closed	
Codec Powersave Bit	**Decoder Control "5"**	**"4"**	**"3"**	**Audio By-Pass**	**Audio Out**	**Output Bias**		**Note**
0	0	0	0	OFF	ON	OFF	Decoder 'idling' fed with "1010101 ...." pattern at 32kb/s.	**1**
0	0	0	1	ON	OFF	OFF		
0	0	1	0	OFF	OFF	OFF		
0	0	1	1	OFF	ON	OFF	Decoder running at the selected sampling rate.	**1**
–	–	–	–	–	–	–		
0	1	1	1	OFF	ON	OFF		
1	0	0	0	OFF	OFF	ON	Decoder circuits Powersaved	
1	0	0	1	ON	OFF	OFF		
1	0	1	0	OFF	OFF	ON		
1	0	1	1	OFF	OFF	ON		
–	–	–	–	–	–	–		
1	1	1	1	OFF	OFF	ON		
	Encoder Control "2"	**"1"**	**"0"**		**Input Bias**			**2**
0	0	0	0		ON		Encoder running at 32kb/s but Encoder Data Output forced to 'idle' pattern "01010 ..."	
0	0	0	1		OFF			
0	0	1	0		OFF			
0	0	1	1		OFF		Encoder running at selected Sampling Rate	
–	–	–	–		–			
0	1	1	1		OFF			
1	0	0	0		ON		Encoder circuits Powersaved	
–	–	–	–		–			
1	1	1	1		ON			

Table 5 Analogue Control – with reference to Fig.3

Notes

1. If the Delta Codec is in the Direct Access mode, these sampling rates will be as provided by the externally applied clock.

2. The Input Bias switch is operated by the Control Register Codec Powersave' and 'Encoder Control' bits to provide a relatively low impedance path for V_{BIAS} to charge the input coupling capacitor whenever the codec is powersaved, or the Encoder control bits are set to "0," so that input bias can be established quickly prior to operation.

Time Compression of Speech

The 25kb/s and 50kb/s sampling rate options are provided for time compression (and subsequent expansion) of speech signals.

For example, 1.0 second of speech stored at 50kb/s may be transmitted in 0.8 seconds if played out at 64kb/s, and finally restored to its original speed at the receiver by storing at 64kb/s and playing out at 50kb/s. A similar result (with a degraded SINAD) may be achieved by using 25kb/s and 32kb/s sampling rates.

However, the speech frequencies are raised by time compression, and since the signal transmitted to air must be band limited to 3400Hz, the effective end-to-end bandwidth is 0.8 x 3400Hz, which is approximately 2700Hz.

"Read Status Register" – Address/Command, 61_H, followed by 1 byte of Reply Data.

Reading					*Function*	
MSB						
Bit 7					**Power Reading**	
1					Ready	
6					**Store Command**	
1					Complete	
5					**Play Command**	
1					Complete	
					Power Register	
4	***3***	***2***	***1***	***0***	**Pwr**	**Compand Bits**/page
0	0	0	0	0		0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0	-39.0 dB	8
0	1	0	0	1		10
0	1	0	1	0	-36.0	12
0	1	0	1	1		14
0	1	1	0	0	-33.5	16
0	1	1	0	1		18
0	1	1	1	0	-30.0	20
0	1	1	1	1		22
1	0	0	0	0	-28.0	24
1	0	0	0	1		32
1	0	0	1	0	-25.0	40
1	0	0	1	1		48
1	0	1	0	0	-22.0	56
1	0	1	0	1		64
1	0	1	1	0	-19.0	72
1	0	1	1	1		80
1	1	0	0	0	-16.0	88
1	1	0	0	1		128
1	1	0	1	0	-10.0	192
1	1	0	1	1		256
1	1	1	0	0	-6.0	320
1	1	1	0	1		384
1	1	1	1	0	0dB	448
1	1	1	1	1		512

Table 6 Status Register

Interrupts
An Interrupt Request (IRQ), (if enabled by the Control Register) is produced by the FX802 to report the following actions:

Power Reading Ready
Store Command Complete
Play Command Complete.

When an Interrupt Request is produced the Status Register must be read to ascertain the source of the interrupt. This action will clear the IRQ output.

Store Command Complete bit
(and an interrupt) is set on completion of a Store command. This bit is cleared by loading the next Store command, or by a General Reset command (01_H).

Play Command Complete bit
(and an interrupt) is set on completion of a Play command. This bit is cleared by loading the next Play command, or by a General Reset command (01_H).

Power Reading Ready bit
(and an interrupt) is set for every 1024 (1 page) voice-data bits from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset command (01_H).

Power Register
The power assessment element shown in Figure 1 assesses the input signal power for each encoded 'page' (every 1024 encoder output bits) by counting the number of 'compand bits' (000 or 111 sequences in the output bit-stream) produced during that 'page,' shown in Table 6, with typical encoder input power levels (dB).
Power Reading measurements (Bits 0 – 4) are produced under the same conditions as in Figure 4.

At the end of each 'page' the "Power Reading Ready" bit of the Status Register is set, an Interrupt Request is generated (if enabled) and the resulting count converted to a 5-bit quasi-logarithmic form.

The Power Register reading is interpreted as below.

00000	represents	0 compand bits
00001	represents	1 compand bit
11111	represents	512 compand bits – the maximum.

This "Power" reading is placed in the Status Register where it can be read by the µC.

Figure 4 shows this output in graphical form, indicating the typical Input Power Level.

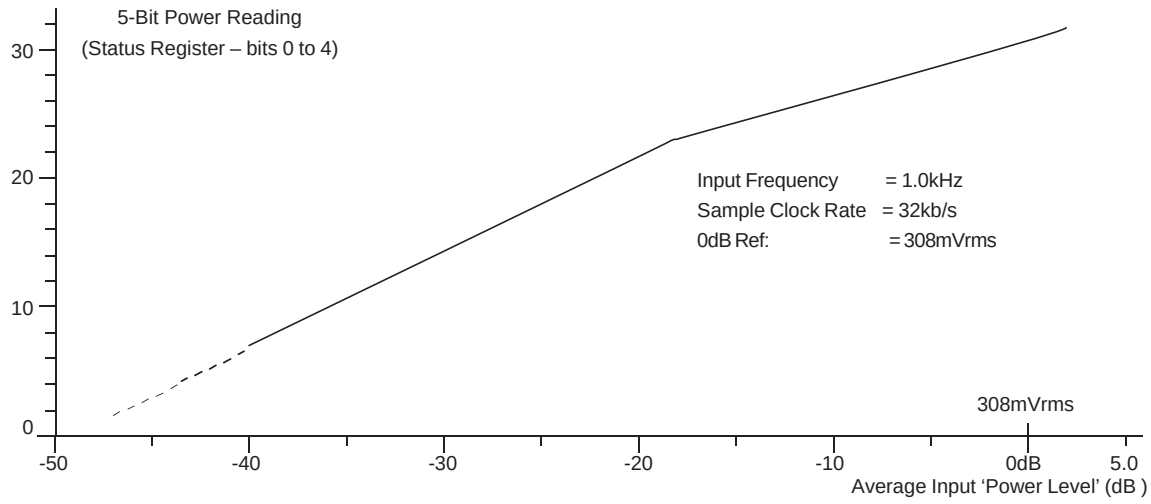


Fig.4 Typical "Power" Readings vs Input Level

Timing Information

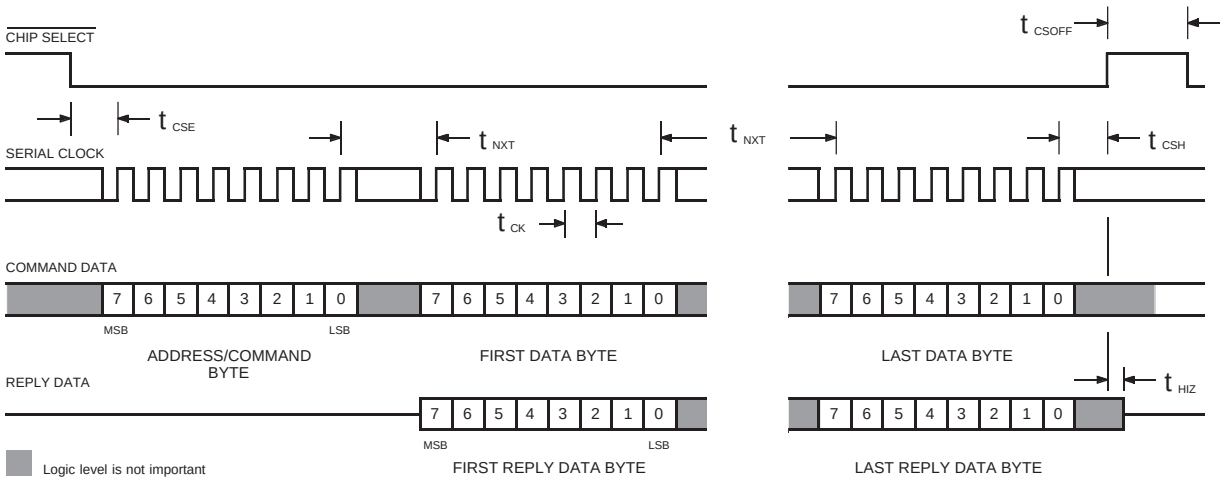


Fig.5 "C-BUS" Timing Information

NOT TO SCALE

"C-BUS" Timing – Figure 5

Parameter	Min.			Max.	Unit
	a	**b**	**c**		
t_{CSE}	2.0	4.0	8.0	–	µs
t_{CSH}	4.0	4.0	8.0	–	µs
t_{HIZ}	–	–	–	2.0	µs
t_{CSOFF}	2.0	4.0	8.0	–	µs
t_{NXT}	4.0	8.0	16.0	–	µs
t_{CK}	2.0	4.0	8.0	–	µs

Direct Access Timing – Figure 6

Parameter	Min.	Typ	Max.	Unit
t_{CH}	1.0	–	–	µs
t_{CL}	1.0	–	–	µs
t_{SU}	450	–	–	ns
t_{H}	600	–	–	ns
t_{PCO}	–	–	750	ns

$t_{SU} + t_H$ = Data True Time

Notes

(1) **Minimum Timing Values**
- (a) For all commands except "Read Data" and "Write Data" commands.
- (b) For "Read Data" and "Write Data" commands when no "Speech Store" or "Speech Play" commands are active.
- (c) For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.

(2) Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first, LSB (bit0) last. Reply Data is read from the peripheral MSB (bit7) first, LSB (bit0) last.

(3) To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity Serial Clock pulses.

(4) Data sent from the µController is clocked into the FX802 on the rising edge of the Serial Clock pulses. Reply Data sent from the FX802 to the µController is clocked into the µController when the Serial Clock is "high."

(5) Loaded commands are acted upon at the end of each command.

Direct Access

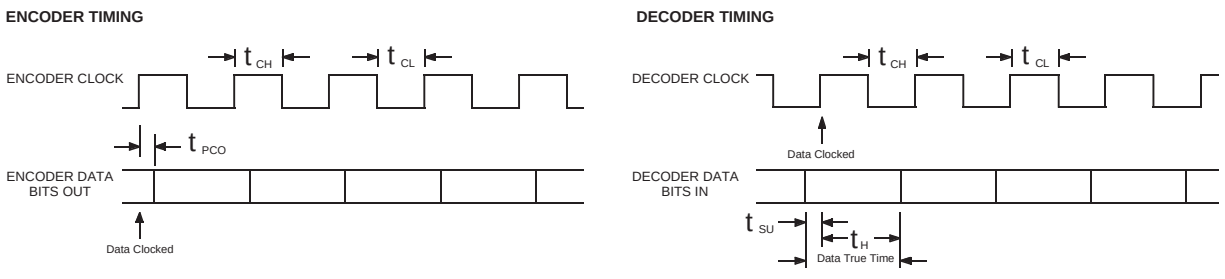


Fig.6 Codec Direct Access Timing

NOT TO SCALE

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX802J**	-40°C to +85°C (cerdip)
	FX802LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX802J**	-55°C to +125°C (cerdip)
	FX802LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0MHz. Standard Test Signal f_o = 1.0kHz. Sample Rate = 31.25kbits/s
Audio Level 0dB ref: = 308mVrms .

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current (enabled)	1	–	7.0	–	mA
Supply Current (all powersaved)	1	–	1.0	–	mA
Digital Interface					
Input Logic "1"	2, 4	3.5	–	–	V
Input Logic "0"	2, 4	–	–	1.5	V
Output Logic "1"					
at IOH = -120µA	8, 4	4.6	–	–	V
at IOH = -50µA	3, 4	4.6	–	–	V
at IOH = 20µA	4, 10	4.6	–	–	V
Output Logic "0"					
at IOL = 20µA	4, 10	–	–	0.4	V
at IOL = 100µA	3, 4	–	–	0.4	V
at IOL = 360µA	4, 8, 9	–	–	0.4	V
Digital Input Current					
(V_{IN} = Logic "1" or "0")	2	–	–	1.0	µA
Leakage Current into IRQ "OFF" Output	5	–	–	4.0	µA
Digital Input Capacitance	2	–	–	7.5	pF
Analogue Impedance					
Input Impedance	13	–	500	–	kΩ
Output Impedance		–	1.5	–	kΩ
Dynamic Values					
Encoder					
Analogue Signal Input Levels	6	-24.0	–	4.0	dB
Passband	11, 12	–	3400	–	Hz
Decoder					
Analogue Signal Output Levels	6	-24.0	–	4.0	dB
Passband	11, 12	300	–	3400	Hz
Encoder/Decoder (Full Codec)					
Passband	11, 12	300		3400	Hz
Passband Gain	12	–	0	–	dB
Passband Ripple	12	-3.0	–	3.0	dB
Stopband		6.0	–	10	kHz
Stopband Attenuation		–	50.0	–	dB
SINAD Level (-6dB)		–	23.0	–	dB
Output Noise (Input short circuit)		–	-50	–	dBp
Idle Channel Noise (Forced)		–	-55	–	dBp
Xtal/clock Frequency	7	–	4.0	–	MHz

Notes

1. Does not include current drawn by any attached DRAM.
2. Serial Clock, Command Data, CS, A1/DEI and A2/DCK inputs.
3. CAS, WE and A0 to A9 outputs.
4. All measurements are made at 5.0 volts V_{DD}, any variations may alter parameters accordingly.
5. When the IRQ Output is at V_{DD}.
6. The optimum range of levels for a good Signal-to-Noise Ratio.
7. Audio frequency responses will vary with respect to Xtal/clock frequency.
8. Reply Data output.
9. IRQ output.
10. RAS Outputs.
11. Passband is reduced to (typically) 2700Hz when a sample rate of 25kb/s or 50kb/s is employed.
12. Measured with a -20dB input level to avoid codec slope-overload.
13. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.

Codec Performance

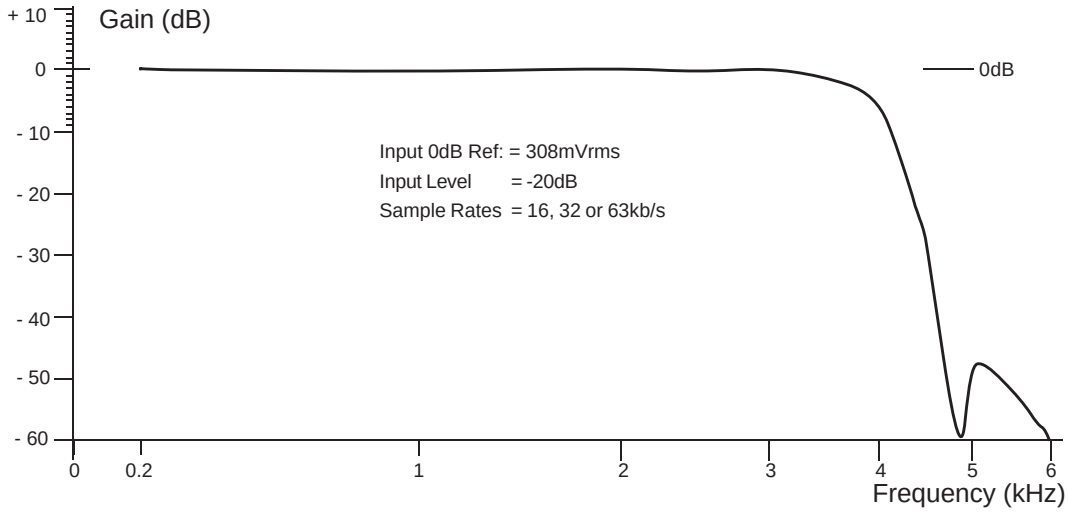


Fig.7 Typical Overall (Encoder + Decoder) Frequency Response

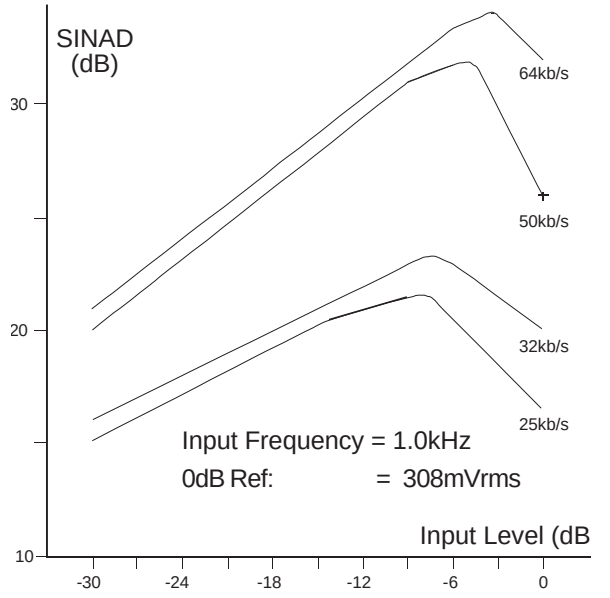


Fig.8 SINAD vs Input Level at Differing Sample Rates

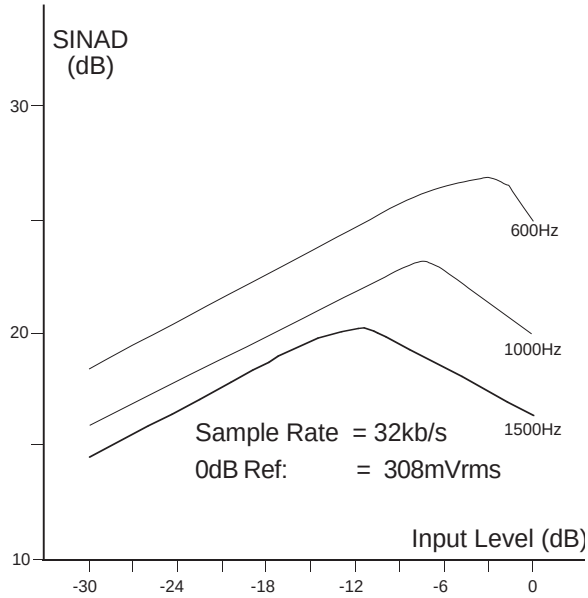


Fig.9 SINAD vs Input Level at Differing Frequencies

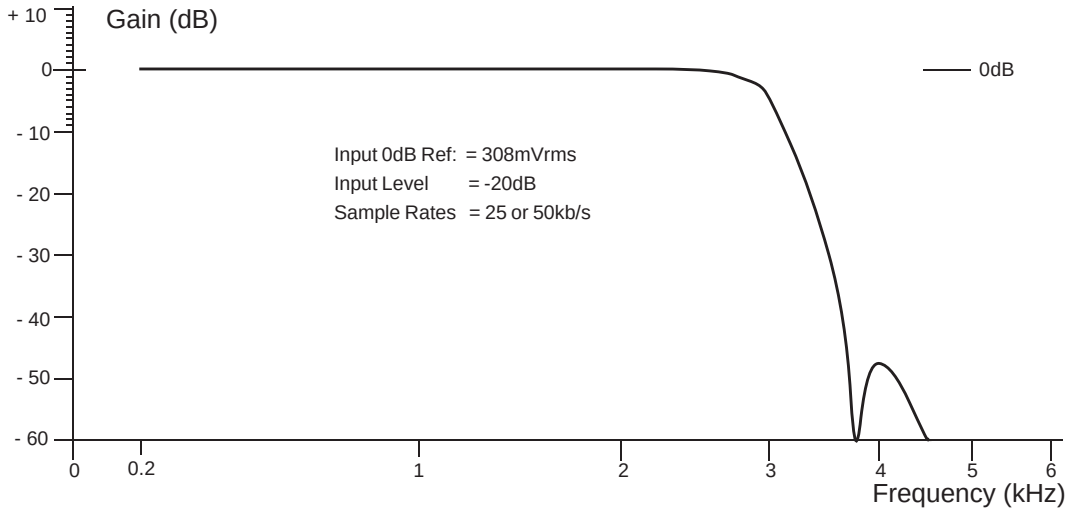


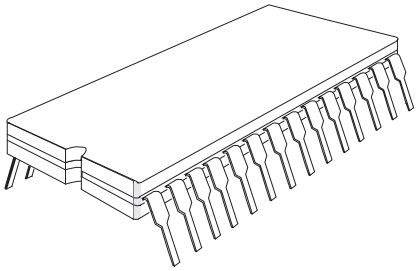
Fig.10 Typical Overall (Encoder + Decoder) Frequency Response

Package Outlines

The FX802 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX802J 28-pin cerdip DIL (J5)

NOT TO SCALE



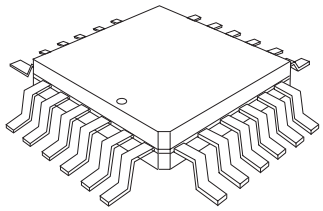
Max. Body Length 37.05mm
Max. Body Width 13.36mm

Handling Precautions

The FX802 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX802LG 24-pin quad plastic encapsulated bent and cropped (L1)

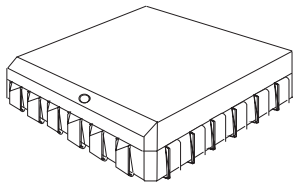
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX802LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX802J	28-pin cerdip DIL (J5)
FX802LG	24-pin encapsulated bent and cropped (L1)
FX802LS	24-lead plastic leaded chip carrier (L2)