

Silicon PNP Power Transistors

2SB1361

DESCRIPTION

- With TO-3PFa package
- Complement to type 2SD2052
- High transition frequency
- Wide area of safe operation

APPLICATIONS

- For high power amplification

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

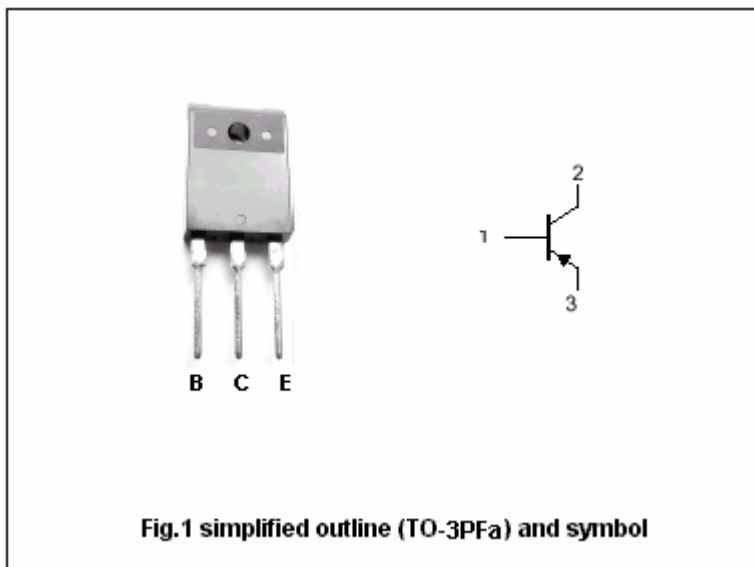


Fig.1 simplified outline (TO-3PFa) and symbol

Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-150	V
V _{CEO}	Collector-emitter voltage	Open base	-150	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-9	A
I _{CP}	Collector current-peak		-15	A
P _C	Collector power dissipation	T _C =25°C	100	W
			3	
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEsat}	Collector-emitter saturation voltage	I _C =-7A ; I _B =-0.7A			-2.0	V
V _{BE}	Base-emitter on voltage	I _C =-7A ; V _{CE} =-5V			-1.8	V
I _{CBO}	Collector cut-off current	V _{CB} =-150V; I _E =0			-50	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-3V; I _C =0			-50	μA
h _{FE-1}	DC current gain	I _C =-20mA ; V _{CE} =-5V	20			
h _{FE-2}	DC current gain	I _C =-1A ; V _{CE} =-5V	60		200	
h _{FE-3}	DC current gain	I _C =-7A ; V _{CE} =-5V	20			
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =-10V; f=1MHz		270		pF
f _T	Transition frequency	I _C =-0.5A ; V _{CE} =-5V; f=1MHz		15		MHz

◆ h_{FE-2} classifications

R	Q	P
40-80	60-120	100-200

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PACKAGE OUTLINE



Fig.2 Outline dimensions (unindicated tolerance:±0.30mm)