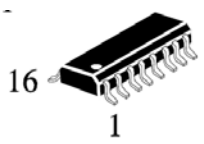
Low Drop Regulator with Signal Interface Logic Circuit

IK3101

DESCRIPTION

The IC is linear voltage regulator 5V with low dropout voltage typically 100mV at light loads and less then 500mV at full loads, with better then 4% output voltage accuracy. In additional IC have logical blokes for additional functions.



D SUFFIX
SOIC

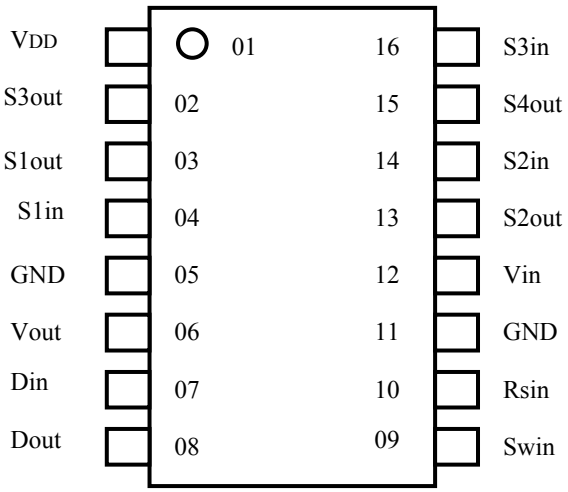
ORDERING INFORMATION
IK3101 SOIC

T_A = -40° to 85°C for package

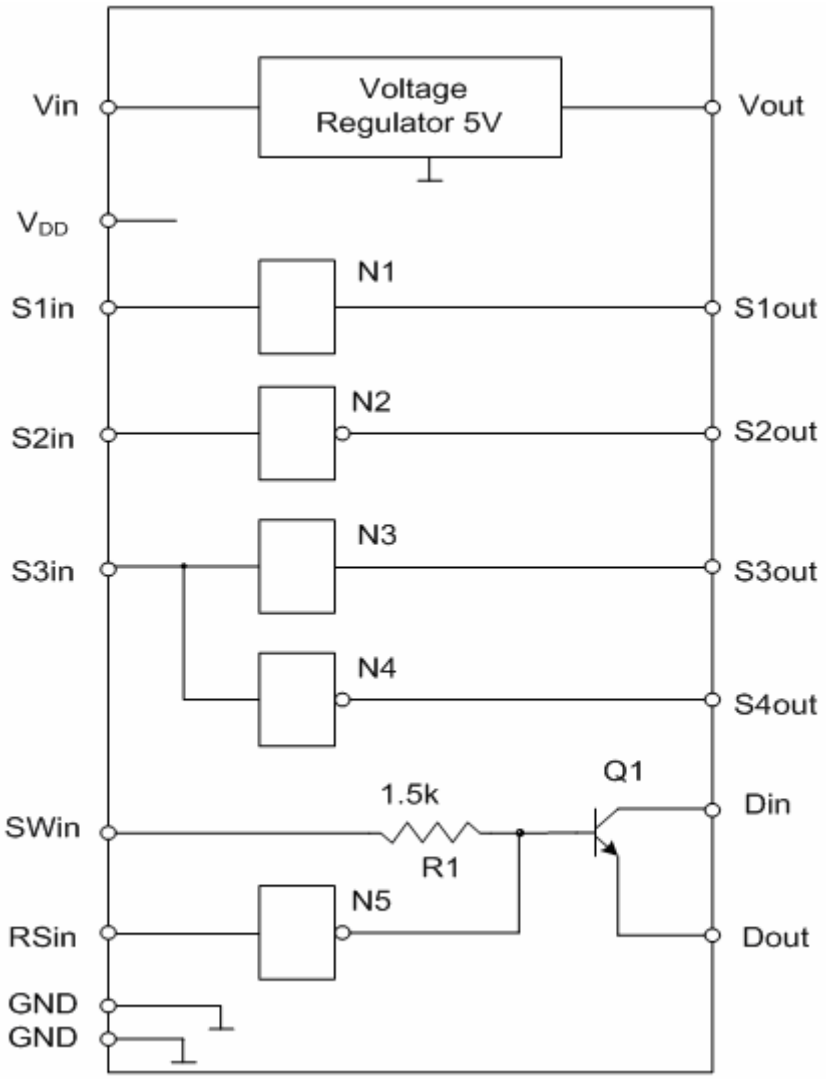
FEATURES

- Voltage regulator 5V with 4% output voltage accuracy
- Low dropout voltage 0.7V Max
- Load current 200mA Max
- Low Standby Current Consumption : 500μA
- Logical blokes for internal back light control
- Over Voltage & Over Temperature Protection
- Short Current Protection
- 60V Load Dump Protection

PIN DIAGRAM



PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
01	VDD	Power supply logic blokes	09	Swin	Input Swin
02	S3out	Output S3out	10	Rsin	Input Rsin
03	S1out	Output S1out	11	GND	Ground
04	S1in	Input S1in	12	Vin	Input voltage
05	GND	Ground	13	S2out	Output S2out
06	Vout	Output regulator voltage 5V	14	S2in	Input S2in
07	Din	Input Din	15	S4out	Output S4out
08	Dout	Output Dout	16	S3in	Input S3in



Schematic Diagram

MAXIMUM RATINGS (Ta=25°C)

Symbol	Characteristics	Rating	Units
Vin	Operating Input Voltage	29	V
Iout	Output Current	200	mA
S1in	Input Voltage	24	V
S2in	Input Voltage	24	V
S3in	Input Voltage	24	V
Swin	Input Voltage	5	V
Rsin	Input Voltage	24	V
Din	Input Voltage	5	V
Ta	Operating Temperature	From -40 to 85	°C
Pd	Power Dissipation	500	mW
Tj	Junction Temperature	-50 ~ 150	°C
Ts	Storage Temperature	-55 ~ 155	°C

DC ELECTRICAL CHARACTERICTICS

(Unless otherwise specified Vin=13V, Vout connected to V_{DD}, Iout=10mA, Cout=100µF, Tj=25°C)

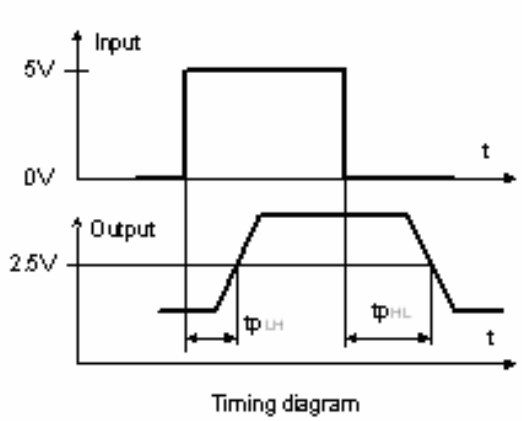
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Voltage regulator						
Output Voltage	Vout	6V ≤ Vin ≤ 24V	4.8	5.0	5.2	V
Voltage Regulation	Reg-Line	6V ≤Vin ≤ 16V			30	mV
Load Regulation	Reg-Load	10mA ≤ Iout ≤ 100mA			50	mV
Dropout Voltage	Vd	Iout=50mA Iout=100mA			0.5 0.7	V
Quiescent Current	Iq	S1in, S2in, S3in, SWin, RSin, Din – open			500	µA
Logic blokes						
High Level Voltage S1out	V_{OH}	S1in=2 - 5V, Iload= - 0.5mA	S1in - 1.2V			V
S2out		S2in=3V, Iload= - 0.5mA	V_{DD} - 0.5V			
S3out		S3in=2 - 5V, Iload= - 0.5mA	V_{DD} - 0.5V			
S4out		S3in=0.2V Iload= - 0.1mA	V_{DD} - 1.5V			
Low Level Voltage S1out	V_{OL}	S1in=0.2V, Iload=0.1mA			1.5	V
S2out		S2in= V_{DD}-0.2V, Iload=0.1mA			1.5	
S3out		S3in=0.2V, Iload=0.1mA			1.5	
S4out		S3in=2 -5V, Iload= 0.5mA			0.5	
Input Current S1in, S2in, S3in, RSin	Iin	S1in=5V, S2in=0V, S3in=5V, Rsin=5V,			0.50	mA
SWin		SWin=5V			3.5	mA
Output Current Din	IDin -	SWin=5V, RSin=0V, Din=13V, Dout=0V	100			mA
Leakage Current Din	I leakage	SWin=5V, RSin=5V, Din=13V, Dout=0V			10	µA
Saturation Voltage D	Vsat	SWin=5V, RSin=0V Dout=0V Iout=50mA Iout=100mA			 0.5 0.7	V

AC ELECTRICAL CHARACTERISTICS (C_L=15pF, V_{DD}= 5 V)

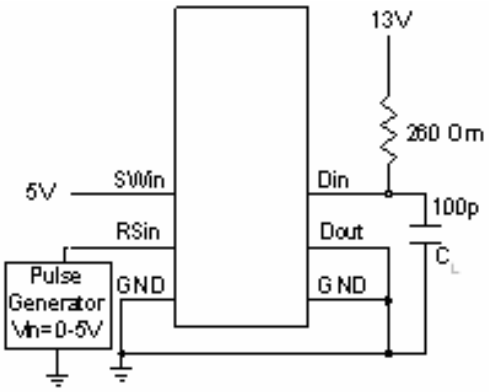
(Unless otherwise specified Vin=13V, Vout connected to V_{DD}, Iout=10mA, Cout=100µF, Tj=25°C)

Parameter	Sumbol	Conditions	Min	Typ	Max	Units
Propagation delay from S1in to S1out	tpLH tpHL	C_L=100p		65 400		ns
Propagation delay from S2in to S2out	tpLH tpHL	C_L=100p		190 720		ns
Propagation delay from S3in to S3out	tpLH tpHL	C_L=100p		240 1250		ns
Propagation delay from S3in to S4out	tpLH tpHL	C_L=100p		550 65		ns
Propagation delay (*1) from RSin to Din	tpLH tpHL	SWin=5V, Dout=0V, R_L=260 Om, C_L=100p		50 75		ns

*1-See circuit in testing schema

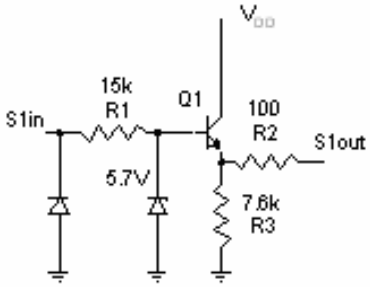


Timing diagram



Testing schem

Logical blokes

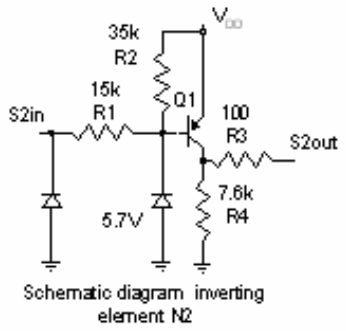


Schematic diagram
noinverting element N1

Functional table

Input S1in	Output S1out
H	H
L	L
Open	L

- for MICOM Input
- IGN Sensing
- TAIL Light Sensing

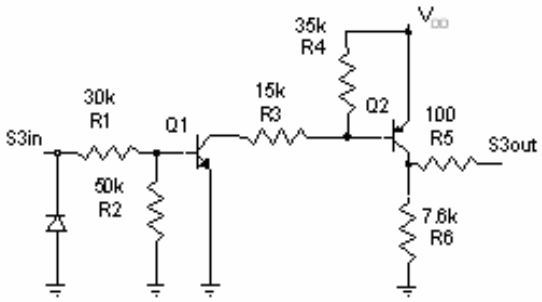


Schematic diagram inverting element N2

Functional table

Input S2in	Output S2out
H	L
L	H
Open	L

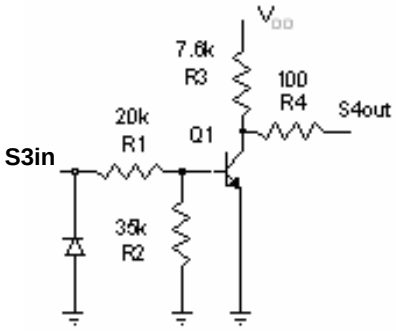
- for MICOM Input
- for (-) CONTROL



Schematic diagram noinverting element N3

Functional table

Input S3in	Output S3out
H	H
L	L
Open	L

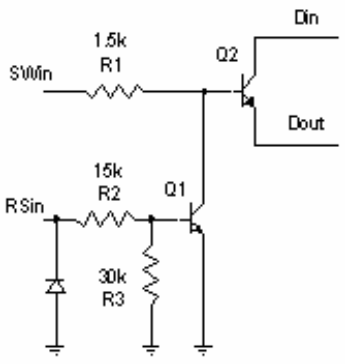


Schematic diagram inverting element N4

Functional table

Input S3in	Output S4out
H	L
L	H
Open	H

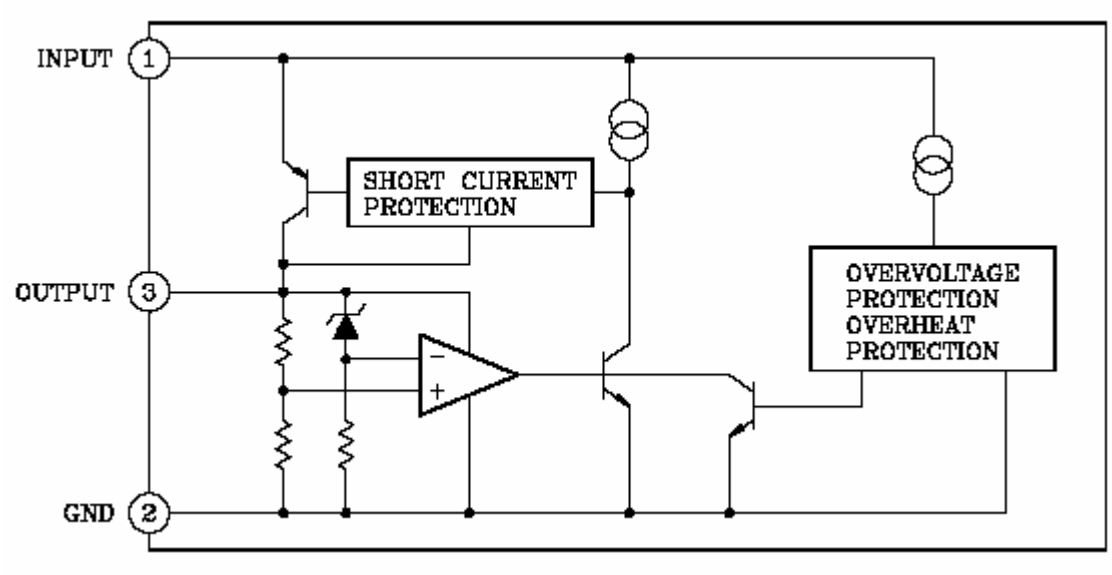
- for MICOM Input
- for SPEED Input



Schematic diagram modulation part

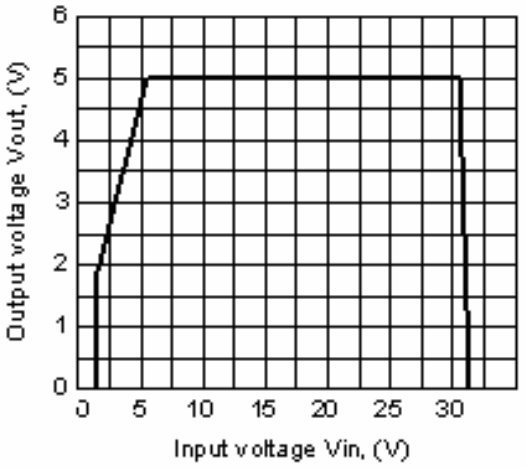
Functional table

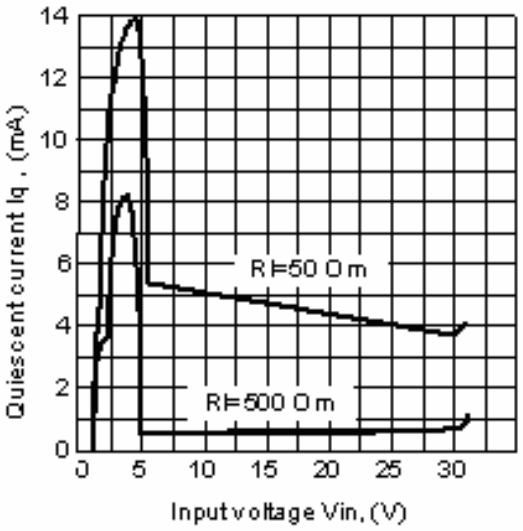
Input RSin	Input SWin	Output Dout	Output Din
H	H	GND	H
L	H	GND	L
H	L	GND	H
L	L	GND	H
Open	H	GND	L
Open	L	GND	H

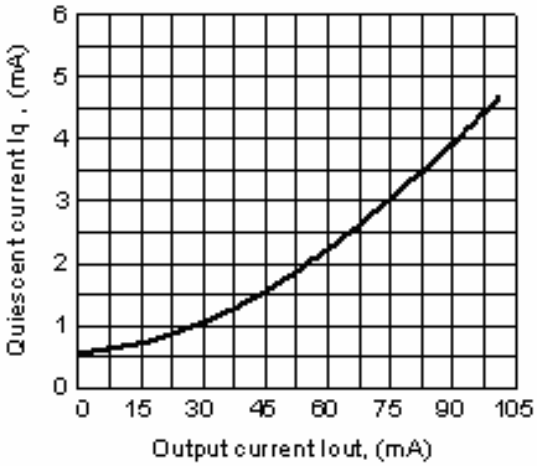


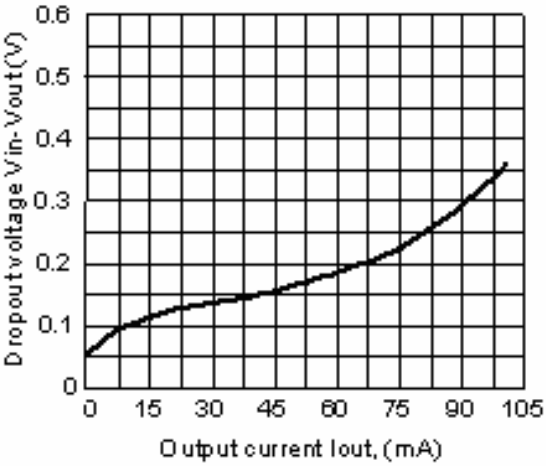
Voltage Regulator Schematic

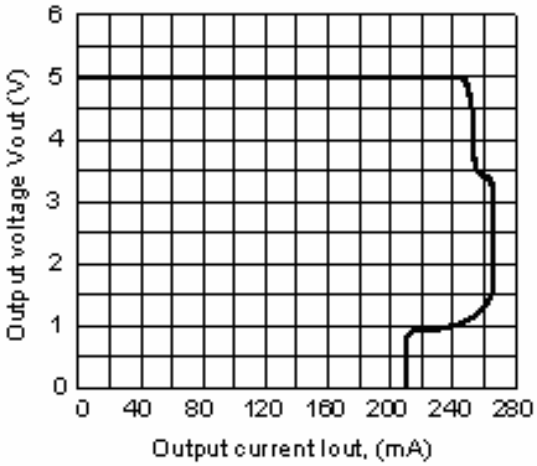
Typical characteristics

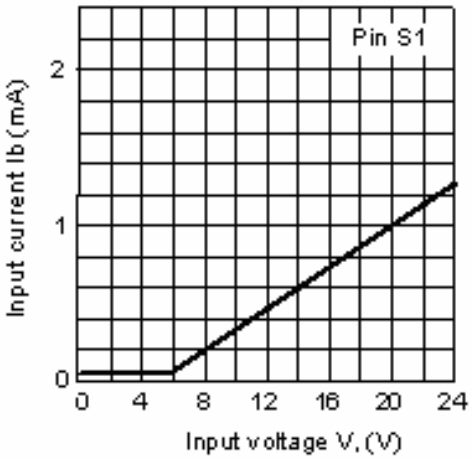


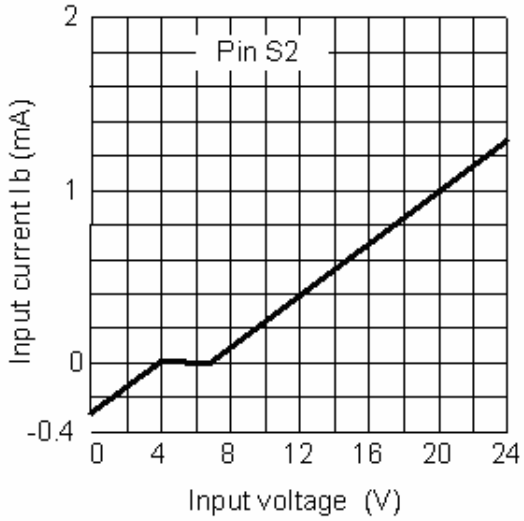


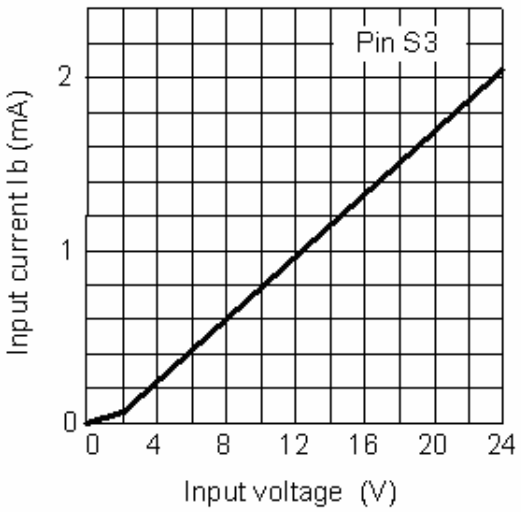


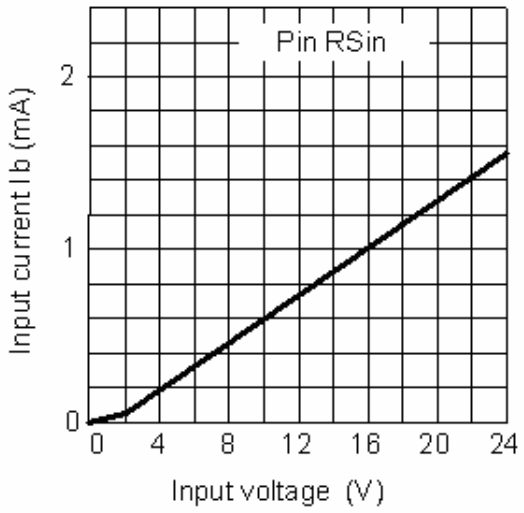


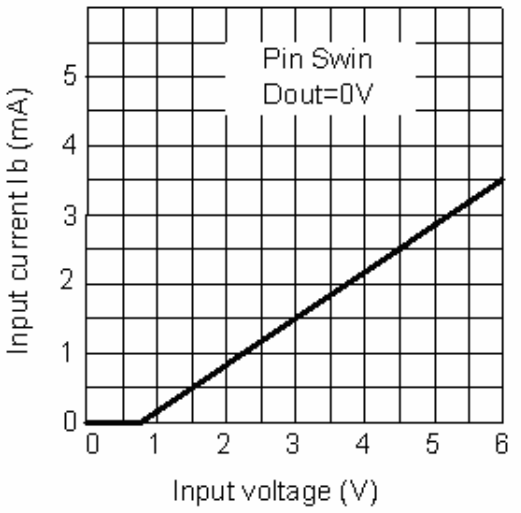


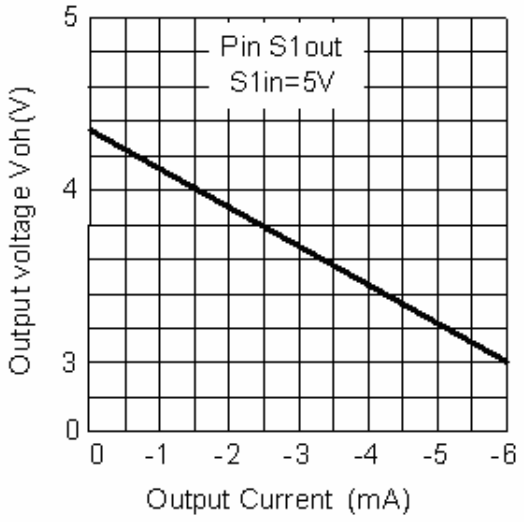


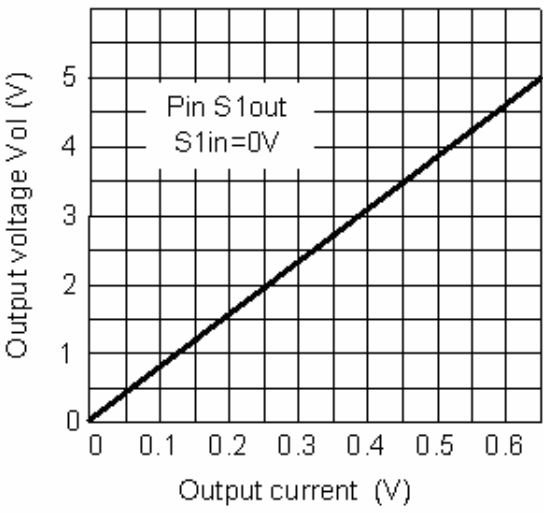

Pin S2
Input current Ib (mA)
2
1
0
-0.4
0 4 8 12 16 20 24
Input voltage (V)

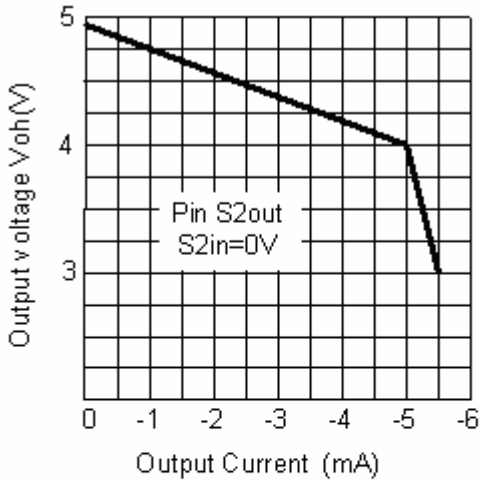

Pin S3
Input current Ib (mA)
2
1
0
0 4 8 12 16 20 24
Input voltage (V)

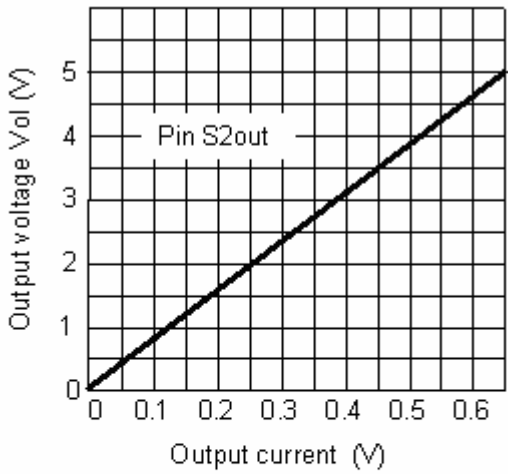

Pin RSin
Input current Ib (mA)
2
1
0
0 4 8 12 16 20 24
Input voltage (V)

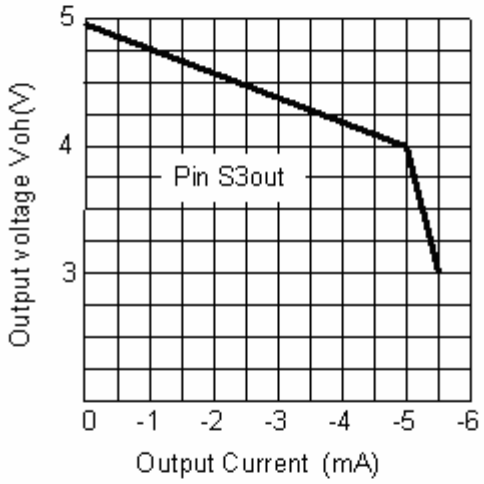

Pin Swin
Dout=0V
Input current Ib (mA)
5
4
3
2
1
0
0 1 2 3 4 5 6
Input voltage (V)

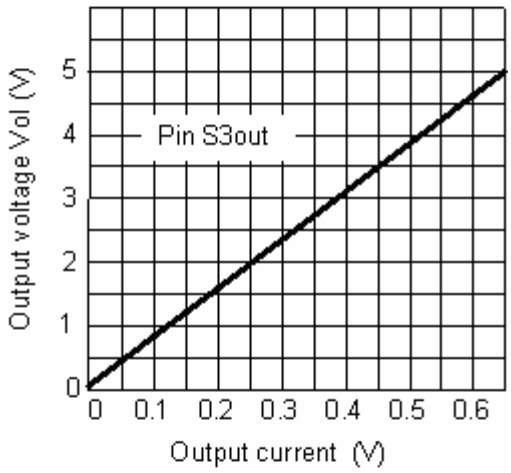

Pin S1out
S1in=5V
Output voltage Voh (V)
5
4
3
0
0 -1 -2 -3 -4 -5 -6
Output Current (mA)

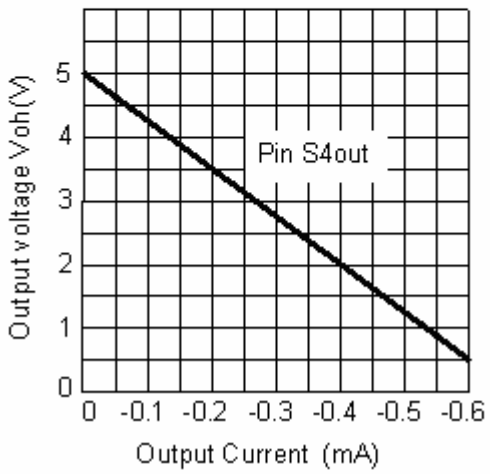

Pin S1out
S1in=0V
Output voltage Vol (V)
5
4
3
2
1
0
0 0.1 0.2 0.3 0.4 0.5 0.6
Output current (V)

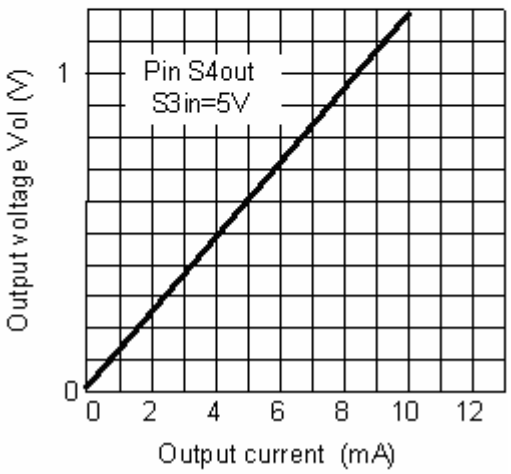

Output voltage Voh(V)
5
4
3
Pin S2out
S2in=0V
0 -1 -2 -3 -4 -5 -6
Output Current (mA)

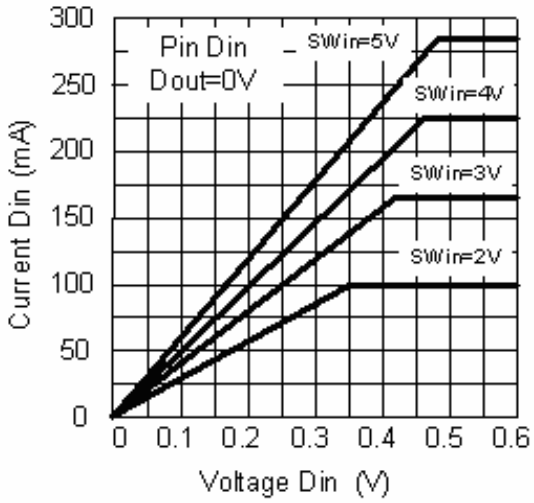

Output voltage Vol (V)
5
4
3
2
1
0
Pin S2out
0 0.1 0.2 0.3 0.4 0.5 0.6
Output current (V)

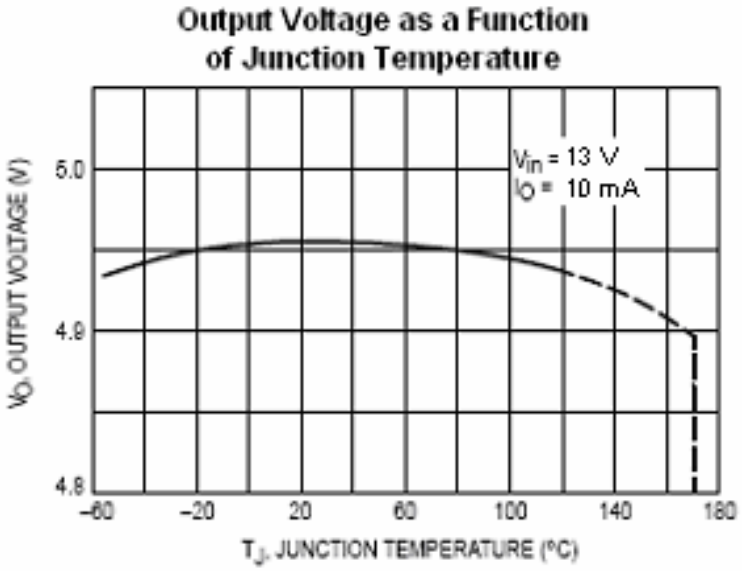

Output voltage Voh(V)
5
4
3
Pin S3out
0 -1 -2 -3 -4 -5 -6
Output Current (mA)


Output voltage Vol (V)
5
4
3
2
1
0
Pin S3out
0 0.1 0.2 0.3 0.4 0.5 0.6
Output current (V)


Output voltage Voh(V)
5
4
3
2
1
0
Pin S4out
0 -0.1 -0.2 -0.3 -0.4 -0.5 -0.6
Output Current (mA)

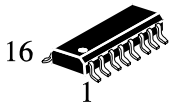

Output voltage Vol (V)
1
0
Pin S4out
S3in=5V
0 2 4 6 8 10 12
Output current (mA)

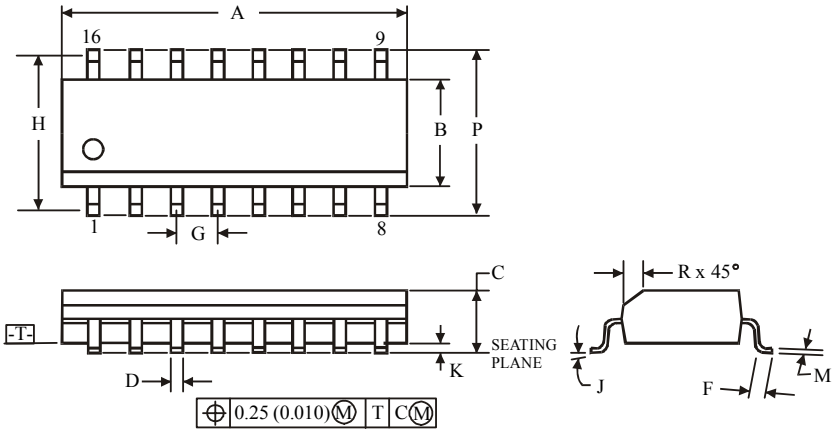

Pin Din
Dout=0V
SWin=5V
SWin=4V
SWin=3V
SWin=2V
Current Din (mA)
Voltage Din (V)
300
250
200
150
100
50
0
0 0.1 0.2 0.3 0.4 0.5 0.6


Output Voltage as a Function of Junction Temperature
Vin = 13 V
Io = 10 mA
VO, OUTPUT VOLTAGE (V)
5.0
4.9
4.8
−60 −20 20 60 100 140 180
TJ, JUNCTION TEMPERATURE (°C)

PKG DIMENSION

D SUFFIX SOIC
(MS - 012AC)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	9.80	10.00
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B – 0.25 mm (0.010) per side.