



# SPN7002L

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN7002L is the N-Channel enhancement mode field effect transistors are produced using high cell density DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 300mA DC and can deliver pulsed currents up to 0.8A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

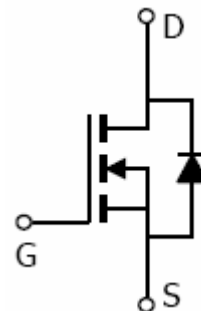
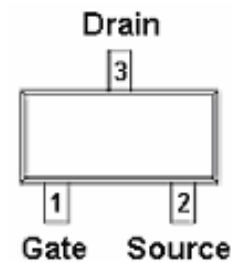
### FEATURES

- ◆ 50V/0.30A ,  $R_{DS(ON)} = 3.5\Omega @ V_{GS} = 10V$
- ◆ 50V/0.25A ,  $R_{DS(ON)} = 5.5\Omega @ V_{GS} = 4.5V$
- ◆ 50V/0.05A ,  $R_{DS(ON)} = 7.5\Omega @ V_{GS} = 2.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

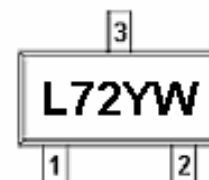
### APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- High saturation current capability. Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

### PIN CONFIGURATION(SOT-23)



### PART MARKING



**Y : Year Code**  
**W : Week Code**



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN7002LS23RG	SOT-23	L72YW

※ Week Code : A ~ Z ( 1 ~ 26 ) ; a ~ z ( 27 ~ 52 )

※ SPN7002LS23RG : Tape Reel ; Pb – Free

### ABSOLUTE MAXIMUM RATINGS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	50	V
Gate –Source Voltage - Continuous	V <sub>GSS</sub>	±20	V
Gate –Source Voltage - Non Repetitive ( t <sub>p</sub> < 50μs)	V <sub>GSS</sub>	±40	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	0.3	A
	TA=25°C		
Pulsed Drain Current (*)	I <sub>DM</sub>	0.8	A
Power Dissipation	P <sub>D</sub>	0.35	W
	TA=25°C		
Operating Junction Temperature	T <sub>J</sub>	-55 ~ 150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 ~ 150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	375	°C/W

(\*) Pulse width limited by safe operating area



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### ELECTRICAL CHARACTERISTICS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	50			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.8	1.25	1.5	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =45V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =45V, V <sub>GS</sub> =0V T <sub>J</sub> =125°C			10	
Drain-Source On-Resistance	R <sub>DSON</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.30A		2.5	3.5	Ω
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =0.25A		3.3	5.5	
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> =0.05A		5.0	7.5	
Source-drain Current	I <sub>SD</sub>				0.35	A
Source-drain Current (pulsed)	I <sub>SDM</sub> (2)				1.4	A
Forward Transconductance	G <sub>fs</sub> (1)	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.5 A		0.6		S
Diode Forward Voltage	V <sub>SD</sub> (1)	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.12A		0.85	1.5	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 5 V		1.4	2.0	nC
Gate-Source Charge	Q <sub>gs</sub>			0.8		
Gate-Drain Charge	Q <sub>gd</sub>			0.5		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		43		pF
Output Capacitance	C <sub>oss</sub>			20		
Reverse Transfer Capacitance	C <sub>rss</sub>			6		
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 0.5 A R <sub>G</sub> = 4.7Ω V <sub>GS</sub> = 4.5 V		5		ns
	t <sub>r</sub>			15		
Turn-Off Time	t <sub>d(off)</sub>			7		
	t <sub>f</sub>			8		

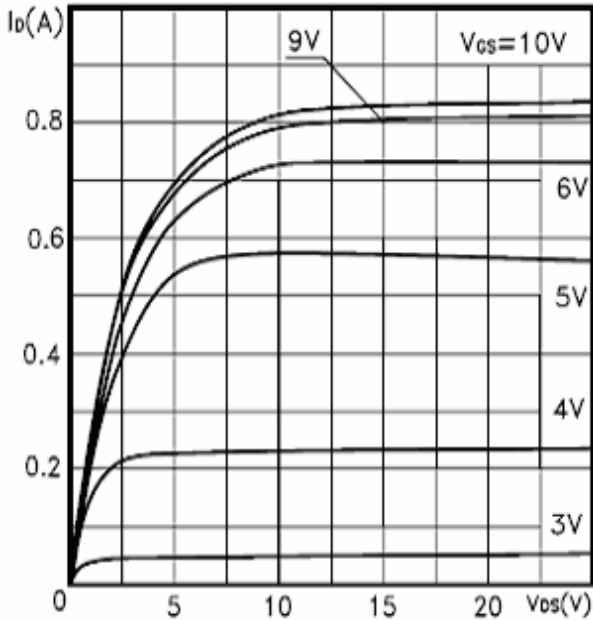
(1) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

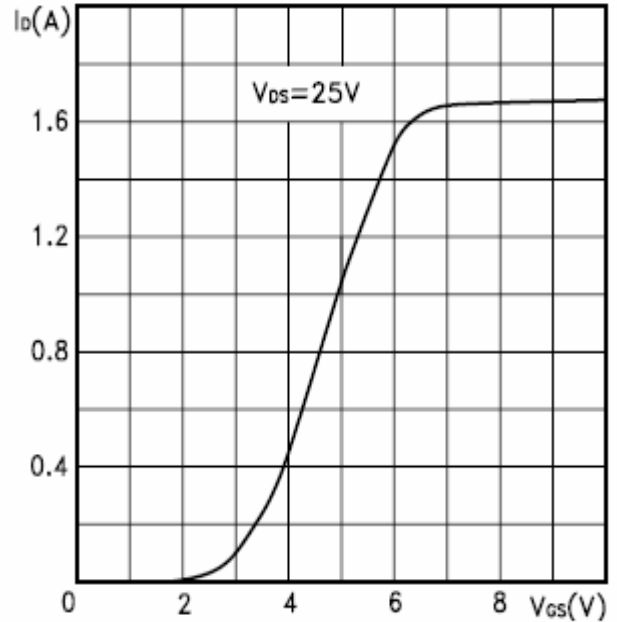


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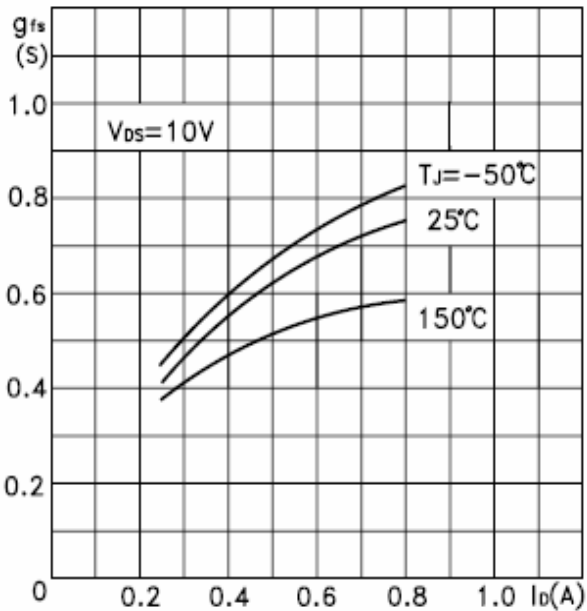
## TYPICAL CHARACTERISTICS



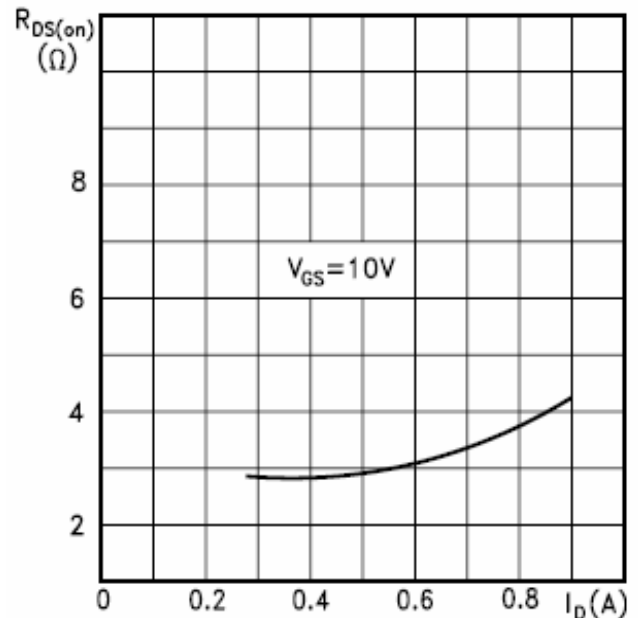
Output Characteristics



Transfer Characteristics



Transconductance



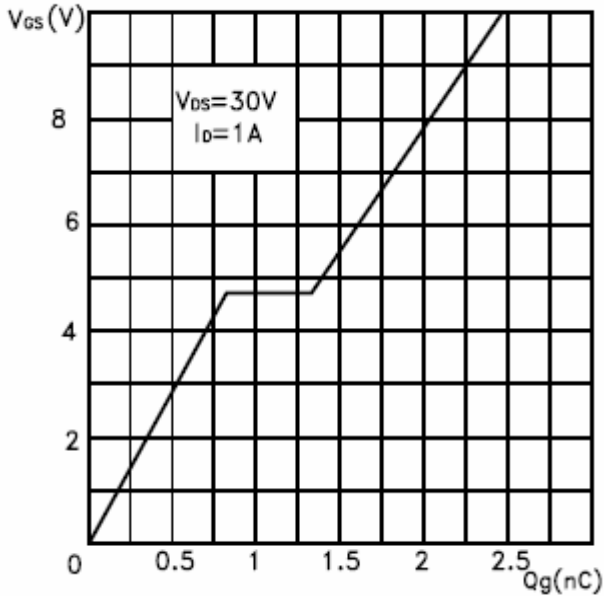
Static Drain-source On Resistance



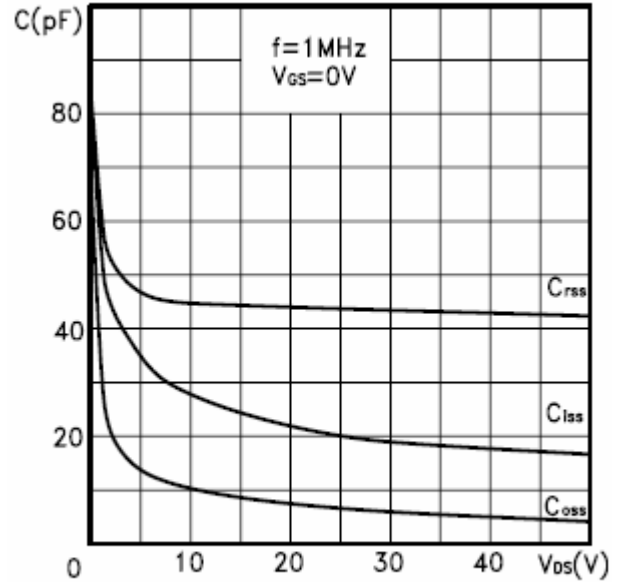
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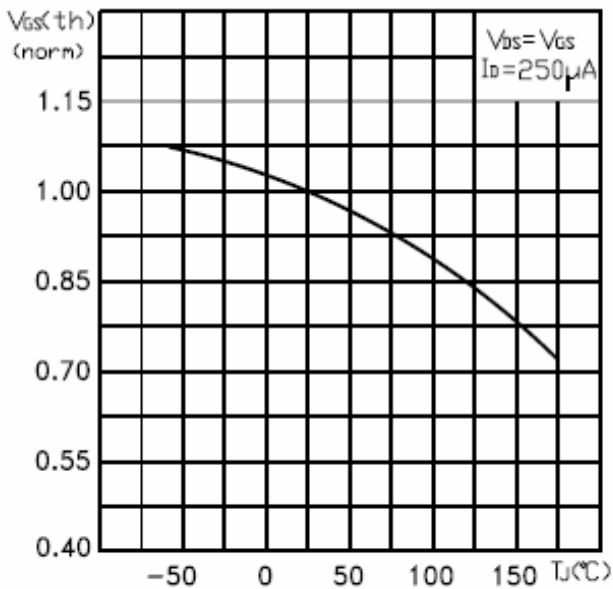
### TYPICAL CHARACTERISTICS



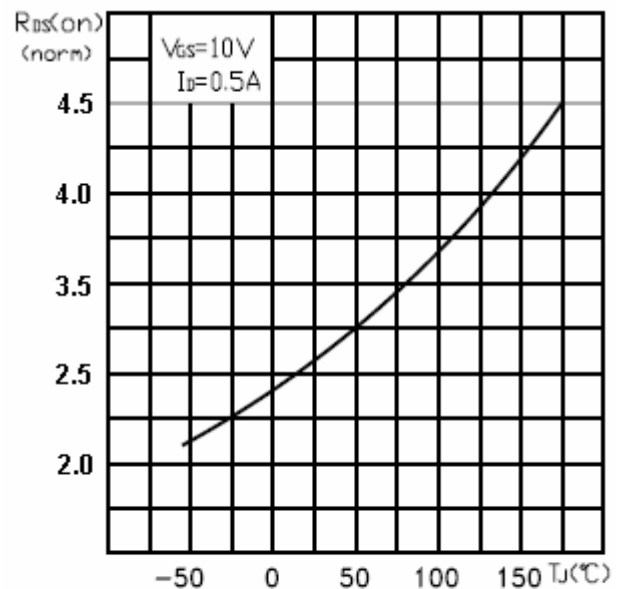
Gate Charge vs Gate-source Voltage



Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature

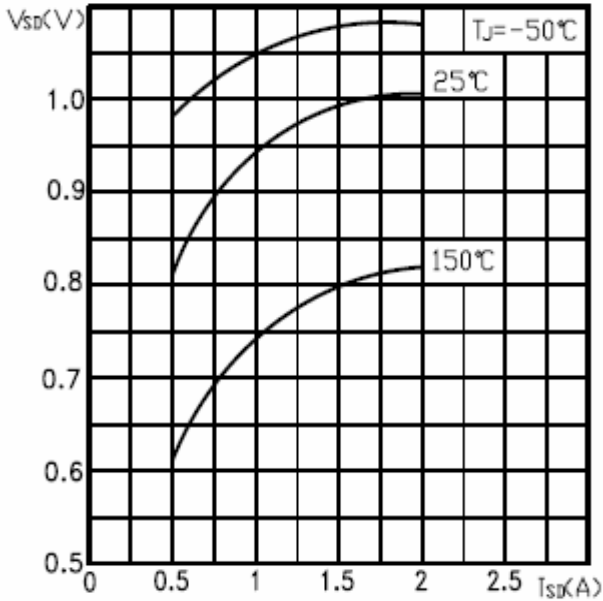


Normalized On Resistance vs Temperature

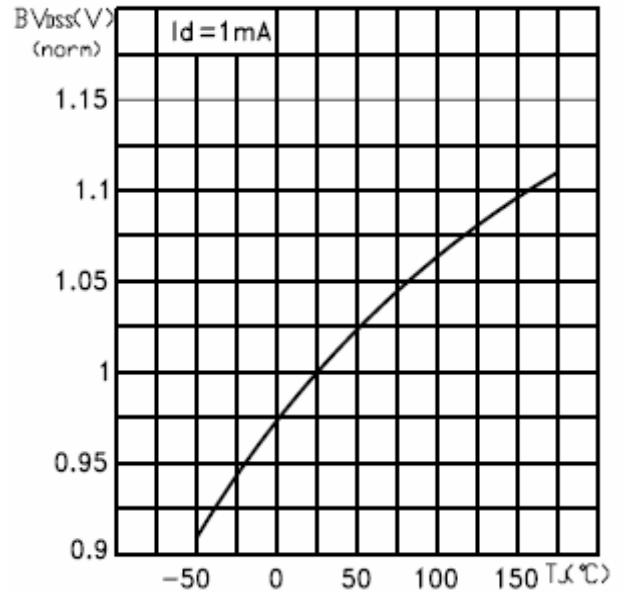


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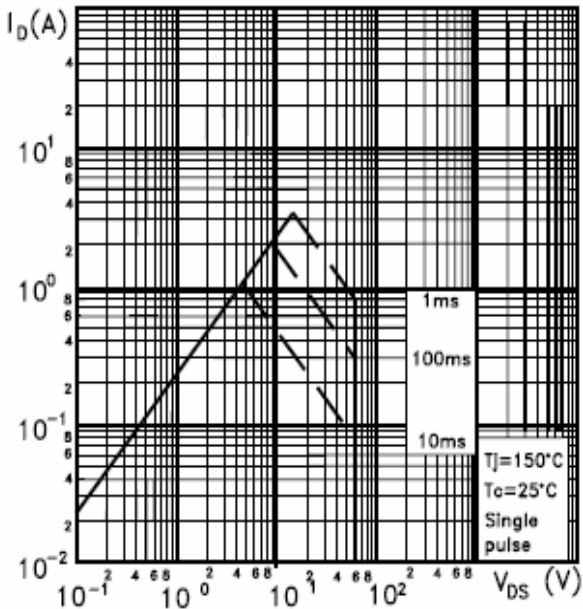
## TYPICAL CHARACTERISTICS



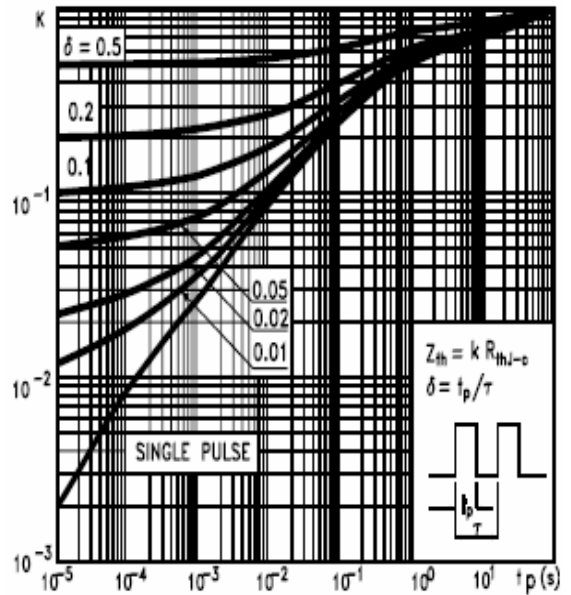
Source-Drain Forward



Normalized BVDSS vs Temperature



Safe Operating Area

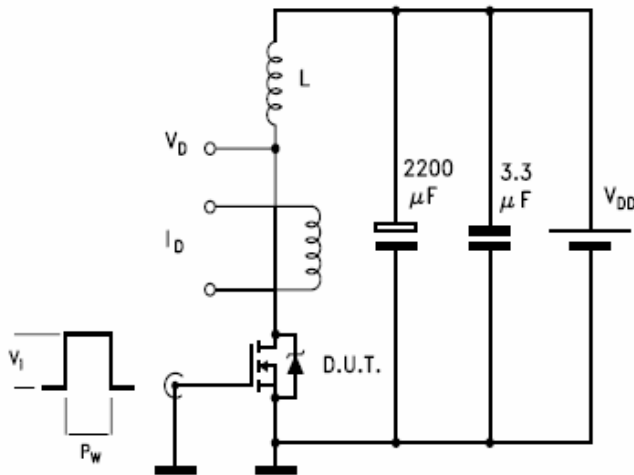


Thermal Impedance

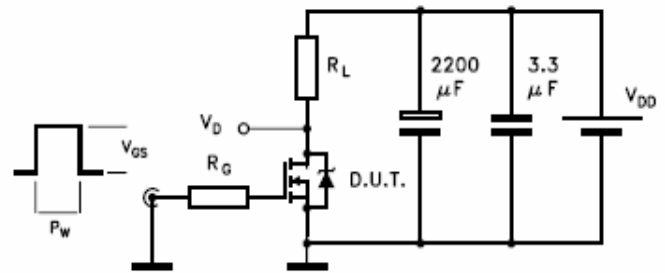


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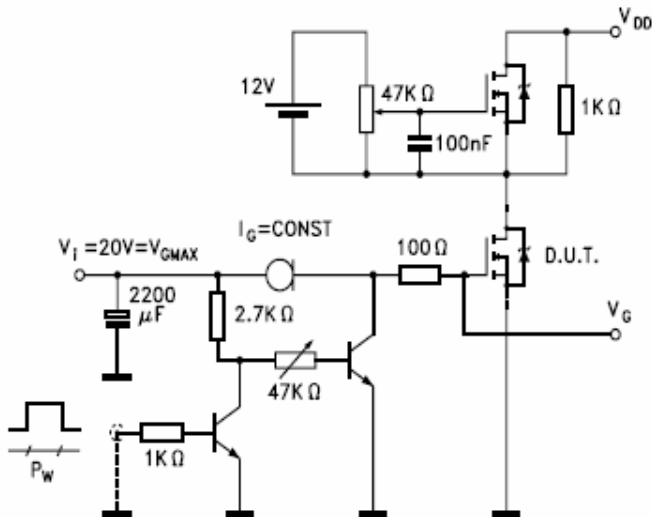
## TYPICAL TESTING CIRCUIT



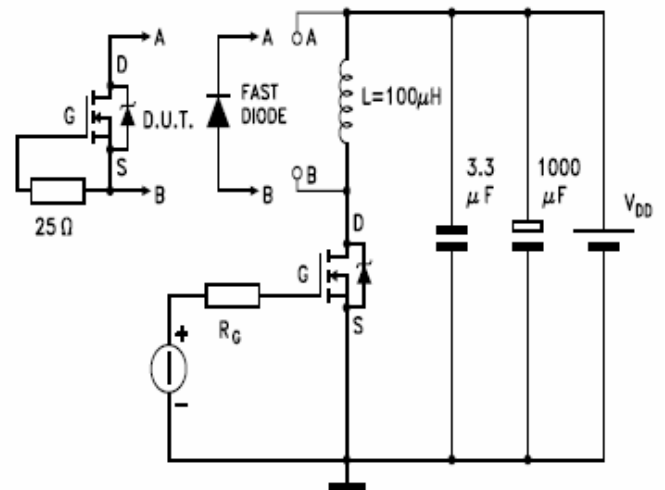
Unclamped Inductive Load Test



Switching Times Test Circuit



Gate Charge Test Circuit



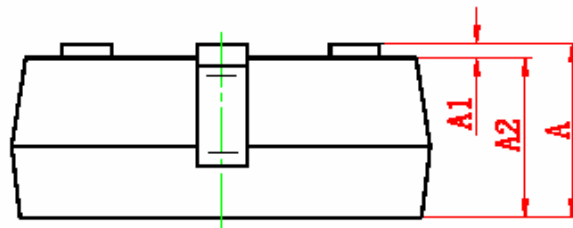
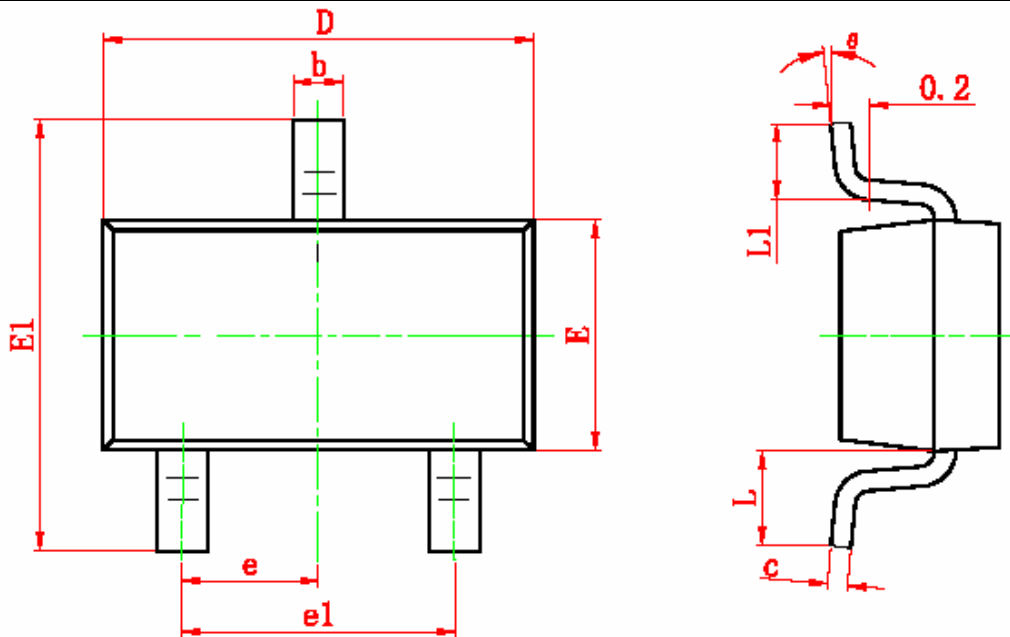
Test Circuit For Inductive Load  
Switching and Diode Recovery Times



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### SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°





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