

# M3625A 4K (1K x 4) PROM

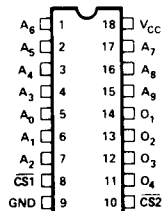
- ± 10% Power Supply Tolerance
- Fast Access Time: 60 ns Maximum
- Lower Power Dissipation: 0.14 mW/Bit Typically
- Simple Memory Expansion Two Chip Select Inputs
- Three-State Outputs
- Polycrystalline Silicon Fuse for Higher Reliability
- Hermetic 18-Pin DIP

The Intel® M3625A is a high density, 4096-bit bipolar PROM organized as 1024 words by 4 bits. The 1024 by 4 organization gives ideal word or bit modularity for memory array expansion. The M3625A is fully specified over the -55°C to 125°C temperature range with ±10% power supply variation.

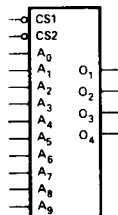
The M3625A is packaged in an 18-pin dual-in-line hermetic package with 300 milli-inch centers. Thus, twice the bit density can be achieved in the same memory board areas as 512 by 8-bit PROMs in 24-pin packages.

The highly reliable polycrystalline silicon fuse technology is used in the manufacturing of the M3625A. All outputs are initially a logical high and logic low levels can be electrically programmed in selected bit locations.

### PIN CONFIGURATION



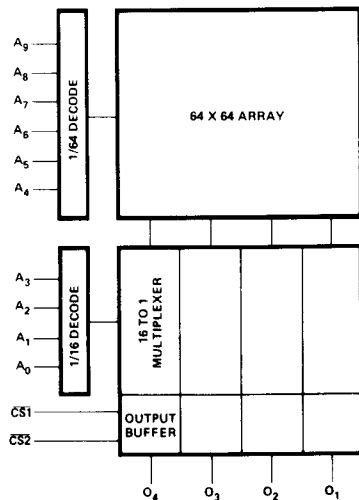
### LOGIC SYMBOL



### PIN NAMES

A <sub>0</sub> - A <sub>9</sub>	ADDRESS INPUTS
CS	CHIP SELECT INPUT
O <sub>1</sub> - O <sub>4</sub>	OUTPUTS

### BLOCK DIAGRAM



## PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions.

## Absolute Maximum Ratings\*

Temperature Under Bias	-65 °C to +135 °C
Storage Temperature	-65 °C to +160 °C
Output or Supply Voltages	-0.5V to 7V
All Input Voltages	-1V to 5.5V
Output Currents	100mA

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

**D.C. Characteristics:** All limits apply for  $V_{CC} = +5.0V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ. <sup>(1)</sup>	Max.	Unit	
$I_{FA}$	Address Input Load Current		-0.05	-0.25	mA	$V_{CC} = 5.5V$ , $V_A = 0.45V$
$I_{FS}$	Chip Select Input Load Current		-0.05	-0.25	mA	$V_{CC} = 5.5V$ , $V_S = 0.45V$
$I_{RA}$	Address Input Leakage Current			40	$\mu\text{A}$	$V_{CC} = 5.5V$ , $V_A = 5.5V$
$I_{RS}$	Chip Select Input Leakage Current			40	$\mu\text{A}$	$V_{CC} = 5.5V$ , $V_S = 5.5V$
$ I_{O} $	Output Leakage for High Impedance Stage			40	$\mu\text{A}$	$V_O = 5.5V$ or $0.45V$ , $V_{CC} = 5.5V$ , $\overline{CS}_1 = \overline{CS}_2 = 2.4V$
$I_{SC}^{(2)}$	Output Short Circuit Current	-20	-35	-80	mA	$V_O = 0V$
$V_{CA}$	Address Input Clamp Voltage		-0.9	-1.5	V	$V_{CC} = 4.5V$ , $I_A = -10\text{mA}$
$V_{CS}$	Chip Select Input Clamp Voltage		-0.9	-1.5	V	$V_{CC} = 4.5V$ , $I_S = -10\text{mA}$
$V_{OH}$	Output High Voltage	2.4			V	$I_{OH} = -2.4\text{mA}$ , $V_{CC} = 4.5V$
$V_{OL}$	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.5V$ , $I_{OL} = 10\text{mA}$
$I_{CC}$	Power Supply Current		110	140	mA	$V_{CC} = 5.5V$ , $V_{A0} \rightarrow V_{A9} = 0V$ , $\overline{CS}_1 = \overline{CS}_2 = V_{IH}$
$V_{IL}$	Input "Low" Voltage			0.85	V	$T_A = 25^\circ\text{C}$
$V_{IH}$	Input "High" Voltage	2.0			V	$T_A = 25^\circ\text{C}$

## NOTES:

- Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltages.
- Unmeasured outputs are open during this test.

**A. C. Characteristics:**  $V_{CC} = +5.0V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Symbol	Parameter	Max. Limits	Unit	Conditions
$t_{A++}$ , $t_{A--}$ $t_{A+-}$ , $t_{A-+}$	Address to Output Delay	60	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ to select the PROM.
$t_{S++}$	Chip Select to Output Delay	35	ns	
$t_{S--}$	Chip Select to Output Delay	35	ns	

**Capacitance**  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ .

Symbol	Parameter	Limits		Unit	Test Conditions	
		Typ.	Max.			
$C_{INA}$	Address Input Capacitance	3	8	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
$C_{INS}$	Chip Select Input Capacitance	4	8	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
$C_{OUT}$	Output Capacitance	5	10	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

**NOTES:**

1. This parameter is only periodically sampled and is not 100% tested.

**Switching Characteristics****Conditions of Test:**

Input pulse amplitudes — 2.5V

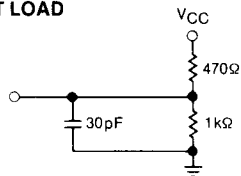
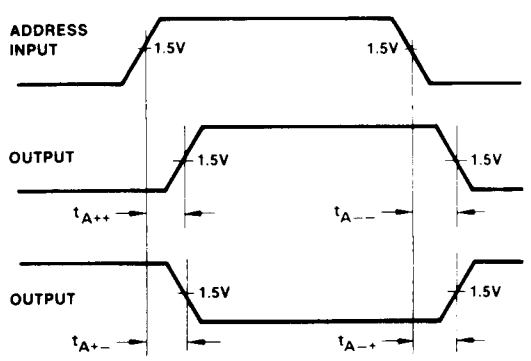
Input pulse rise and fall times of

5 nanoseconds between 1V and 2V

Speed measurements are made at 1.5V levels

Output loading — 10mA and 30pF

Frequency of test — 2.5MHz

**10 mA TEST LOAD****Waveforms****ADDRESS TO OUTPUT DELAY****CHIP SELECT TO OUTPUT DELAY**