General Description

The PMD-100 HDCD® Process Decoder is a sophisticated 0.6 micron CMOS Integrated Circuit that performs precise decoding of HDCD encoded recordings. The Decoder also functions as a state-of-the-art digital filter when fed data from non-HDCD recordings. It is designed to interface directly with popular data receivers and DAC's, eliminates the need for conventional monolithic digital filters. The PMD-100 has been carefully designed to maximize performance and ease of use in a wide variety of applications.

HDCD Process Information

Data encoded with HDCD process information carries precisely encrypted signals, hidden within the LSB of the 16-bit data word. Over time, only 1 to 5% of the LSB is used for this hidden code. The encoded information is inaudible and causes no perceptible loss of information. The PMD-100 recognizes the encrypted signals as HDCD process information, and directs the decoding function to precisely reconstruct the high resolution signal in a form appropriate for output to the D-A converter being used.

Note: *To preserve HDCD process information, no alteration of the encoded data is allowed prior to processing by the PMD-100. Digital data processing including phase inversion prior to the PMD-100 input will result in the loss of HDCD process information encoded in the data.*

SPECIAL FEATURES

Automatic HDCD Process Decoding

When the PMD-100 detects HDCD® process information in the input data, it automatically switches to HDCD® decode mode, and provides an output to drive an LED indicator. When non-HDCD® process input data is received, the decoder automatically operates as a high performance digital filter.

Excellent Filter Characteristics

When operating as a digital filter, the PMD-100 exhibits passband characteristics that have been carefully optimized to provide extremely accurate sound quality. Passband ripple from 0 to 20 kHz is within ±.0001 dB and stopband attenuation is greater than 120 dB.

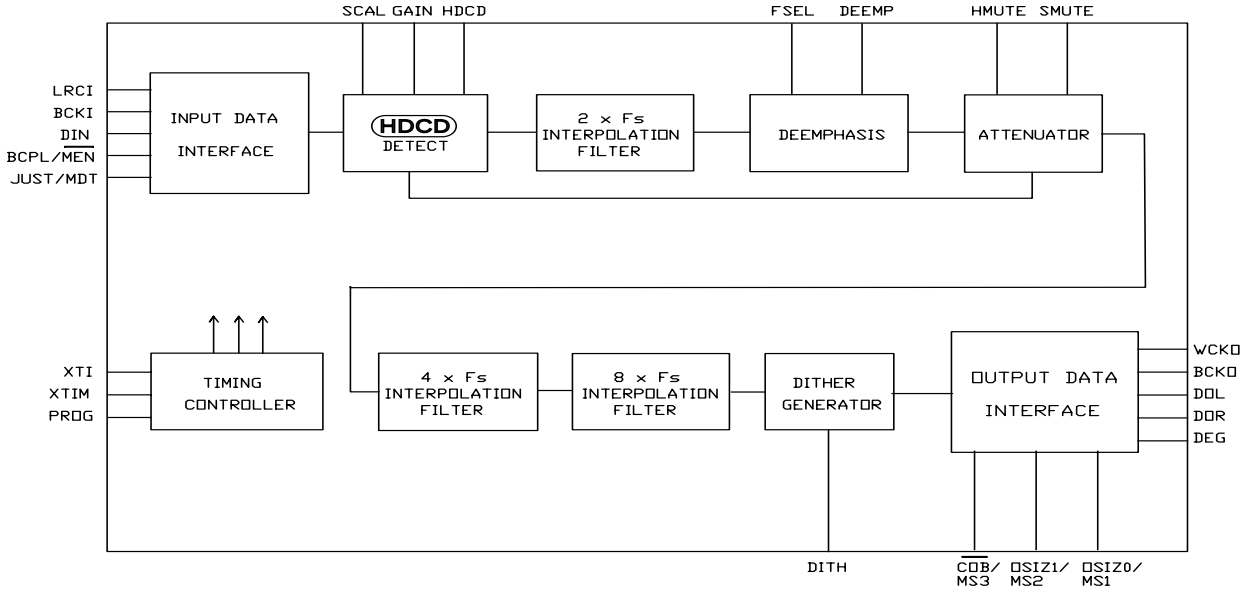
Two Operating Modes

Stand-Alone

In Stand-Alone Mode, the PMD-100 requires no external controller, allowing for the most cost effective designs.

Program

In Program mode, an external processor controls the PMD-100's many advanced operating modes and features.



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SPECIAL FEATURES (Cont.)

DAC Optimize Operating Modes

To achieve the best possible performance from a variety of different DAC types, adjustable parameters are provided including eight different levels of dither and Patented "Silent Conversion" variable clock timing.

Constant Clock Output

The PMD-100 constantly provides output clocking to the DAC, even if input data and master clocks are lost. This feature eliminates the possiblility of spikes or DC offsets at the DAC's output.

Additional Features

- *24 bit or greater accuracy provided for all operations.*
- *Up to 24 bit input data passed without truncation.*
- *32 kHz to 55 kHz input data rates.*
- *Output digital attenuation over a 96 dB range in 0.188 dB steps.*
- *Output soft mute and hard mute functions.*
- *16, 18, 20 or 24 bit output data.*
- *8 Fs, 4 Fs or 2 Fs output data rates. (Multiple output data rates are provided to allow flexible DAC operation and ease of use in designs that employ custom DSP based filters for non-HDCD® process recordings.)*
- *Digital domain deemphasis.*
- *256 Fs or 384 Fs system clock.*

DC Specifications

Electrical

Digital Characterisitcs V_{DD} = 4.75V to 5.25V, V_{SS} = OV, T_A = 0°C to +70°C unless otherwise specified.

PARAMETER	PIN	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INPUT							
Logic Family					CMOS		
Logic Voltage	XTI	V_{IL}				$0.3V_{DD}$	V
	XTI	V_{IH}		$0.7V_{DD}$			V
	OTHER INPUTS	V_{IL}				0.5	V
	OTHER INPUTS	V_{IH}		2.4			V
Input Leakage Curent	XTI	I_{LH}	$V_{IN} = V_{DD}$		10	20	µA
	XTI	I_{LL}	V_{IN} = OV		10	20	µA
	OTHER INPUTS	I_{LH}	$V_{IN} = V_{DD}$			1	µA
Input Current	OTHER INPUTS	I_{IL}	V_{IN} = OV		10	20	µA
OUPUT							
Logic Family					CMOS		
Logic Voltages	ALL OUTPUTS	V_{OL}	I_{OL} = 1.6mA			0.4	V
	ALL OUTPUTS	V_{OH}	I_{OH} = -0.4mA	2.5			V
Power Supply Requirements							
Supply Voltage		V_{DD}		4.75	5	5.25	V
Supply Current		I_{DD}	V_{DD} = 5V			110	mA
Power Dissipation		P_D	NOMINAL V_{DD}			550	mW

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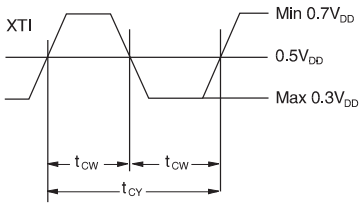
AC Specifications

Electrical

V_{DD} = 4.75V to 5.25V, V_{SS} = OV, T_A = 0°C to +70°C unless otherwise specified.

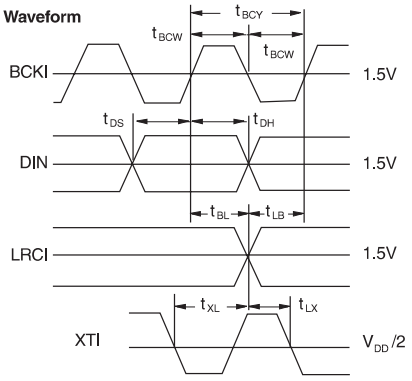
PARAMETER	SYMB	CONDITION XTIM	CONDITION x fs	XTI MIN	XTI MAX	UNITS
EXTERNAL CLOCK						
Clock Pulse Width	t_{CW}	H	384	18	54	ns
	t_{CW}	L	256	21	80	ns
Clock Period	t_{CY}	H	384	47	81	ns
	t_{CY}	L	256	70	122	ns
NOTES: (1) fs = sampling frequency						

Timing Waveform



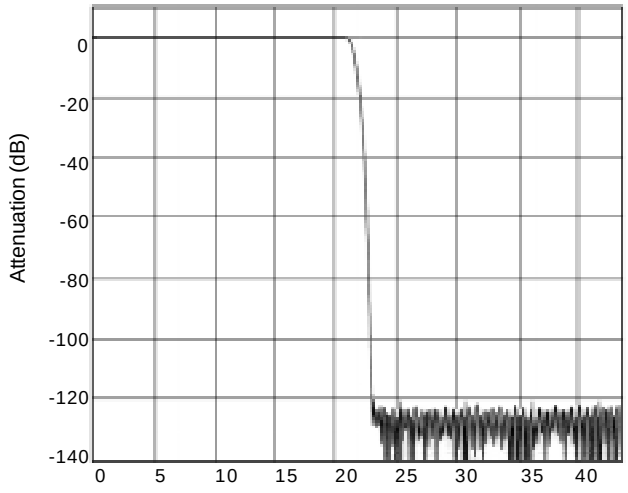
PARAMETER	SYMB	MIN	UNITS
INPUT TIMING (BCKI, DIN, LRCI,XTI)			
BCKI, Pulse Width	t_{BCW}	140	ns
BCKI, Cycle Time	t_{BCY}	280	ns
DIN, Setup Time	t_{DS}	15	ns
DIN, Hold Time	t_{DH}	20	ns
Rising Edge of Last BCKI To Edge of LRCI	t_{BL}	20	ns
Edge of LRCI To Rising Edge of First BCKI	t_{LB}	15	ns
Falling Edge of XTI To Edge of LRCI	t_{XL}	25	ns
Edge of LRCI To Falling Edge of XTI	t_{LX}	0	ns

Timing Waveform



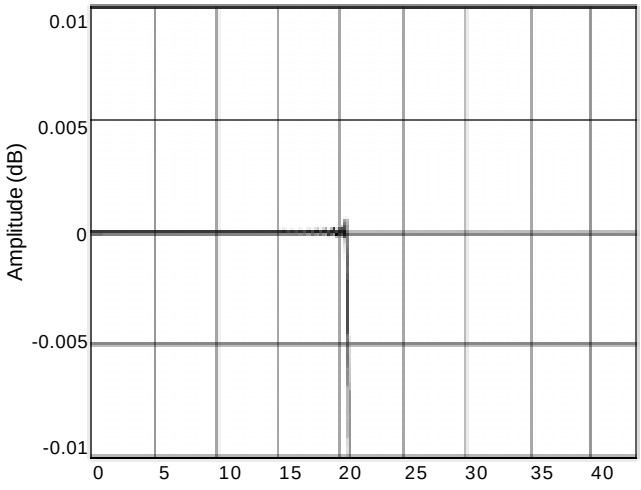
Stopband Response

Frequency kHz at 44.1 kHz sampling



Passband Response

Frequency kHz at 44.1 kHz sampling



Pin Description (Stand-Alone Mode) - Pin 9 Low

(I = Input, O = Output. All input levels TTL compatible except XTI which must be CMOS level. No inputs have pull-ups. All outputs are full CMOS levels.)

1: DIN (I) Serial data input.
2: BCKI (I) Bit clock input.
3: XTIM (I) Select system clock frequency.
Low = 256 Fs, High = 384 Fs.
4: DITH (I) Dither select.
Low = dither disabled,
High = dither added.
5: GAIN (O) Analog output stage gain.
Use only if Pin 19 is High (see page 14).
Low = low gain,
High = high gain (+6 dB).
(See pin 19 description).
6: XTI (I) System clock input.
7: VDD1 +5 volt power for filter.
8: VSS1 Ground
9: PROG(I) Select Program mode.
Low = Stand-Alone,
High = Program.

Note: Pins 10 through 14 perform different functions depending on whether Stand-Alone or Program mode is selected.

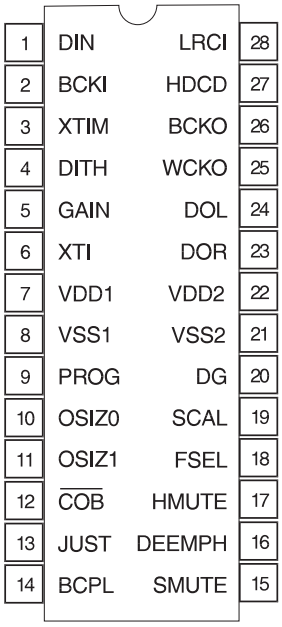
Stand-Alone Mode:

16 Bits	18 Bits	20 Bits	24 Bits
0	1	0	1
0	0	1	1

10: OSIZ0 (I)
11: OSIZ1 (I)

These two pins determine the output word size, as well as the number of pulses on BCKO.

12: $\overline{\text{COB}}$ (I) Output data format.
Low = complementary offset binary,
High = 2's complement.
13: JUST (I) Input data justification.
Low = data assumed to be left justi fied up to 24 bits in length,
High = data right justified 16 bits.
14: BCPL (I) Input data latching.
Low = input data latched on rising edge of BCKI. High = input data latched on falling edge of BCKI.
15: SMUTE (I) Soft mute. Low = off, High = on.
16: DEEMPH(I) De-emphasis filter.



Pin Configuration
Stand-Alone Mode

Low = off, High = on.
17: HMUTE (I) Hard mute. Low = off, High = on.
18: FSEL (I) De-emphasis filter Fs.
Low = 44.1 kHz, High = 48 kHz.
19: SCAL (I) Gain scaling.
Low = 6dB gain scaling is performed internally in the digital domain,
High = analog output gain stage is set by pin 5 GAIN. (See page 14.)
20: DG (O) DAC sample and hold deglitch signal.
21: VSS2 Ground. (Common with VSS1)
22: VDD2 +5 volt power for output interface.
23: DOR (O) Right channel serial data output.
24: DOL (O) Left channel serial data output.
25: WCKO(O) Word clock output.
26: BCKO (O) Bit clock output.
27: HDCD (O) HDCD encoding detect.
Low = no encoding. High = HDCD encoded input data. (Output current rated at 12mA.)
28: LRCI (I) Word clock input.

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Pin Description (Program Mode) - Pin 9 High

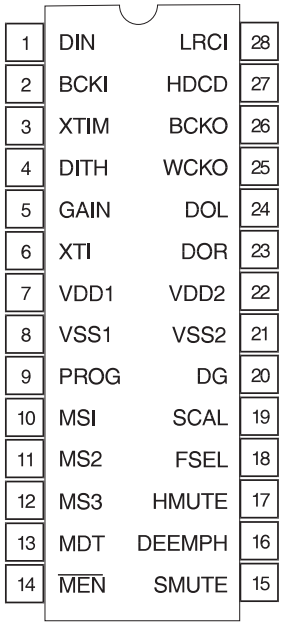
(I = Input, O = Output. All input levels TTL compatible except XTI which must be CMOS level. No inputs have pull-ups. All outputs are full CMOS levels.)

1: DIN (I) Serial data input.
2: BCKI (I) Bit clock input.
3: XTIM (I) Select system clock frequency. Low = 256 Fs, High = 384 Fs.
4: DITH (I) Dither select. Low = dither disabled, High = dither added.
5: GAIN (O) Analog output stage gain. Use only if Pin 19 is High (see page 14). Low = low gain, High = high gain (+6 dB). (See pin 19 description).
6: XTI (I) System clock input.
7: VDD1 +5 volt power for filter.
8: VSS1 Ground
9: PROG(I) Select Program mode. Low = Stand-Alone, High = Program.

Note: Pins 10 through 14 perform different functions depending on whether Stand-Alone or Program mode is selected.

Program Mode:

10: MS1 (I) Mode set bit.
11: MS2 (I) Mode set bit.
12: MS3 (I) Mode set bit.
13: $\overline{\text{MDT}}$ (I) Mode data.
14: $\overline{\text{MEN}}$ (I) Mode enable. MS1, MS2 and MS3 form eight different three bit words which select the command mode. The next rising edge on $\overline{\text{MEN}}$ activates the selected mode. Data on MDT is entered us ing the SHIFT mode (See program mode description page 11.)
15: SMUTE (I) Soft mute. Low = off, High = on.
16: DEEMPH(I) De-emphasis filter. Low = off, High = on.



Pin Configuration Program Mode

17: HMUTE (I) Hard mute. Low = off, High = on.
18: FSEL (I) De-emphasis filter Fs. Low = 44.1 kHz, High = 48 kHz.
19: SCAL (I) Gain scaling. Low = 6dB gain scaling is performed internally in the digital domain, High = analog output gain stage is set by pin 5 GAIN. (See page 14).
20: DG (O) DAC sample and hold deglitch sig nal.
21: VSS2 Ground. (Common with VSS1)
22: VDD2 +5 volt power for output interface.
23: DOR (O) Right channel serial data output.
24: DOL (O) Left channel serial data output.
25: WCKO(O) Word clock output.
26: BCKO(O) Bit clock output.
27: HDCD (O) HDCD encoding detect. Low = no encoding. High = HDCD encoded input data. (Output current rated at 12mA.)
28: LRCI (I) Word clock input.

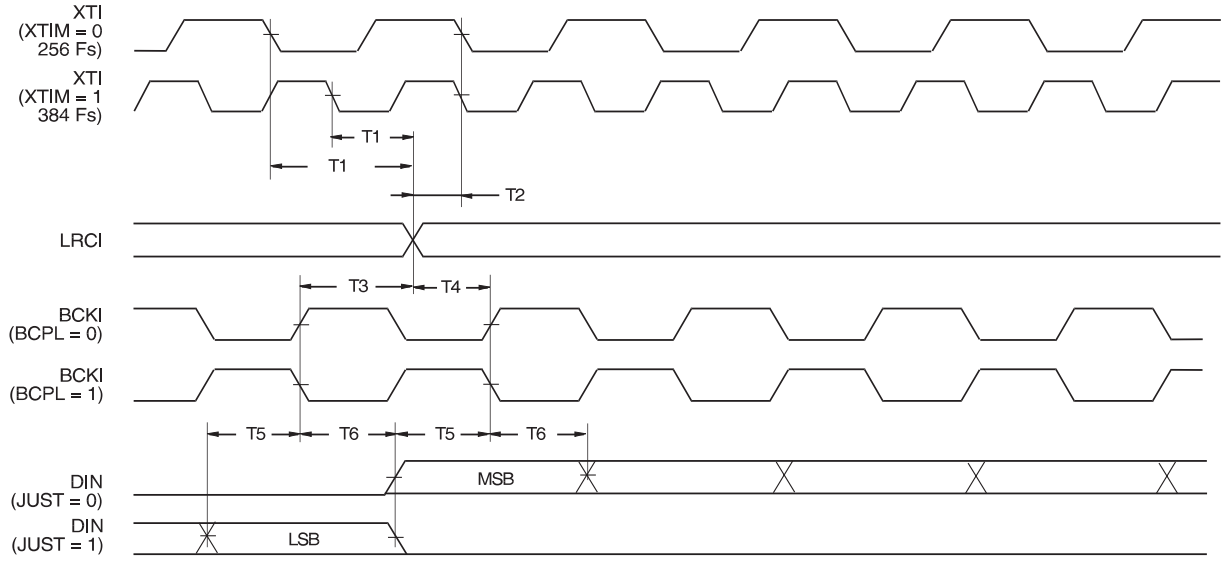
Timing Characteristics

The PMD-100 is designed as a synchronous circuit, which means that it uses a master clock input XTI which is always synchronized with and typically derived from the input data stream. The master clock frequency can be either 256 or 384 times the input sampling frequency (256 Fs or 384 Fs). If XTIM is low (XTI = 256 Fs), XTI must be between 8.192 and 14.1312 MHz with a 33 to 67% duty cycle. If XTIM is high (XTI = 384 Fs), XTI must be between 12.288 and 18.432 MHz with a 33 to 67% duty cycle, or between 18.432 and 21.1968 MHz with a 40 to 60% duty cycle. A selection of timing values are as follows:

Fs	XTI = 256 FS	Period	XTI = 384 Fs	Period
32.0 kHz	8.192 MHz	122 ns	12.288 MHz	81 ns
44.1 kHz	11.2896 MHz	88 ns	16.9344 MHz	59 ns
48.0 kHz	12.288 MHz	81 ns	18.432 MHz	54 ns
55.2 kHz	14.1312 MHz	70 ns	21.1968 MHz	47 ns

The PMD-100 constantly provides WCKO and BCKO outputs even if input data (DIN) and/or master clock (XTI) is lost. This constant clock output eliminates the possiblility of spikes or DC offsets at the DAC's output. It is recommended that if DIN or XTI are lost, hard mute (HMUTE) is enabled to prevent invalid data output. *If the chip detects a synchronization error between the master clock (XTI) and the input word clock (LRCI) it automatically exerts a hard mute internally.*

Input Detailed Timing
Stand-Alone or Programmed Mode



	MIN	MAX
T1	25 ns	
T2	0 ns	
T3	20 ns	
T4	15 ns	
T5	15 ns	
T6	20 ns	

T1 and T2 should be examined with a 'scope to ascertain compliance. If necessary, an inverter stage should be added between the PMD-100 XTI signal and the LRCI source to correct any observed error. (See Fig. 1.)

Note: that the timing diagrams display the worst case scenario and actual performance should be better.

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Data Input

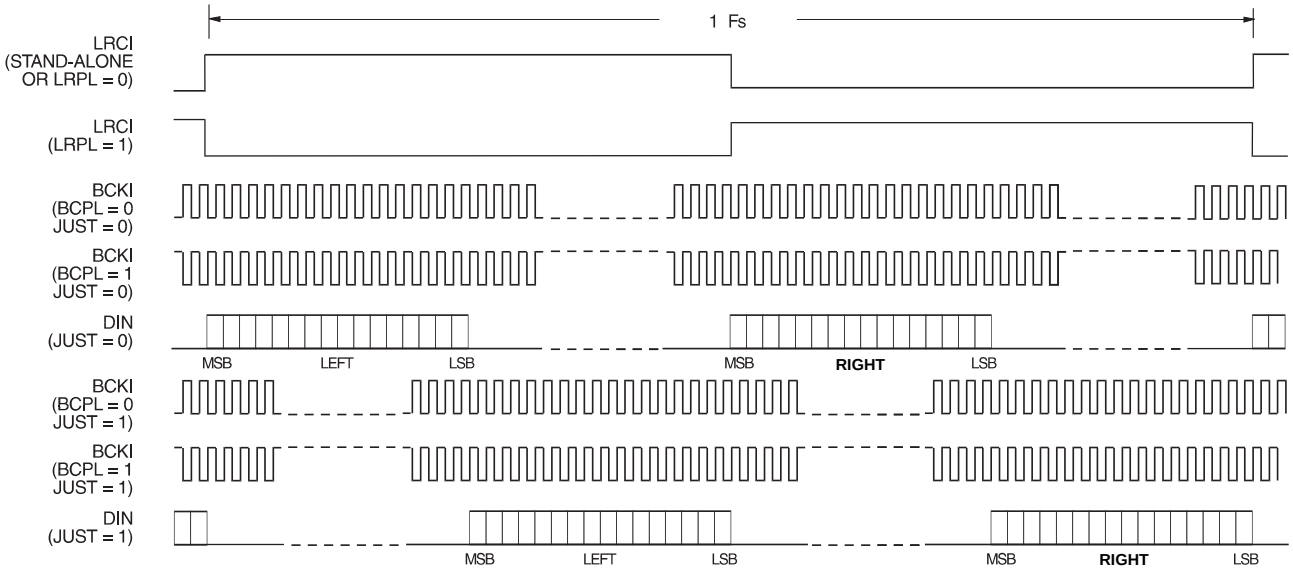
The input data word format is MSB first, 16 to 24-bit left justified or 16 bit right justified (selected by JUST).

Left and right channel data words are input alternately, with the left channel first. Refer to the Input Timing diagram below. Each serial input data bit is shifted into the serial to parallel conversion register on the rising or falling edge (selected by BCPL) of the BCKI bit clock input. The parallel data output is alternatively latched into the left and right channel input registers respectively on the rising and falling edges of the LRCI clock. The number of BCKI active edges must be 16, 18, 20, 24, or more while LRCI is low or LRCI is high. The polarity of the LRCI clock is selected by LRPL. In Stand-Alone Mode, LRPL default is low. If LRPL is low, the rising edge of LRCI indicates the start of the data input cycle. Left channel data is input while LRCI is high and latched on the falling edge. Right channel data is then input while LRCI is low, and latched on the rising edge. If LRPL is high, the clock polarity is reversed and the falling edge of LRCI indicates the start of the data input cycle.

The group (data input-to-output) delay is 83 input samples. This is measured from the active edge of LRCI preceding the input data, to the active edge of LRCI preceding the same phase output data. The group delay is the same with 2 Fs, 4 Fs or 8 Fs operation.

When the input data format is I^2S, the word clock is received one bit clock too early. A simple method for delaying the word clock for proper timing is to use a logic device to delay the word clock until it is triggered by the rising edge of the bit clock. (See Application Notes pg.s 16-20).

Input Timing
Stand-Alone or Programmed Mode



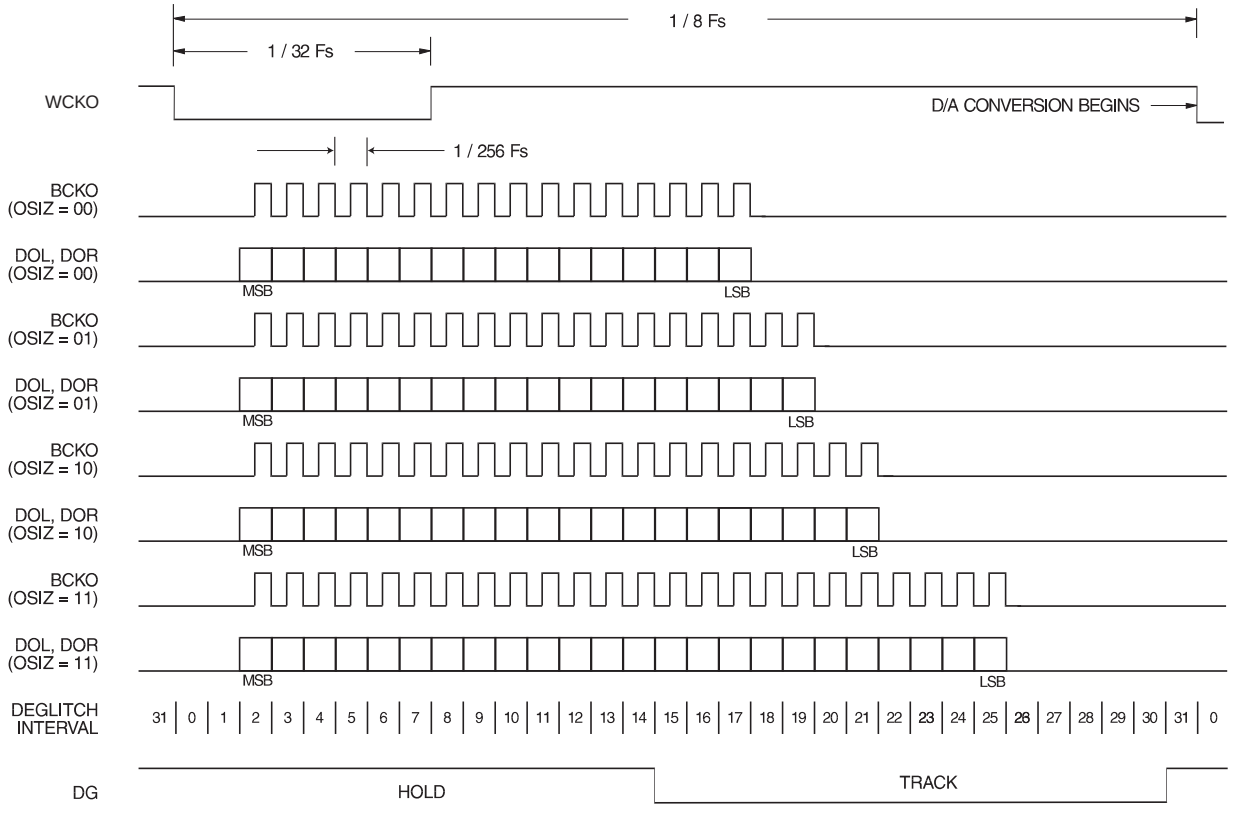
Data Output

The output data format is determined by the oversampling rate and the word length. The oversampling rate of 2 Fs, 4 Fs, or 8 Fs is selected by OVER1 and OVER0. The default in Stand-Alone Mode is 8Fs. The output word length of 16, 18, 20, or 24 bits is selected by OSIZ1 and OSIZ0. This selection also determines the number of pulses on the BCKO bit clock output. Note that if OVER0 and OVER1 are set to 2 Fs, then OSIZ0 and OSIZ1 must be set to 24 bits and DITH must be set low (dither disabled).

Refer to the Output Timing diagrams below; DOL and DOR are the left and right channel data outputs. Output data is MSB first and is selectable by $\overline{COB}$ to be either 2's complement or complementary offset binary. Data is clocked out on the falling edge and latched on the rising edge of the BCKO bit clock output. There are as many bit clock rising edges as there are output data bits. The data word start is marked by the rising or falling edge (selected by WCPL) of the word clock output WCKO. The default setting for WCKO is the falling edge. After the last bit of the data word is output, the BCKO signal is halted, and remains in this mode until WCKO changes state and the DAC initiates D/A conversion. This "Silent Conversion" minimizes conversion jitter and ground bounce by allowing time for the DAC substrate noise to settle out prior to conversion.

There are 32 deglitch intervals dividing the output sampling period. In Stand Alone Mode DG goes low at the beginning of the 15th interval and high at the beginning of the 31st interval. In Program Mode variable deglitch timing is available. The falling and rising edges can be programmed to occur at any of the 32 deglitch intervals as defined by DGL4, DGL3, DGL2, DGL1, and DGL0 (falling edge) and by DGH4, DGH3, DGH2, DGH1, and DGH0 (rising edge). (See: Program Mode).

8 Fs Output Timing
Stand-Alone Mode (PROG Pin = 0)



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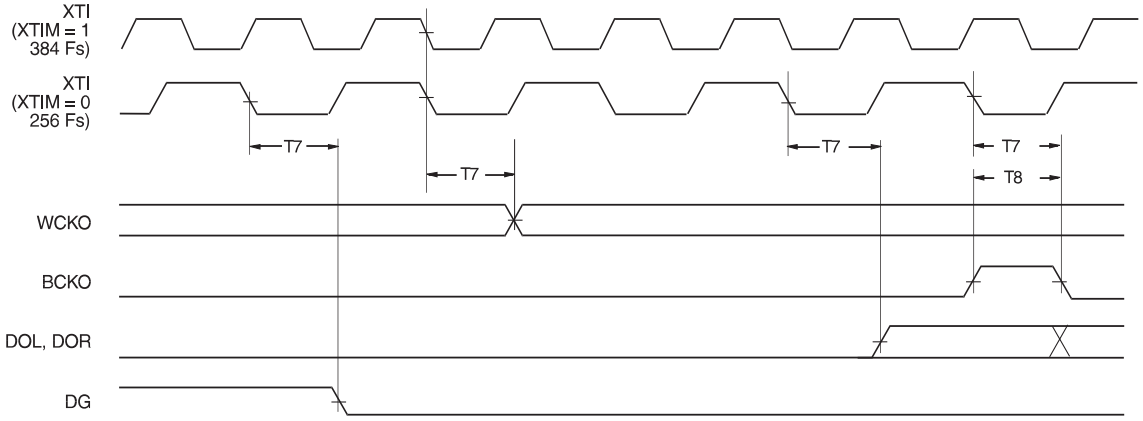
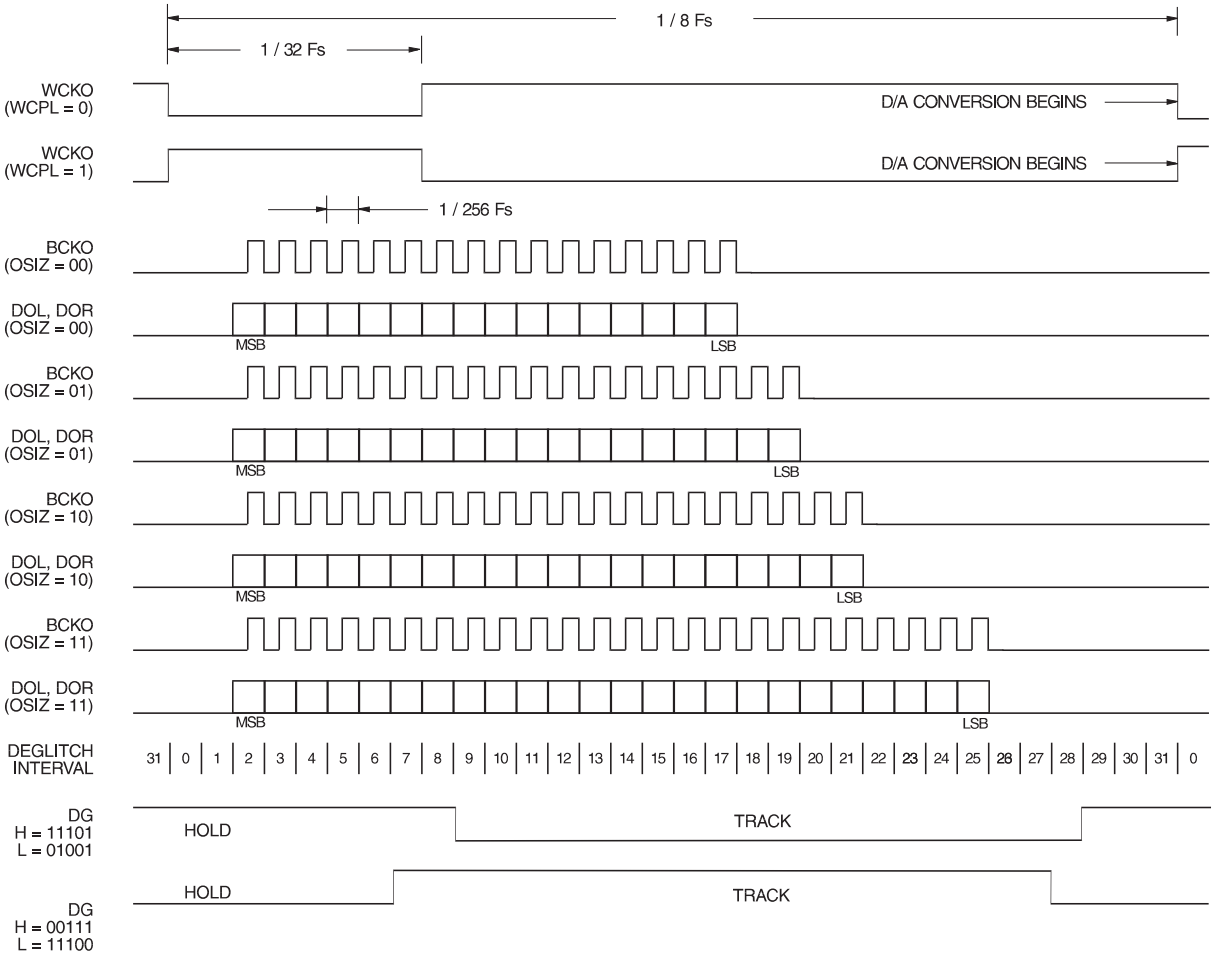
Output Detailed Timing
Stand-Alone or Programmed Mode

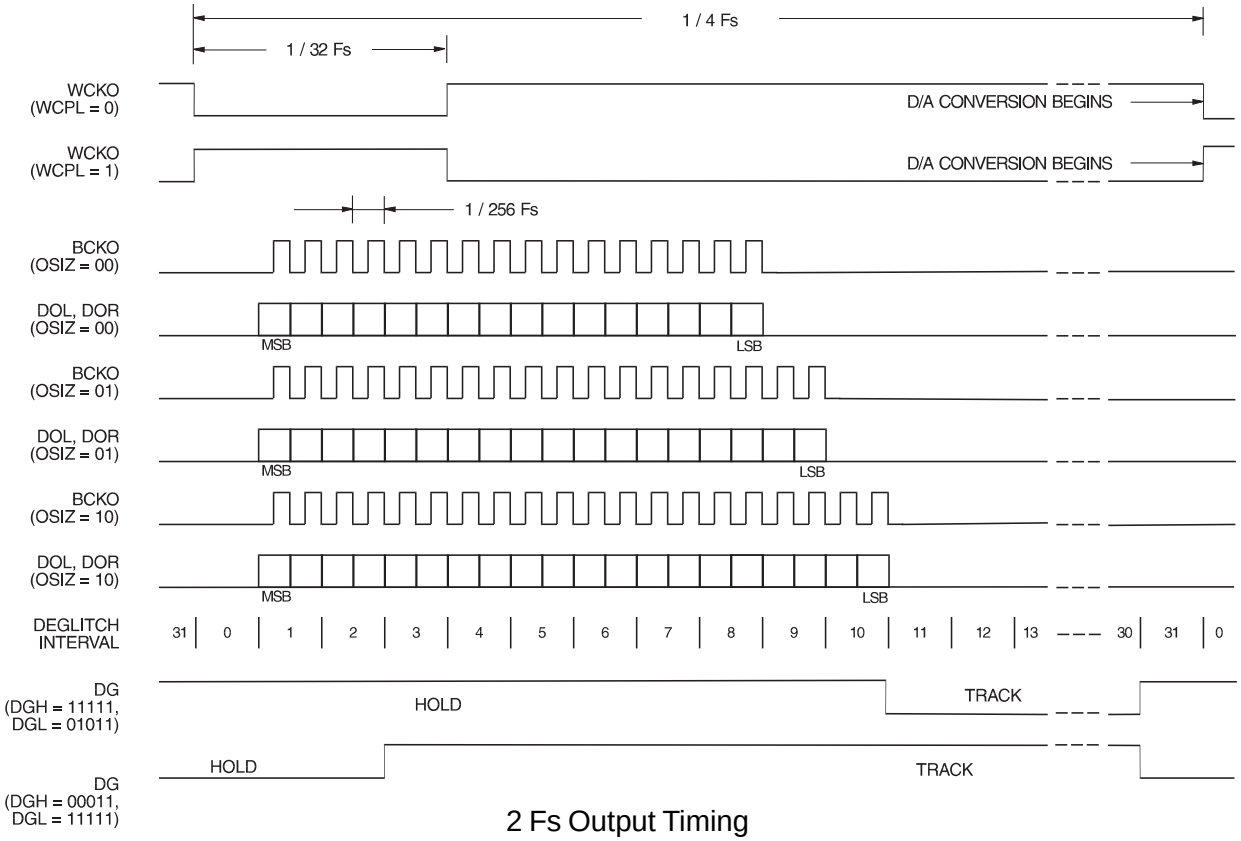


	MIN	MAX
T7	15 ns	**50** ns
T8	15 ns	

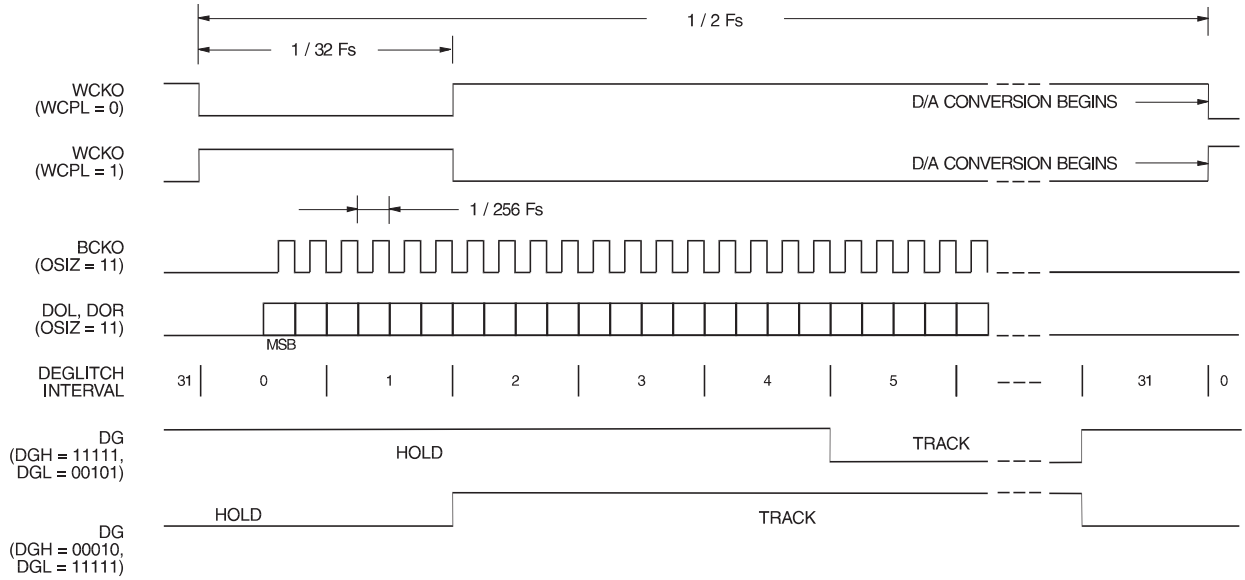
8 Fs Output Timing
Programmed Mode (PROG Pin = 1)



4 Fs Output Timing
Programmed Mode (PROG Pin = 1)



2 Fs Output Timing
Programmed Mode (PROG Pin = 1)



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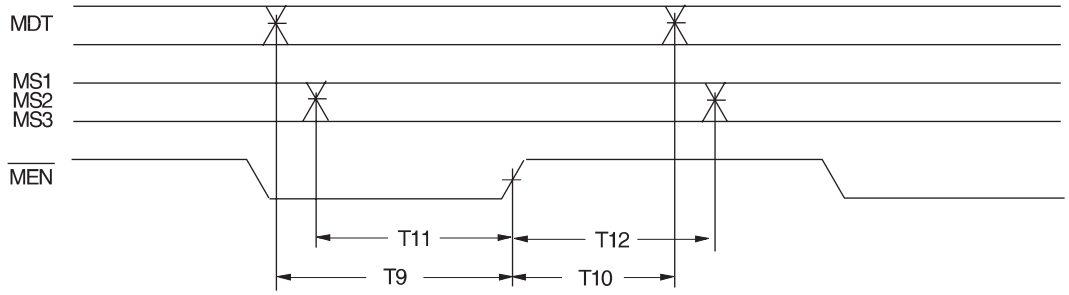
Program Mode

Important: In Program mode (PROG pin 9 high) the mode enable input clock ($\overline{\text{MEN}}$ pin 14), which enters data and commands on its rising edge, must remain high after the last command is executed, as shown in the timing diagram. Bringing it low again can cause the equivalent of a soft mute, or other anomalies.

The modes set by the three inputs MS3, MS2 and MS1 are described below: (High = 1, Low = 0).

MS3	MS2	MS1	CONTROL FUNCTION	DESCRIPTION
0	0	0	SHIFT	Causes data on MDT pin to be stored in a 24 bit shift register. Successive SHIFT instructions fill the register.
0	0	1	INCREMENT	Increments left and right attenuation registers by 0.188 dB.
0	1	0	DECREMENT	Decrements left and right attenuation registers by 0.188 dB.
0	1	1	ZERO	Sets left and right attenuation registers to zero, i.e. unity gain.
1	0	0	SET LEFT	Sets left attenuation register to the value represented by the last nine data bits entered using the SHIFT instruction (the LSB is the last entered). The value can be between 0 and 511 with a corresponding attenuation between 0 and 96.068 dB.
1	0	1	SET RIGHT	Same as SET LEFT for right attenuation register.
1	1	0	SET CONTROL	Sets control register to the value represented by the last 24 bits entered using the SHIFT instruction.
1	1	1	RESERVED	Do Not Use.

Programming Detailed Timing



	MIN	MAX
T9	15 ns	
T10	15 ns	
T11	15 ns	
T12	15 ns	

Mode Control

The 24-bit mode control flag entered on pin 13 MDT has the names and functions listed below: (Data is entered in the order listed. Multiple bit fields, such as OVER are entered LSB first (OVER0). Refer to the Mode Control Register diagram.

OVER0, OVER1:
- 00 (Not used)
- 10 Output data oversampling rate is 2 Fs.
- 01 Output data oversampling rate is 4 Fs.
- 11 Output data oversampling rate is 8 Fs.*

BCPL:
- 0 Input data is latched on BCKI rising edge.
- 1 Input data is latched on BCKI falling edge.

JUST:
- 0 Input data is left justified up to 24 bits.
- 1 Input data is right justified, assumed to be 16 bits.

WCPL:
- 0 Output word boundry is on WCKO falling edge.*
- 1 Output word boundry is on WCKO rising edge.

COB:
- 0 2's complement output data.
- 1 Complementary offset binary output data.

DGL0, DGL1, DGL2, DGL3, DGL4:
The falling edge of DG can be programmed to occur at the beginning of any one of 32 deglitch intervals dividing the output sampling period. This five bit word selects the falling edge of the deglitch interval. (In Stand-Alone Mode, DG goes low at the beginning of the 15th interval).

DGH0, DGH1, DGH2, DGH3, DGH4:
The rising edge of DG can be programmed to occur at any one of 32 deglitch intervals dividing the output sampling period. This five bit word selects the rising edge of the deglitch interval. (In Stand-Alone Mode, DG goes high at the beginning of the 31st interval).

LRPL:
- 0 LRCI rising edge is the start edge.*
- 1 LRCI falling edge is the start edge.

OSIZ0, OSIZ1:
- 00 Output word length is 16 bits.
- 10 Output word length is 18 bits.
- 01 Output word length is 20 bits.
- 11 Output word length is 24 bits.

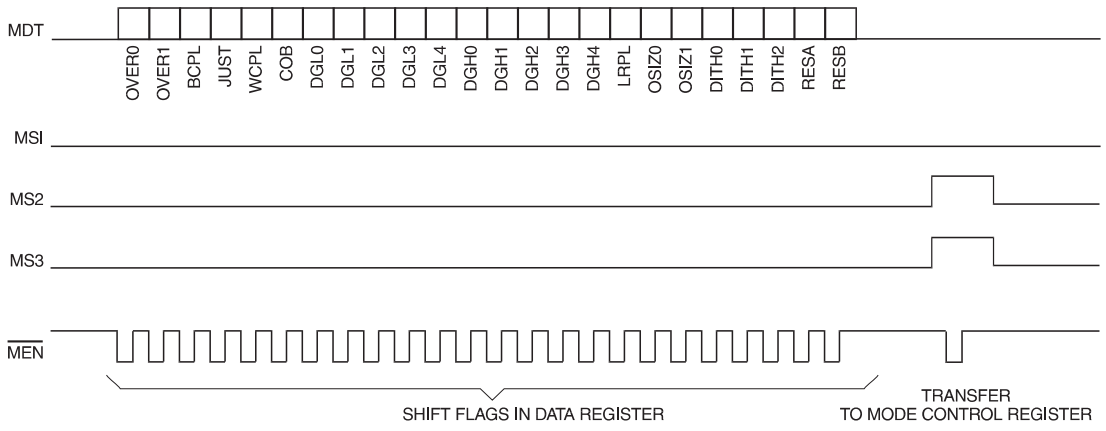
DITH0, DITH1, DITH2:
- 000 Dither mode 0. Minimum high frequency weighted*
- 100 Dither mode 1.
- 010 Dither mode 2.
- 110 Dither mode 3.
- 001 Dither mode 4.
- 101 Dither mode 5.
- 011 Dither mode 6. Maximum high frequency weighted.
- 111 Dither mode 7. Minimum white triangular PDF dither.

RESA:
- 0 Reserved, must be set to 0.

RESB:
- 0 Reserved, must be set to 0. RESB is the last bit entered.

*Denotes default value in Stand-Alone Mode.

Mode Control Register



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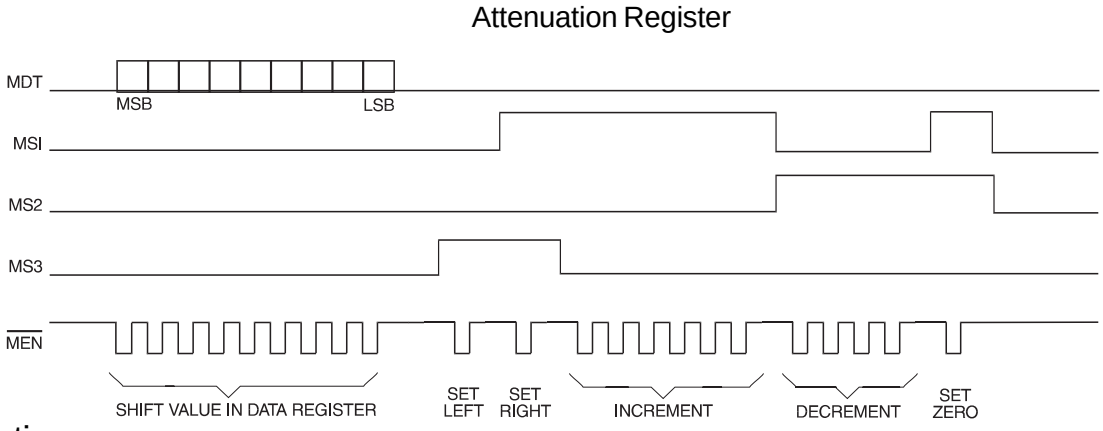
Attenuation Mode

In Program mode, the PMD-100 has a digital attenuator which can be set for each channel in increments of 0.188 dB between 0 and approximately 96 dB of attenuation. The attenuation value is entered MSB first as a 9 bit word on the MDT pin. The same value attenuation may be clocked to both left and right registers by the use of the attenuators mode controls (see timing diagram below). Changes in attenuation value are always carried out smoothly at a rate of one 0.188 dB step every 16 input samples. The delay between an attenuation command and the first sample it affects can be between 84 and 100 input samples.

Since the PMD-100 has no reset pin, when it is powered up in Program mode, the attenuator registers will contain arbitrary values. As part of the initial programming, it is necessary to issue a ZERO attenuation command or set the attenuation to known value using the SET LEFT and SET RIGHT commands.

Attenuation Data Byte	Attenuation	Attenuation Data Byte	Attenuation
0 0000 0000	0 dB	0 0010 0000	6.016 dB
0 0000 0001	0.188 dB	0 0011 0101	9.964 dB
0 0000 0110	1.128 dB	0 0100 0000	12.032 dB
0 0000 1011	2.068 dB	0 1000 0000	24.064 dB
0 0001 0000	3.008 dB	1 0000 0000	48.128 dB
		1 1111 1111	96.068dBs



Muting

The chip has two muting functions, hard mute and soft mute, which are activated by raising the respective input pins HMUTE and SMUTE to logic high. The soft mute ramps the output signal down at the same rate as the digital attenuator (one step per 16 input samples). It is designed for voluntary muting, such as when changing input selection. The hard mute goes to full attenuation in approximately 1millisecond, which is less than the group delay through the filter, and is intended to be used for emergency situations such as loss of input signal. Both muting functions release softly, at the rate of the digital attenuator. When combined with the fact that the chip continues to supply clock signals to the DAC's in the absence of input signals, the digital muting may eliminate the need for analog muting in many circuit designs. Note that during soft mute, the output dither remains on, while during hard mute, output dither is off.

Dither Modes

The PMD-100 provides 8 different output dithers in Program mode. All dither levels are available for output data widths from 16 to 24 bits at 8 Fs and 4 Fs oversampling rates only. Dither must be disabled if the 2 Fs oversampling rate is selected (as well as 24 bit mode must be selected when the 2 Fs oversampling rate is selected). There are seven levels of high-frequency weighted dither (modes 0-6) plus minimum amplitude white triangular PDF dither (mode 7). Modes 0 and 7 are minimum amplitude dithers which correct quantizing errors only, whereas modes 1 through 6 are increasing levels of high-frequency weighted dither designed to smooth out non-linearity errors in multi-bit DAC's (Modes 0 or 7 are appropriate for single-bit DAC's). The HF weighted dithers put the dither energy above the audio spectrum, where most of it is later filtered out by the analog low-pass filter following the DAC. In general, multi-bit DAC's behave better with high levels of dither, but some analog circuits following the DAC may have problems with transient intermodulation distortion (TIM) when confronted with high levels of high frequency energy. The best dither level for a particular circuit implementation must be determined empirically.

Dither Notes:
1) Dither level 6 is the highest level of high-frequency weighted dither available with the PMD-100.
2) In Stand-Alone Mode, dither mode 0 (minimum high frequency weighted) is available. Setting pin 4 DITH low will disable all dither including programmed dither and should be used only for test purposes.

Gain and Scale

The PMD-100 has a design attenuation of 1 dB to allow for filter overshoot on transients.

Most HDCD recordings are encoded using peak extension which gives them more "head room" than standard 16 bit recordings. In order to ensure that the average program output level of most HDCD recordings match that of standard recordings, it is necessary to increase the gain of the system 6 dB for those HDCD recordings, or, equivalently, reduce the gain of standard recordings 6 dB. This can be done either in the analog domain after the DAC's, which allows the full range of the DAC's to be used for both types of recordings, or in the digital domain within the PMD-100.

Note that one or the other of these gain scaling options must be used.

If the designer elects to use the analog approach, a 6 dB glitch-free gain change, controlled by the GAIN output of the chip, must be provided in the analog circuit. In this case, the SCAL pin is tied high. Since HDCD recordings can have peaks which are 6 dB higher than standard recordings with the same average levels, the analog circuits must provide enough head room for these higher levels. The gain change switching in the analog circuitry should occur within 50 msec of the GAIN output change to insure proper audio output levels.

To elect the digital scaling option, the SCAL pin is tied low and the GAIN pin must be left open. In this case, standard 16 bit recordings and those HDCD recordings encoded without peak extension are attenuated 6 dB inside the chip. The digital implementation has the advantage of simplicity and the lack of audible glitches, but does not use 1 bit of DAC resolution on non-HDCD recordings. If 20 bit DAC's are used, especially in conjunction with the PMD-100's output dither options, this does not represent much of a loss in practice since standard recordings only have 16 bit resolution. However, if 20 or 24-bit signal sources are expected, gain scaling is best accomplished in the analog domain.

De-emphasis Filter

The purpose of the digital de-emphasis filter is to reduce high-frequency quantization noise and to increase dynamic range with pre-emphasized non-HDCD encoded recordings. De-emphasis is turned ON by setting the DEEMPH input HIGH. The filter coefficients are selected for the input data sample frequency (44.1 or 48 kHz) by setting the FSEL mode control flag.

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Additional PMD-100 Considerations

Power and Ground

VDD1 (pin 7) powers the core. VDD2 (pin 22) powers the output pins. VDD1 may be connected to VDD2 externally. For lowest output clock jitter, it is recommended that VDD_2 be powered from it's own separately regulated power supply. VSS1 (pin 8) and VSS2 (pin 21) are internally connected and must be externally connected to the same ground source. Adding a 0.1uF capacitor on each VDD-VSS pair, as close to these pins as possible, is strongly recommended.

Input Pins

Some of the input pins, such as HMUTE (pin 17) can produce several 10's of microamps of noise current when pulled low. Because these inputs have TTL compatible input thresholds, this current can produce false triggering of logic high unless the impedance to ground is less than 1000 ohms. If these inputs are driven by logic or pulled low to ground with a switch, there is no problem.

Serial Data Input

Due to the high-speed characteristics of the PMD-100, care should be taken to minimize high-frequency noise on the serial data and clock inputs. The PMD-100 operates at TTL level thresholds and even very narrow spikes over 0.5V may be interpreted as valid data. Input data to the PMD-100 should be properly terminated, either by series termination at the source, or if necessary, AC termination at the PMD-100 input. Series termination may be especially helpful for the master clock source, XTI. A 100 ohm resistor in series with the XTI signal, as close to the source as possible, will help to prevent undershoot and potential lock-up. Also, pay close attention to the timing relationship of XTI relative to LRCI.

Output Clocking

Although every effort has been made to keep the internally generated jitter low in the PMD-100, for the best sonic performance we recommend re-clocking the critical conversion clock(s) using external circuitry. Don't forget to maintain the timing relationships of the word clock, bit clock, and the right and left data outputs. The simplest thing to do is to just re-clock all of these output signals. When used as a low jitter filter without external re-clocking, the PMD-100 should have its own power regulator and a 10uf in parallel with a 0.1uf decoupling capacitor for each power pin. Although the PMD-100 accepts either 256 or 384 Fs, it's output timing is based upon a 256 Fs system clock with a changing duty cycle.

The PMD-100 incorporates the Patented "Silent Conversion" variable clock timing and was designed to output a very stable word clock. These features resulted in minimizing jitter induced sonic degradation. However, the PMD-100 was designed prior to the introduction of bit clocked DACs. Therefore, additional care must be used when implementing the PMD-100 and any bit clocked DAC. In general, the PMD-100 exhibits more jitter on it's bit clock output when compared to it's word clock output.

The PMD-100's internally generated jitter on the bit clock output is lower when it is operated at 256 Fs when compared to 384 Fs (XTIM low versus high). When implementing the PMD-100 into a 384 Fs and bit clocked DAC design, we strongly recommend using re-clocking circuitry in order to attain the best possible sonic perfomance. To assure jitter-free conversion, digital signals should be reclocked directly from an oscillator placed near the DAC(s). By selecting a 768 Fs system clock to synchronize the re-clocking circuitry, then divide the system clock by two (using a flip-flop) which yields the desired 384 Fs system clock to drive the rest of the circuitry. For additional details on this implementation of the PMD-100, please contact Pacific Microsonics.

Application Notes

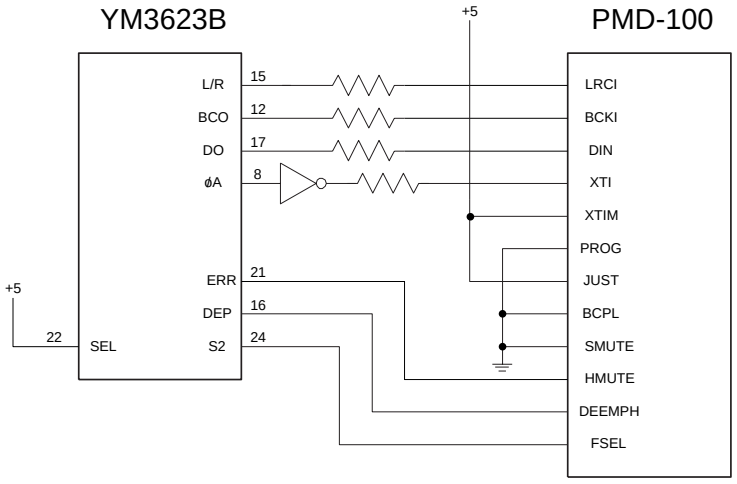

FIG. 1 Connecting PMD-100 to the Yamaha YM3623B Digital Receiver

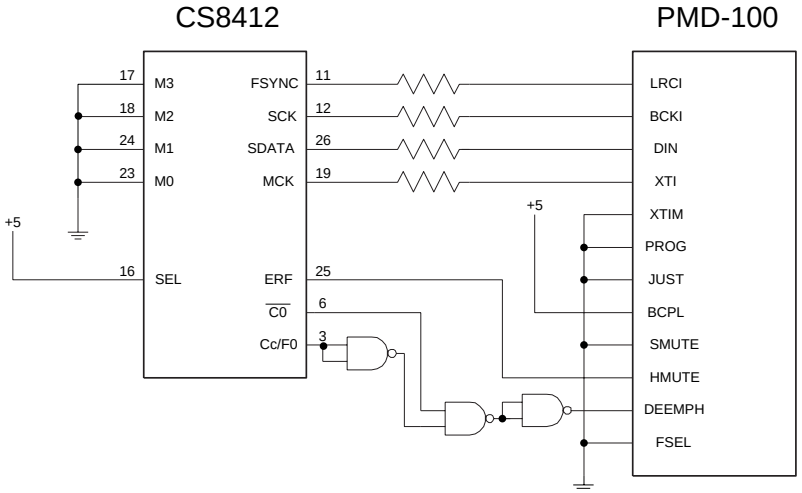

FIG. 2 Connecting the PMD-100 to the Crystal CS8412 Digital Receiver

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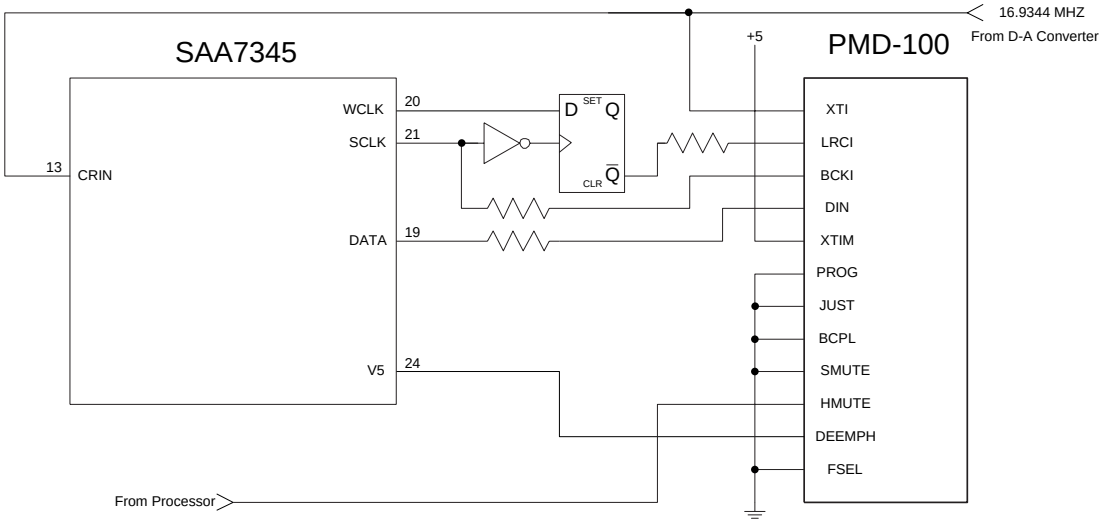

FIG. 3 Connecting the PMD-100 to the Phillips SAA7345 Demodulator I^2s Mode

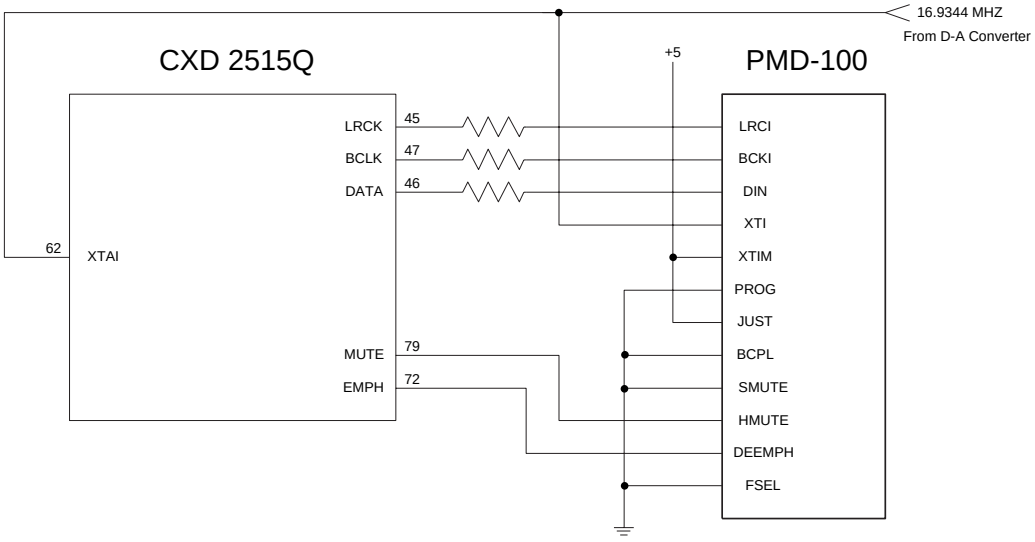

FIG. 4 Connecting the PMD-100 to the Sony CXD2515Q Decoder EIAJ Mode

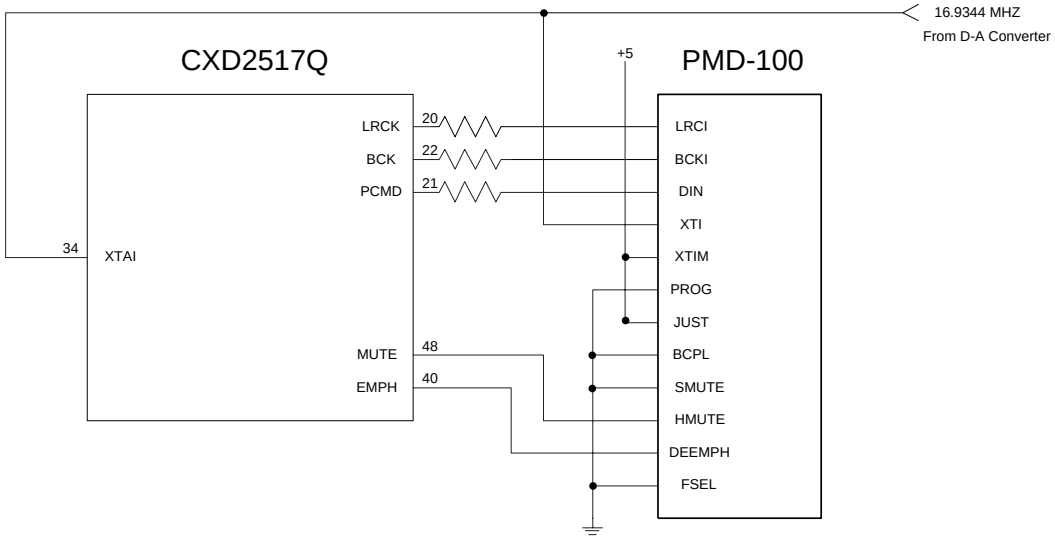

FIG. 5 Connecting the PMD-100 to the Sony CXD2517Q

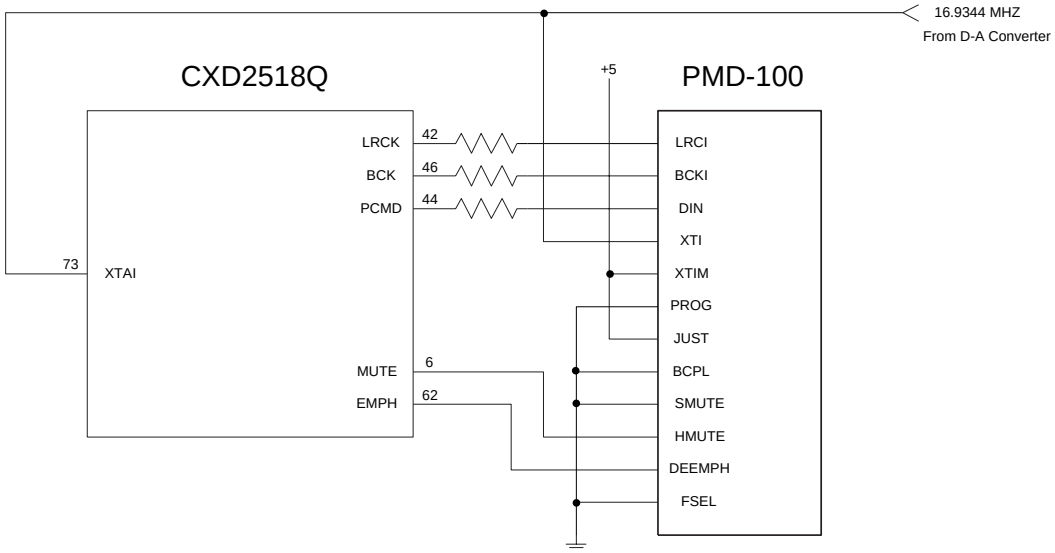

FIG. 6 Connecting the PMD-100 to the Sony CXD2518Q

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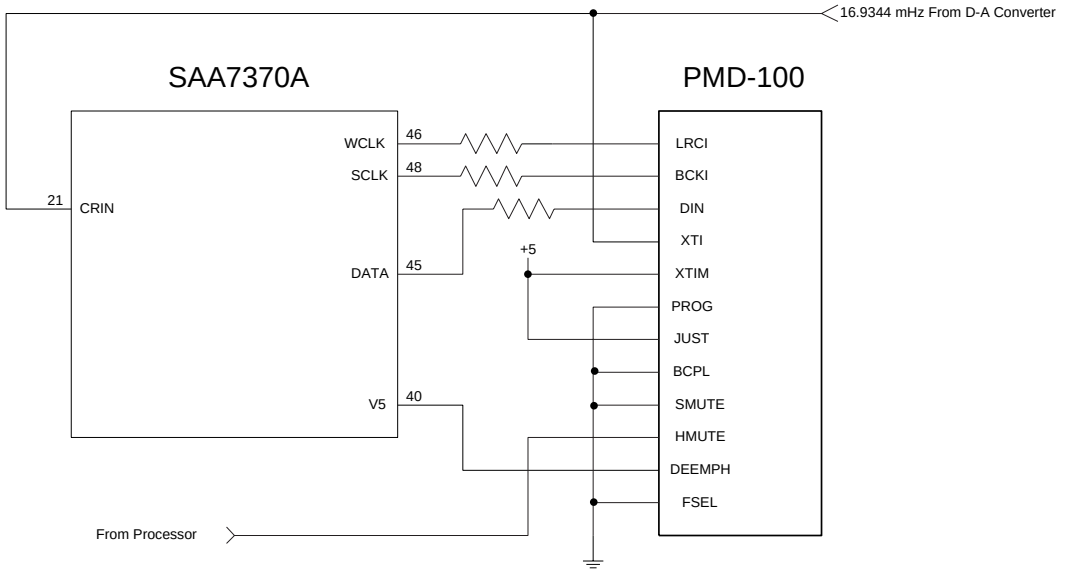

FIG. 7 Connecting the PMD-100 to the Phillips SAA7370A Demodulator in EIJA Mode
Control Register 3 @ 0011 set to 0010
Control Register D @ 1101 set to 01xx

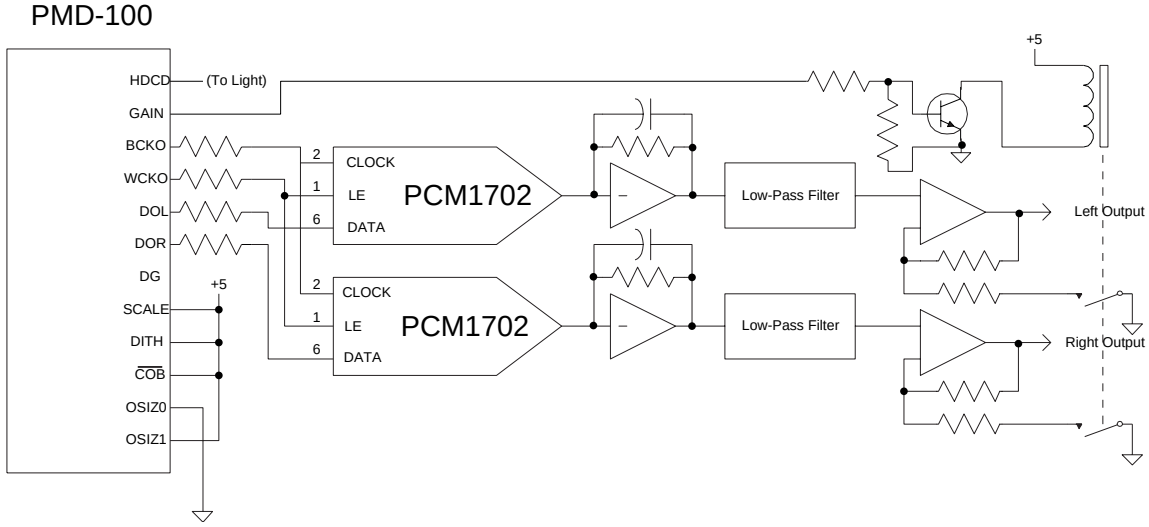

FIG. 8 20 Bit / 8x Oversampled Conversion using the Burr-Brown PCM1702 DAC

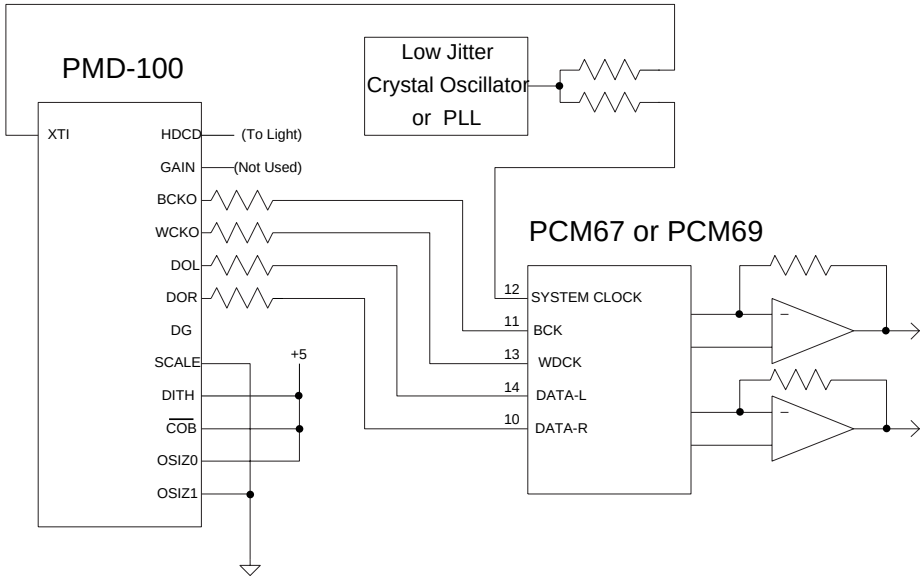

FIG. 9 18 Bit / 8x Oversampled Conversion using the Burr-Brown PCM67 or 69 DAC

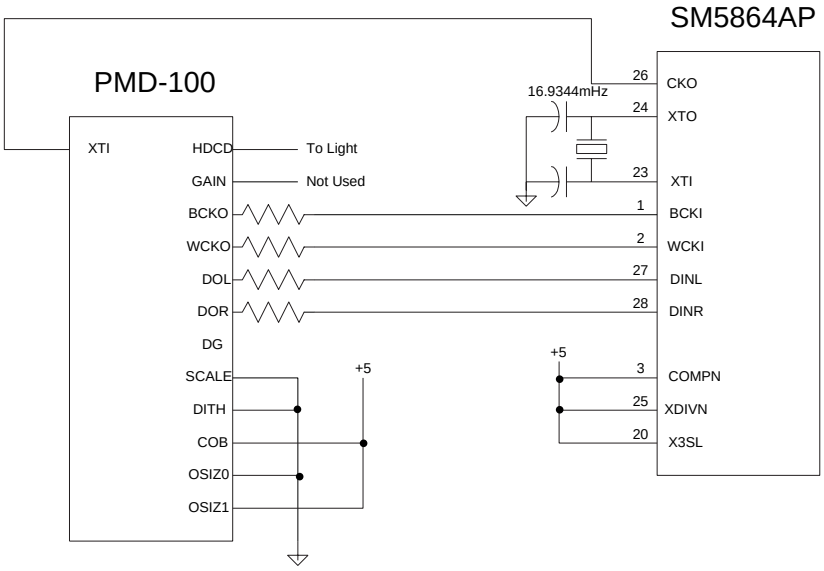

FIG. 10 20 Bit / 8x Conversion using the NPC SM5864AP DAC

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Digital Filter Compatibility & Comparison

The PMD-100 HDCD® Process Decoder is pin compatible with existing Digital Oversampling Filters: the NPC SM5842, NPC SM5803, and BB DF1700. Pin for pin, the data and clock input and output lines are as follows:

Pin	Name	Description
1	DIN	Serial Data Input
2	BCKI	Bit Clock Input
6	XTI	System Clock Input
23	DOR	Right Channel Serial Data Output
24	DOL	Left Channel Serial Data Output
25	WCKO	Word Clock Output
26	BCKO	Bit Clock Output
28	LRCI	Word Clock Input

A general comparison of the different digital filter specifications are outlined in the following table:

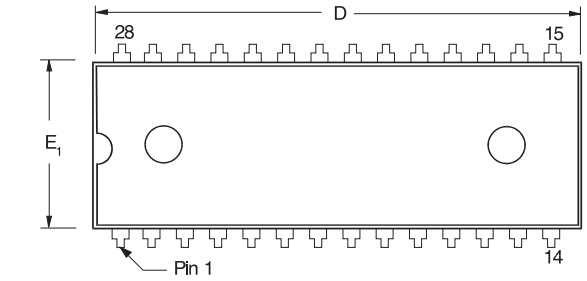
Features	PMD-100	NPC SM5842	NPC SM5803	BB DF1700
HDCD Process Decoding	Yes	No	No	No
Operating Modes (Program/Stand-Alone)	Both	Stand-Alone only	Program only	Stand-Alone only
Digital Attenuation	0-96dB (.188 steps)	No	0-96dB (.188 steps)	No
Stopband Attenuation	>120 dB	>117 dB	>110 dB	>110 dB
Dither Modes	Choice of 8	1 only	“Noise Shaping”	None
Oversampling Rates	8X, 4X, 2X	8X	8X, 4X	8X
Input Word Length (bits)	16, 18, 20, 29	16, 18, 20, 24	16, 18	16
Output Word Length (bits)	16, 18, 20, 24	18, 20, 22, 24	16, 18, 20	16, 18, 20
System Clock (Fs)	256, 384	256, 384	192, 256, 384, 512	192, 256, 384, 512
Input Sample Rate (kHz)	32 - 55	32, 44.1, 48	32, 44.1, 48	32, 44.1, 48
Muting	Hard & Soft	Soft, L & R Independent	Soft, L & R Independent	None
Digital Deemphasis	Yes	Yes	Yes	No
“Jitter Free” Clocking	Yes	Yes	Yes	No

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Pacific Microsonics, Inc. recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

MECHANICAL

P Package - 28-Pin Plastic DIP

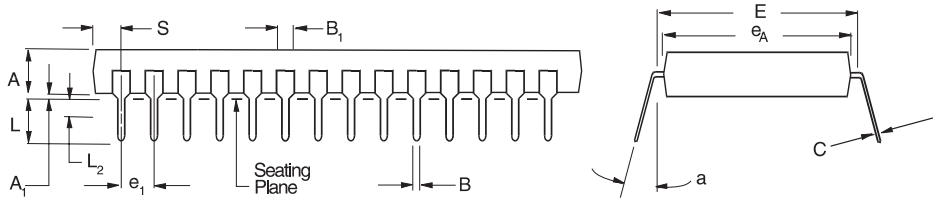


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A (1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D (1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
a	0°	15°	0°	15°
S(1)	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



Pin Out for PMD-100CQ Stand-Alone Mode (for descriptions refer to Page 4)

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1:	GAIN	12:	$\overline{\text{COB}}$	23:	SCAL	34:	BCKO
2:	XTI	13:	JUST	24:	DG	35:	HDCD
3:	N.C.	14:	N.C	25:	N.C.	36:	N.C.
4:	VDD 1a	15:	BCPL	26:	VSS 2a	37:	LRCI
5:	VDD 1b	16:	N.C.	27:	VSS 2b	38:	N.C.
6:	N.C.	17:	SMUTE	28:	N.C.	39:	DIN
7:	VSS 1a	18:	N.C.	29:	VDD 2a	40:	N.C.
8:	VSS 1b	19:	DEEMPH	30:	VDD 2b	41:	BCKI
9:	PROG	20:	N.C.	31:	DOR	42:	N.C.
10:	OSIZ0	21:	HMUTE	32:	DOL	43:	XTIM
11:	OSIZ1	22:	FSEL	33:	WCKO	44:	DITH

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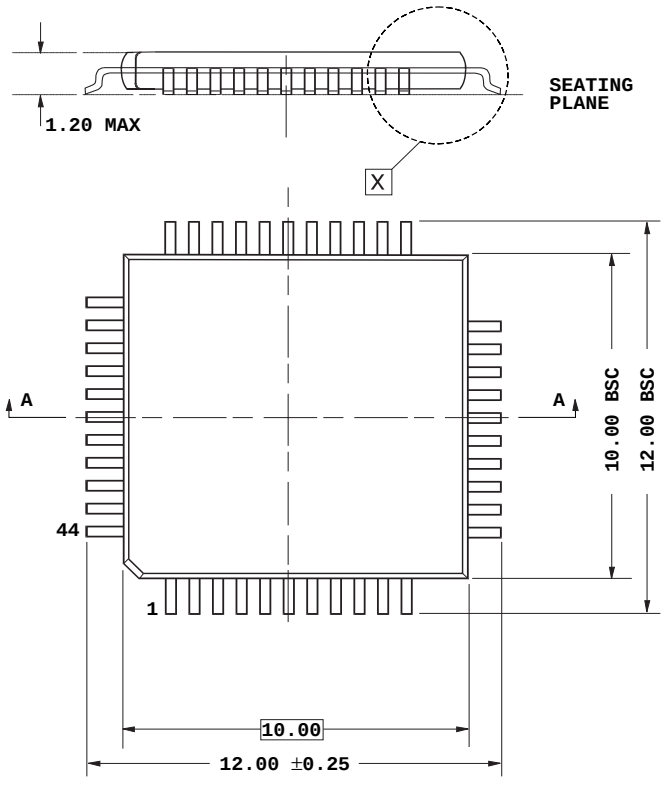
Pin Out for PMD-100CQ Program Mode (for descriptions refer to Page 5)

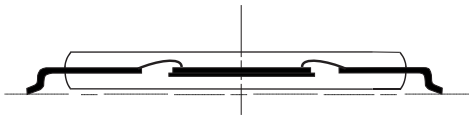
Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1:	GAIN	12:	MS 3	23:	SCAL	34:	BCKO
2:	XTI	13:	MDT	24:	DG	35:	HDCD
3:	N.C.	14:	N.C	25:	N.C.	36:	N.C.
4:	VDD 1a	15:	$\overline{\text{MEN}}$	26:	VSS 2a	37:	LRCI
5:	VDD 1b	16:	N.C.	27:	VSS 2b	38:	N.C.
6:	N.C.	17:	SMUTE	28:	N.C.	39:	DIN
7:	VSS 1a	18:	N.C.	29:	VDD 2a	40:	N.C.
8:	VSS 1b	19:	DEEMPH	30:	VDD 2b	41:	BCKI
9:	PROG	20:	N.C.	31:	DOR	42:	N.C.
10:	MS 1	21:	HMUTE	32:	DOL	43:	XTIM
11:	MS 2	22:	FSEL	33:	WCKO	44:	DITH

NOTE: N.C. means there is no internal connection to this pin.

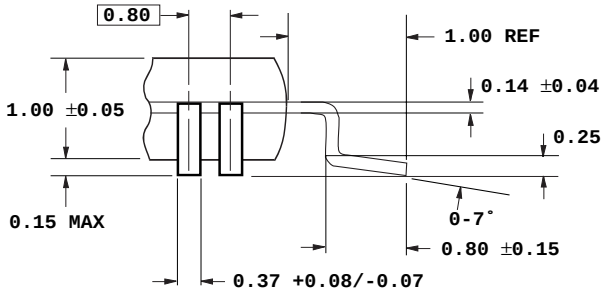
MECHANICAL

TQFP44 (Thin quad flat pack package, 44 leads).





SECTION A-A



DETAIL X

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. LEADFRAME MATERIAL: COPPER.
3. TO BE MOLDED CAVITY UP (SEE SECTION A-A).

HDCD Decoder Distributors

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