Jz4730

32 Bits Microprocessor

Data Sheet

Revision: 1.1
Date: Aug. 2006

北京君正集成电路有限公司
Ingenic Semiconductor Co. Ltd

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Release history

Date	Revision	Change
Apr. 2006	1.0	First release
Aug. 2006	1.1	- Change ball assignment and some DC parameter tables - Add solder process description

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Ingenic Semiconductor Co. Ltd

22th Floor, Building A, Cyber Tower, No.2, Zhong Guan Cun South Avenue
Haidian District, Beijing 100086, China
Tel: 86-10-82511297
Fax: 86-10-82511589
Http: //www.ingenic.cn

Content

1 Overview

Jz4730 is a 32 Bits RISC processor targeting for handheld and general embedded applications. Incorporate the JzRISC core based on leading micro architecture technology, this processor provides high integration, high performance and low power consumption solution for embedded device.

The JzRISC is the advanced and power-efficient 32-bit RISC core with 16K I-Cache and 16K D-Cache in this processor, operating at speeds up to 400MHz. On-chip modules such as LCD controller, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. The memory interface supports a variety of memory types that allow flexible design requirements, include the glueless connection to NAND Flash for cost sensitive applications. WLAN, Bluetooth and expansion options are provided through the PCMCIA/CF, USB, and MMC/SD host controllers. And the other peripherals such as UART, SPI, and Ethernet controller as well as general-system resources provide enough compute and connectivity capability for many applications. For the processor block diagram, refer to .

1.1 Block Diagram

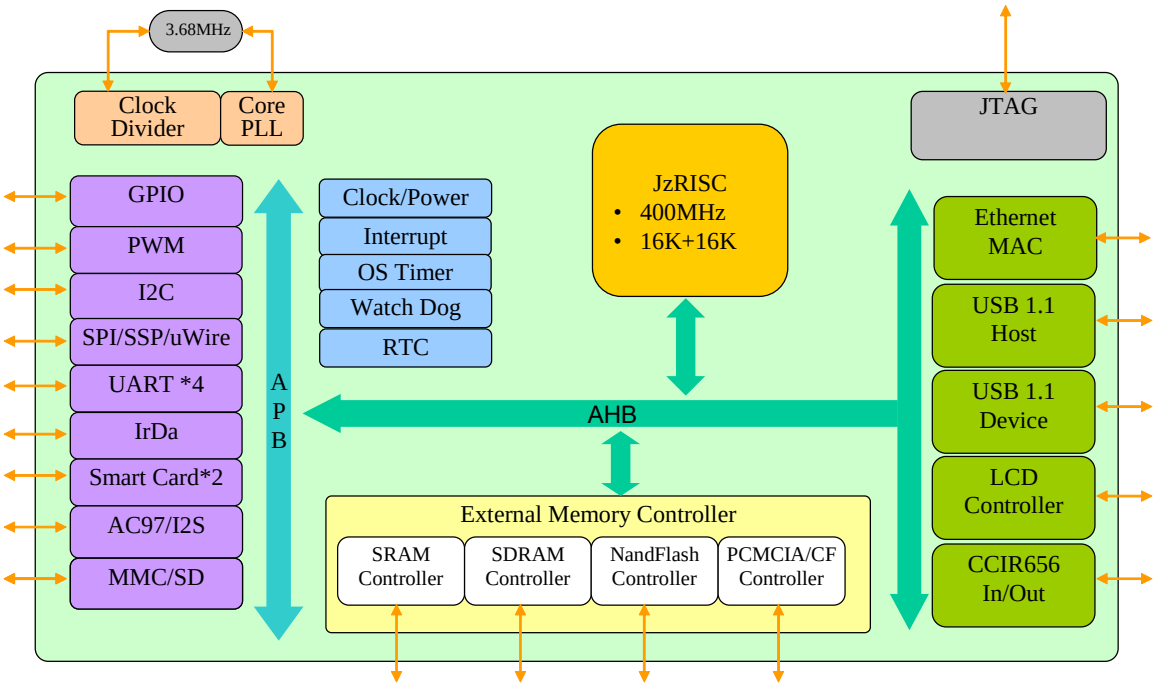


Figure 1-1 Jz4730 Diagram

1.2 Features

1.2.1 JzRISC Core

JzRISC core is a high performance and low power microprocessor core.

- 32-bit RISC CPU, clock up to 400MHz
- Low power consumption: < 0.5mW/MHz
- 16K I-Cache & 16K D-Cache
- MMU support with I-TLB, D-TLB and J-TLB
- Hardware Debug support via JTAG port

1.2.2 System Control and Timers

- Interrupt controller
  - Total 28 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Operating system timer
  - Provide three separate channels
  - 32-bit counter with auto-reload function
  - Generate interrupt when the down counter underflows
  - Six counting clock sources: RTCCLK (real time clock), EXTAL (external clock input), ϕ/4, ϕ/16, ϕ/64 and ϕ/256. (ϕ is the internal clock for on-chip peripheral)
- Watchdog timer
  - 32-bit counter with RTC clock
  - Generate power-on reset
- Pulse Width Modulator (PWM)
  - Period control through a 6-bit clock divider and a 10-bit period counter
  - 10-bit pulse counter
- General-Purpose I/O ports
  - Total GPIO pin number is 128
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output

1.2.3 Memory Interface

- Static memory interface
  - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash

- Six chip-select pin for static memory, each can be configured separately
- Support 8, 16 or 32 bits data width
- The size and base address of static memory banks are programmable

- NAND Flash interface
  - Support on CS3, sharing with static memory bank 3
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Hardware ECC generation
  - Support automatic boot up from NAND Flash devices
- Synchronous DRAM Interface
  - 2 banks with programmable size and base address
  - 32-bit and 16-bit data bus width is supported
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions
  - Supports power-down mode to minimize the power consumption of SDRAM
  - Supports page mode
- PC Card Interface
  - Fully compliant with the release of March 1997 of PC Card standard (16-bit PC Card)
  - DMA transfer support
  - Supports two PCMCIA or CF socket
- Direct Memory Access Controller
  - Eight independent DMA channels
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
  - Transfer requests can be: auto-request within DMA; on-chip peripheral module request; and external request
  - Interrupt on transfer completion or transfer error
  - Supports two transfer modes: single mode or block mode
- The Jz4730 processor system supports little endian only

1.2.4 Inter-chip Connectivity

- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition
- Synchronous serial interface
  - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
  - Configurable 2 - 17 (or multiples of them) bits data transfer
  - Full-duplex/transmit-only/receive-only operation
  - Supports normal transfer mode or Interval transfer mode
  - Programmable transfer order: MSB first or LSB first
  - 17-bit width, 16-level deep transmit-FIFO and receive-FIFO

- Programmable divider/prescaler for SSI clock
- Back-to-back character transmission/reception mode

1.2.5 Connectivity and Expansion

- Four UART interface
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 16x8bit FIFO for transmit and 16x11bit FIFO for receive data
  - Programmable baud rate up to 230.4Kbps
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
- Two smart card controller
  - Compliant with ISO/IEC standard 7816-3, supports both normal smart card and UIM card interface
  - Support asynchronous character (T = 0)/ block (T = 1) communication modes
  - 8-bit, 16-level FIFO, and programmable SCC_CLK output clock frequency
  - Interrupt support for data communication and error handling
- USB host interface
  - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible
- USB device interface
  - Compliant with USB protocol revision 1.1
  - Supports suspend/resume and remote wakeup
  - Supports 8 physical endpoints and 9 logic endpoints
  - Supports bulk, isochronous, interrupt and control transaction
- Ethernet MAC interface
  - Compliant with IEEE802.3, 802.3u
  - 10/100 Mbps data transfer rates with full and half duplex modes
  - IEEE802.3 compliant MII interface to talk to an external PHY
  - VLAN support
  - 2K bytes Tx buffers, and 2K bytes Rx buffers
  - Supports DMA engine using burst mode
  - Supports remote wake-up frame and magic packet frame

1.2.6 Multimedia Interface

- LCD
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - Up to 64K colors in active mode, and up to 4096 colors in passive mode
  - Display size up to 800×600 pixels

- 256×16 bits internal palette RAM
- Support ITU601/656 data format

- AC97/I2S controller
  - Supports 16, 18 and 20 bit sample for AC-link format, and 8, 16, 18, 20 and 24 bit for I2S/MSB-Justified format
  - DMA transfer mode support
  - Programmable Output channels and Input channels or Fixed mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
- Camera interface
  - Input image size up to 2048×2048 pixels
  - Supports CCIR656 data format
  - 32×32 image data receive FIFO with DMA support
- MultiMedia Card/Secure Digital Controller
  - Compliant with "The MultiMediaCard System Specification version 3.3"
  - Compliant with "SD Memory Card Specification version 1.01" and "SDIO Card Specification version 1.0" with 1 command channel and 4 data channels
  - 20~80 Mbps maximum data rate
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status

1.2.7 Clock and Power Management

- Clock generation Module
  - On-chip 3.6864MHz oscillator circuit
  - One On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, SCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
- Power Manager
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function.

2 Packaging and Pinout Information

2.1 Overview

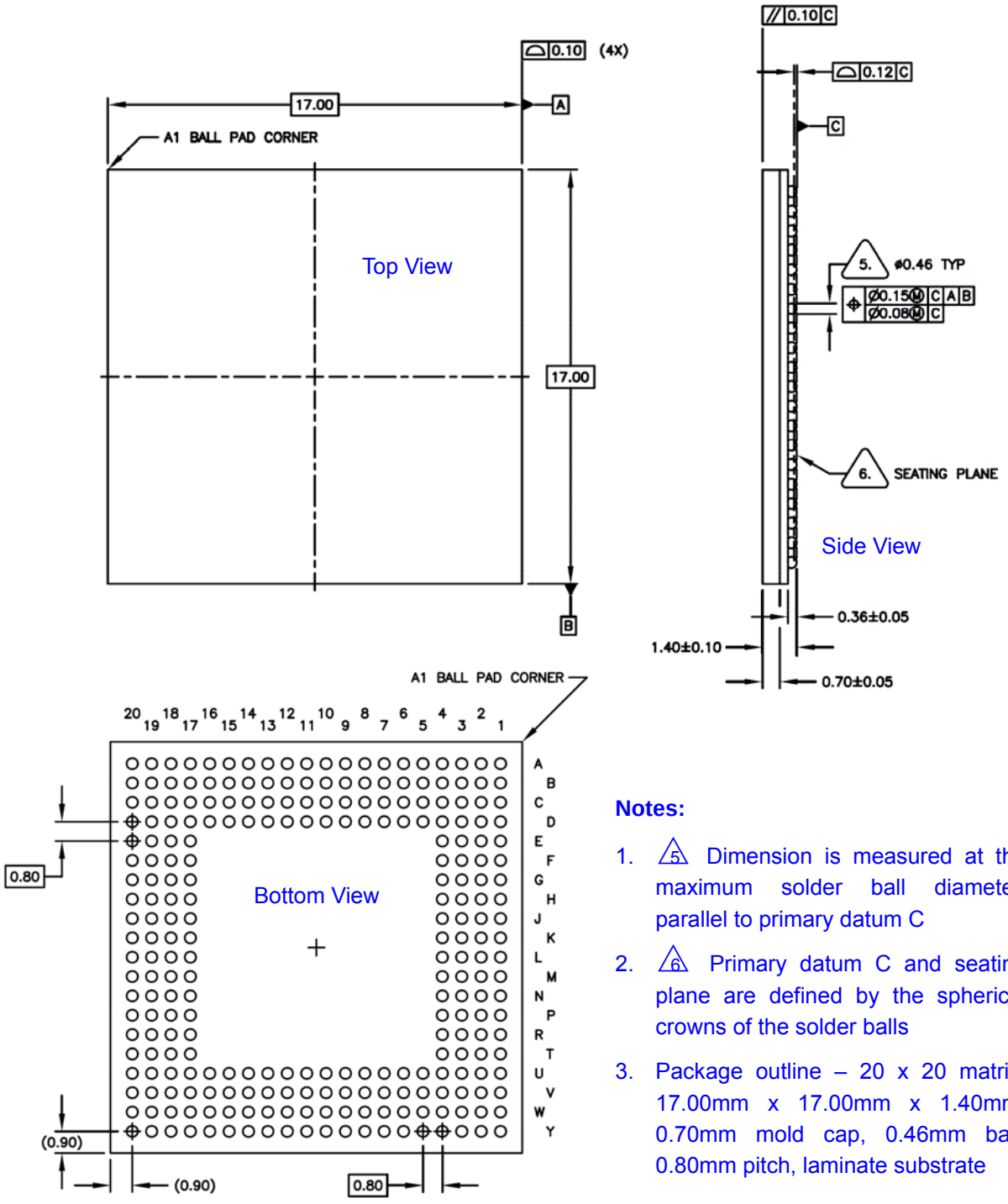
Jz4730 processor is packaged in a 256-pin ball grid array (LFBGA), has a square 17x17 and 4 rows ball assignment. The following figures and tables list all the functional pins.

Most of the GPIO pins are multiplexed on the on-chip peripheral modules, and the reset state is general-purpose input with internal pull-up or pull-down.

2.2 Solder Process

Jz4730 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Package



Notes:

1. ⚠5 Dimension is measured at the maximum solder ball diameter, parallel to primary datum C
2. ⚠6 Primary datum C and seating plane are defined by the spherical crowns of the solder balls
3. Package outline – 20 x 20 matrix, 17.00mm x 17.00mm x 1.40mm, 0.70mm mold cap, 0.46mm ball, 0.80mm pitch, laminate substrate

Figure 2-1 Jz4730 package

2.4 Pin Description

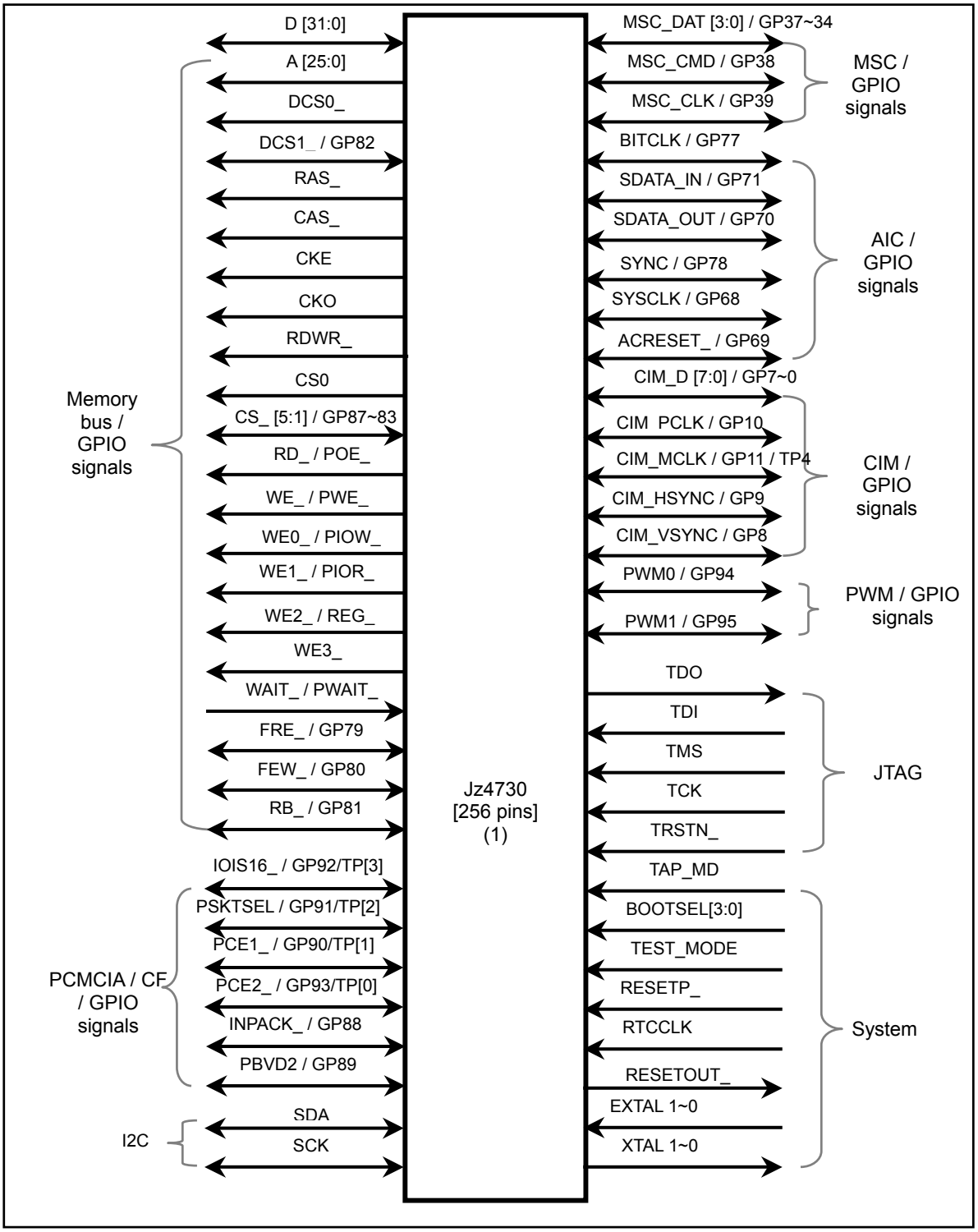


Figure 2-2 Jz4730 Pin Diagram (1)

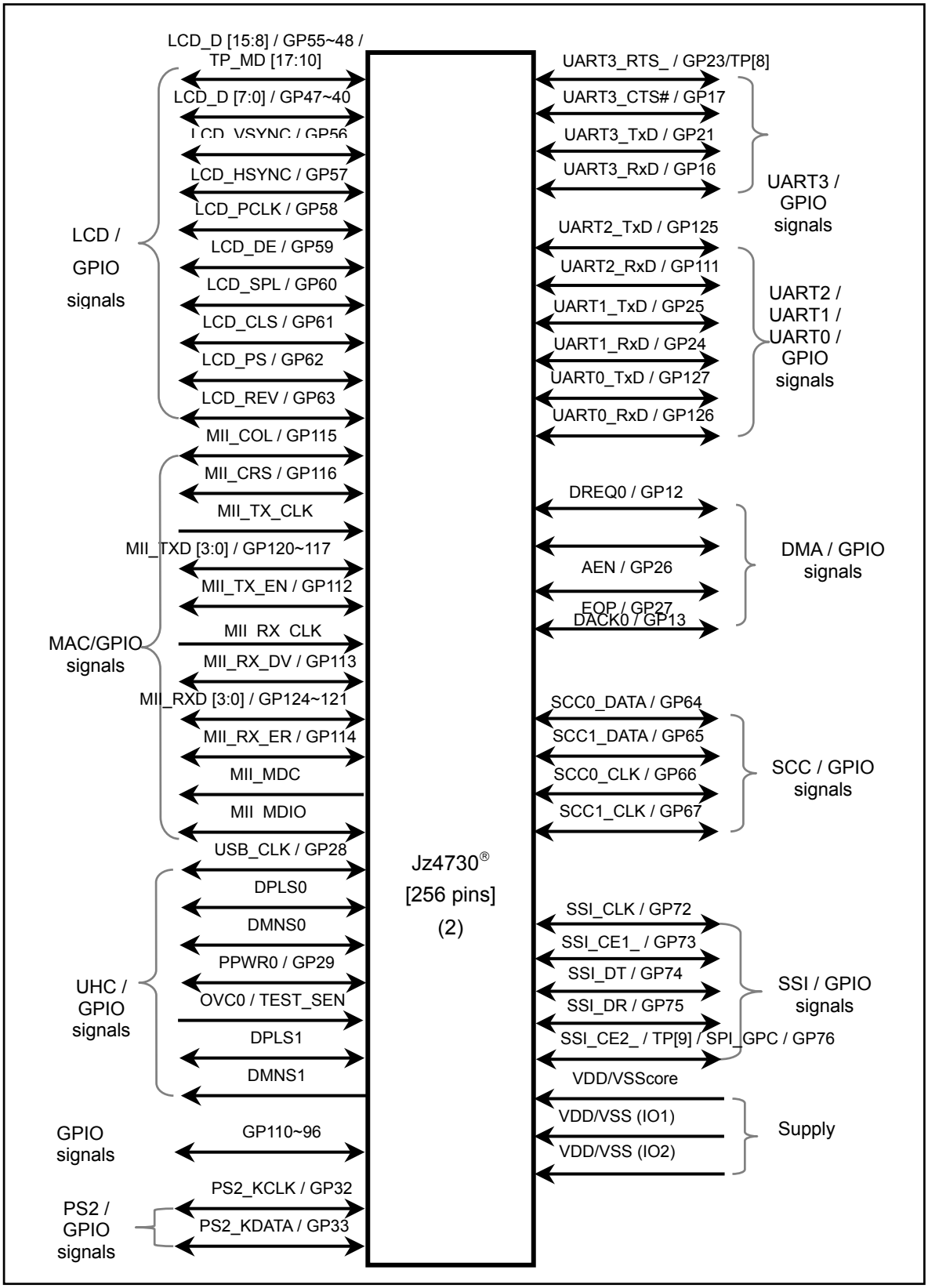


Figure 2-3 Jz4730 Pin Diagram (2)

Table 2-1 EMC Pins (81 for 256; 9 GPIO)

Pin Name	Type	Description	Comments
D[31:16]	I/O	Memory data bus, used for 32-bit memories	
D[15:0]	I/O	Memory data bus, lower 16 bits of the data bus	
A[25:17]	Output	Static memory address	
A[16:2]	Output	SDRAM memory address, multiplexing static memory address	
A[1:0]	Output	Static memory address	
DCS0_	Output	SDRAM chip select 0	
DCS1 / GP82	I/O	SDRAM chip select 1 / GPIO 82	Pull-up input at reset
RAS_	Output	Row address strobe for SDRAM	
CAS_	Output	Column address strobe for SDRAM	
CKE	Output	Clock enable for SDRAM	
RDWR_	Output	Read/write signal, 1 – read; 0 – write	
CKO	Output	SDRAM clock	
CS0_	Output	Static memory bank 0 chip select	
CS1_ / GP83	I/O	Static memory bank 1 chip select / GPIO 83	Pull-up input at reset
CS2_ / GP84	I/O	Static memory bank 2 chip select / GPIO 84	Pull-up input at reset
CS3_ / GP85	I/O	Static memory bank 3 chip select / GPIO 85	Pull-up input at reset
CS4_ / GP86	I/O	Static memory bank 4 chip select / GPIO 86	Pull-up input at reset
CS5_ / GP87	I/O	Static memory bank 5 chip select / GPIO 87	Pull-up input at reset
RD_ / POE_	Output	Read strobe for static memory device / Pcmcia memory read strobe	
WE_ / PWE_	Output	Write strobe for static memory device / Pcmcia memory write strobe	
WE0_ / PIOW_	Output	Byte 0 write enable / pcmcia IO write strobe	
WE1_ / PIOR_	Output	Byte 1 write enable / pcmcia IO read strobe	
WE2_ / PREG_	Output	Byte 2 write enable / pcmcia register select	
WE3_	Output	Byte 3 write enable	
WAIT_ / PWAIT_	Input	Wait signal for slow memory / pcmcia wait input	Internal pull-up

FRE_ / GP79	I/O	Read enable for NAND Flash / GPIO 79	Pull-up input at reset
FWE_ / GP80	I/O	Write enable for NAND Flash / GPIO 80	Pull-up input at reset
FRB_ / GP81	I/O	Ready or busy signal for NAND Flash / GPIO 81	Pull-up input at reset

Table 2-2 PCMCIA/CF Pins (6 for 256; 6 GPIO)

Pin Name	Type	Description	Comments
IOIS16_ / GP92 / TP[3]	I/O	PCMCIA IO address 16 bit select / GPIO 92 / Test port [3]	Pull-up input at reset
PSKTSEL / GP91 / TP[2]	I/O	PCMCIA socket select / GPIO 91 / Test port [2]	Pull-up input at reset
PCE1_ / GP90 / TP[1]	I/O	PCMCIA card enable 1 / GPIO 90 / Test port [1]	Pull-up input at reset
PCE2_ / GP93 / TP[0]	I/O	PCMCIA card enable 2 / GPIO 93 / Test port [0]	Pull-up input at reset
INPACK_ / GP88	I/O	PCMCIA INPACK_ input / GPIO 88	Pull-up input at reset
PBVD2 / GP89	I/O	PCMCIA BVD2 input / GPIO89	Pull-up input at reset

Table 2-3 LCD Pins (24 for 256; 24 GPIO)

Pin Name	Type	Description	Comments
LCD_D[15:8] / GP55 ~ GP48 / TP[17:10]	I/O	Higher 8-bit of LCD data / GPIO 55 ~ GPIO 48 / Test port [17:10]	Pull-down input at reset
LCD_D[7:0] / GP47 ~ GP40	I/O	Lower 8-bit of LCD data / GPIO 47 ~ GPIO 40	Pull-up input at reset
LCD_VSYNC / GP56	I/O	LCD frame clock/vertical sync / GPIO 56	Pull-down input at reset
LCD_HSYNC / GP57	I/O	LCD line clock/horizonal sync / GPIO 57	Pull-up input at reset
LCD_PCLK / GP58	I/O	LCD pixel clock / GPIO 58	Pull-down input at reset
LCD_DE / GP59	I/O	STN AC bias drive/Non-STN data enable output / GPIO 59	Pull-down input at reset

LCD_SPL / GP60	I/O	LCD SPL output for special TFT panel / GPIO 60	Pull-up input at reset
LCD_CLS / GP61	I/O	LCD CLS output for special TFT panel / GPIO 61	Pull-up input at reset
LCD_PS / GP62	I/O	LCD PS output for special TFT panel / GPIO 62	Pull-up input at reset
LCD_REV / GP63	I/O	LCD REV output for special TFT panel / GPIO 63	Pull-up input at reset

Table 2-4 I2C Pins (2 for 256)

Pin Name	Type	Description	Comments
I2C_SDA	I/O	I2C serial data	Open drain
I2C_SCK	I/O	I2C serial clock	Open drain

Table 2-5 SCC Pins (4 for 256; 4 GPIO)

Pin Name	Type	Description	Comments
SCC0_DATA / GP64	I/O	SCC0 data / GPIO 64	Pull-up input at reset
SCC0_CLK / GP66	I/O	SCC0 clock / GPIO 66	Pull-up input at reset
SCC1_DATA / GP65	I/O	SCC1 data / GPIO 65	Pull-up input at reset
SCC1_CLK / GP67	I/O	SCC1 clock / GPIO 67	Pull-up input at reset

Table 2-6 UART3 Pins (4 for 256; 8 GPIO)

Pin Name	Type	Description	Comments
UART3_CTS_ / GP17	I/O	UART3 clear to send / GPIO 17	Pull-up input at reset
UART3_RTS_ / GP23 / TP[8]	I/O	UART3 request to send / GPIO 23 / Test port [8]	Pull-up input at reset
UART3_TxD_ / GP21	I/O	UART3 TxD / GPIO 21	Pull-up input at reset
UART3_RxD_ / GP16	I/O	UART3 RxD / GPIO 16	Pull-up input at reset

Table 2-7 UART2 Pins (2 for 256; 2 GPIO)

Pin Name	Type	Description	Comments
UART2_TxD_ / GP125	I/O	UART2 TxD / GPIO 125	Pull-up input at reset
UART2_RxD_ / GP111	I/O	UART2 RxD / GPIO 111	Pull-up input at reset

Table 2-8 UART1 Pins (2 for 256; 2 GPIO)

Pin Name	Type	Description	Comments
UART1_TxD_ / GP25	I/O	UART1 TxD / GPIO 25	Pull-up input at reset
UART1_RxD_ / GP24	I/O	UART1 RxD / GPIO 24	Pull-up input at reset

Table 2-9 UART0 Pins (2 for 256; 2 GPIO)

Pin Name	Type	Description	Comments
UART0_TxD_ / GP127	I/O	UART0 TxD / GPIO 127	Pull-up input at reset
UART0_RxD_ / GP126	I/O	UART0 RxD / GPIO 126	Pull-up input at reset

Table 2-10 SSI Pins (5 for 256; 5 GPIO)

Pin Name	Type	Description	Comments
SSI_CLK / GP72	I/O	SSI clock output / GPIO 72	Pull-up input at reset
SSI_CE1_ / GP73	I/O	SSI chip enable 1 / GPIO 73	Pull-up input at reset
SSI_DT / GP74	I/O	SSI data output / GPIO 74	Pull-up input at reset
SSI_DR / GP75	I/O	SSI data input / GPIO 75	Pull-up input at reset
SSI_CE2_ / SPI_GPC / GP76 / TP[9]	I/O	SSI chip enable 2 / SSI GPC / GPIO 76 / Test port [9]	Pull-up input at reset

Table 2-11 DMA Pins (4 for 256; 6 GPIO)

Pin Name	Type	Description	Comments
DREQ0 / GP12	IO	DMA external request 0 / GPIO 12	Pull-up input at reset

DACK0 / GP13	IO	DMA transfer acknowledge 0 / GPIO 13	Pull-up input at reset
AEN / GP26 / TP[5]	IO	Address enable for transfer / GPIO 26 / Test port [5]	Pull-up input at reset
EOP / GP27 / TP[6]	IO	DMA transfer end / GPIO 27 / Test port [6]	Pull-up input at reset

Table 2-12 PWM Pins (2 for 256; 2 GPIO)

Pin Name	Type	Description	Comments
PWM0 / GP94	I/O	PWM 0 output / GPIO 94	Pull-up input at reset
PWM1 / GP95	I/O	PWM 1 output / GPIO 95	Pull-up input at reset

Table 2-13 UHC Pins (7 for 256; 4 GPIO)

Pin Name	Type	Description	Comments
USB_CLK / GP28	I/O	USB 48MHz clock / GPIO 28	Pull-up input at reset
DPLS0	Analog I/O	USB transceiver data plus 0	
DMNS0	Analog I/O	USB transceiver data minus 0	
OVC0 / TEST_SEN	I	Overcurrent input 0 / Scan enable for scan-req	
PPWR0 / GP29	I/O	Power enable output 0 / GPIO 29	Pull-up input at reset
DPLS1	Analog I/O	USB transceiver data plus 1	
DMNS1	Analog I/O	USB transceiver data minus 1	

Table 2-14 MAC Pins (17 for 256; 13 GPIO)

Pin Name	Type	Description	Comments
MII_COL / GP115	I/O	Ethernet collision / GPIO 115	Pull-up input at reset
MII_CRS / GP116	I/O	Ethernet carrier sense / GPIO 116	Pull-up input at reset

MII_TX_CLK	Input	Ethernet transmit clock	
MII_TXD[3] / GP120	I/O	Ethernet transmit data / GPIO 120	Pull-up input at reset
MII_TXD[2] / GP119	I/O	Ethernet transmit data / GPIO 119	Pull-up input at reset
MII_TXD[1] / GP118	I/O	Ethernet transmit data / GPIO 118	Pull-up input at reset
MII_TXD[0] / GP117	I/O	Ethernet transmit data / GPIO 117	Pull-up input at reset
MII_TX_EN / GP112	I/O	Ethernet transmit enable / GPIO 112	Pull-up input at reset
MII_RX_CLK	Input	Ethernet receive clock	
MII_RX_DV / GP113	I/O	Ethernet receive data valid / GPIO 113	Pull-up input at reset
MII_RXD[3] / GP124	I/O	Ethernet receive data / GPIO 124	Pull-up input at reset
MII_RXD[2] / GP123	I/O	Ethernet receive data / GPIO 123	Pull-up input at reset
MII_RXD[1] / GP122	I/O	Ethernet receive data / GPIO 122	Pull-up input at reset
MII_RXD[0] / GP121	I/O	Ethernet receive data / GPIO 121	Pull-up input at reset
MII_RX_ER / GP114	I/O	Ethernet receive error / GPIO 114	Pull-up input at reset
MII_MDC	Output	Ethernet management clock	
MII_MDIO	I/O	Ethernet management data inout	

Table 2-15 CIM Pins (12 for 256; 12 GPIO)

Pin Name	Type	Description	Comments
CIM_D [7:0] / GP7 ~ GP0	I/O	Data input from image sensor / GPIO 7 ~ GPIO 4	Pull-up input at reset
CIM_PCLK / GP10	I/O	CIM pixel clock / GPIO 10	Pull-up input at reset
CIM_MCLK / GP11 / TP[4]	I/O	CIM master clock / GPIO 11 / Test port [4]	Pull-up input at reset
CIM_HSYNC / GP9	I/O	CIM horizontal clock / GPIO 9	Pull-up input at reset
CIM_VSYNC / GP8	I/O	CIM vertical clock / GPIO 8	Pull-up input at reset

Table 2-16 PS2 Keyboard Pins (2 for 256; 2 GPIO)

Pin Name	Type	Description	Comments
PS2_KCLK / GP32	I/O	PS/2 keyboard clock / GPIO 32	Pull-up input at reset
PS2_KDATA / GP33	I/O	PS/2 keyboard data / GPIO 33	Pull-up input at reset

Table 2-17 AC97/I2S Pins (6 for 256; 6 GPIO)

Pin Name	Type	Description	Comments
BITCLK / GP77	I/O	AIC serial clock pin / GPIO 77	Pull-up input at reset
SDATA_IN / GP71	I/O	AIC serial data input / GPIO 71	Pull-up input at reset
SDATA_OUT / GP70	I/O	AIC serial data output / GPIO 70	Pull-up input at reset
SYNC / GP78	I/O	AIC frame synchronization pin / GPIO 78	Pull-up input at reset
SYSCLK / GP68	I/O	AIC system clock output / GPIO 68	Pull-up input at reset
ACRESET_ / GP69	I/O	AIC reset output / GPIO 69	Pull-up input at reset

Table 2-18 MSC Pins (6 for 256; 6 GPIO)

Pin Name	Type	Description	Comments
MSC_DAT[3] / GP37	I/O	MSC data / GPIO 37	Pull-up input at reset
MSC_DAT[2] / GP36	I/O	MSC data / GPIO 36	Pull-up input at reset
MSC_DAT[1] / GP35	I/O	MSC data / GPIO 35	Pull-up input at reset
MSC_DAT[0] / GP34	I/O	MSC data / GPIO 34	Pull-up input at reset
MSC_CMD / GP38	I/O	MSC command / GPIO 38	Pull-up input at reset
MSC_CLK / GP39	I/O	MSC clock output / GPIO 39	Pull-up input at reset

Table 2-19 GPIO Pins (15 for 256;)

Pin Name	Type	Description	Comments

GP110 ~ GP96	I/O	Special GPIO 110 ~ GPIO 96	Pull-up input at reset

Table 2-20 JTAG Pins (5 for 256)

Pin Name	Type	Description	Comments
TRSTN_	Input	JTAG reset	Internal pull-down
TMS	Input	JTAG mode select	Internal pull-up
TDI	Input	JTAG serial data input	Internal pull-up
TCK	Input	JTAG clock	Internal pull-down
TDO	Output	JTAG serial data output	

Table 2-21 System Pins (11 for 256)

Pin Name	Type	Description	Comments
EXTAL	Analog Input	System clock input	
XTAL	Analog Output	OSC output	
RTCCLK	Input	RTC clock input	
RESETOUT_	Output	Reset output	
RESETP_	Input	System power on reset input	
BOOT_SEL[3]	Input	Boot select input 3: 0->boot from ROM at CS0; 1->boot from NAND flash device at CS3	Internal pull-down
BOOT_SEL[2]	Input	Boot select input 2: NAND flash address cycles when boot from it, 0->low cycle; 1->high cycle	Internal pull-down
BOOT_SEL[1]	Input	Boot_select input 1: NAND flash page size when boot from it, 0->512B; 1->2048B	Internal pull-down
BOOT_SEL[0]	Input	Boot select input 0: NAND flash width when boot from it, 0->8bit; 1->16bit	Internal pull-down
TEST_MODE	Input	Chip test mode	Internal pull-down
TAP_MD	Input	TAP mode input - (1: internal JTAG; 0: boundary)	Internal pull-down

Table 2-22 Power Pins (28 for 256)

Pin Name	Description
VDDIO1	Power supply for IO pad (1.8V ~ 3.3V)
VSSIO1	Ground supply for IO pad (0V)
VDDIO2	Power supply for IO pad (3.3V)
VSSIO2	Ground supply for IO pad (0V)
VDDcore	Power supply for core (1.8V)
VSScore	Ground supply for core (0V)
VDDPLL	PLL power supply for analog (1.8V)
VSSPLL	PLL ground supply for analog
VDDUSB	Power supply for USB IO pad (3.3V)
VSSUSB	Ground supply for USB IO pad (0V)

2.5 Ball Assignment

Table 2-23 Ball and IO cell description[1, 2, 3]

Ball#	Signal Name	I/O	IO Cell	IO Cell Characteristics	Power	Note
A1	MII_TX_CLK	I	I		VDDIO2	
A2	MII_MDC	O	T02	2mA out	VDDIO2	
A3	MII_RX_ER/GP114	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
A4	MII_RX_CLK	I	I		VDDIO2	
A5	AEN/GP26	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
A6	VDDIO1	P	-	-	-	
A7	CS5_/GP87	IO	MUW02	2mA out, pull-up, pull-up on/off	VDDIO1	
A8	CS2_/GP84	IO	MUW02	2mA out, pull-up, pull-up on/off	VDDIO1	
A9	WAIT_	I	MUS	Pull-up, Schmitt	VDDIO1	
A10	A[0]	O	MO02	2mA out	VDDIO1	
A11	A[18]	O	MO02	2mA out	VDDIO1	
A12	A[22]	O	MO02	2mA out	VDDIO1	
A13	A[25]	O	MO02	2mA out	VDDIO1	
A14	CKO	O	MT12	12mA out	VDDIO1	
A15	WE0_	O	MO08	8mA out	VDDIO1	
A16	D[2]	IO	MB08	8mA out	VDDIO1	
A17	D[6]	IO	MB08	8mA out	VDDIO1	
A18	D[9]	IO	MB08	8mA out	VDDIO1	
A19	D[11]	IO	MB08	8mA out	VDDIO1	
A20	D[12]	IO	MB08	8mA out	VDDIO1	
B1	MII_MDIO	IO	B02	2mA out	VDDIO2	
B2	MII_TXD1/GP118	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
B3	MII_RXD2/GP123	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
B4	MII_CRS/GP116	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
B5	DREQ0/GP12	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
B6	DACK0/GP13	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
B7	FWE_/GP80	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO1	
B8	CS3_/GP85	IO	MUW02	2mA out, pull-up, pull-up on/off	VDDIO1	
B9	CS0_	O	MT02	2mA out	VDDIO1	
B10	RD_	O	MT02	2mA out	VDDIO1	
B11	A[17]	O	MO02	2mA out	VDDIO1	
B12	A[21]	O	MO02	2mA out	VDDIO1	
B13	A[24]	O	MO02	2mA out	VDDIO1	
B14	DCS0_	O	MO08	8mA out	VDDIO1	
B15	RAS_	O	MO08	8mA out	VDDIO1	
B16	D[1]	IO	MB08	8mA out	VDDIO1	
B17	D[5]	IO	MB08	8mA out	VDDIO1	

Ball#	Signal Name	I/O	IO Cell	IO Cell Characteristics	Power	Note
B18	D[8]	IO	MB08	8mA out	VDDIO1	
B19	D[10]	IO	MB08	8mA out	VDDIO1	
B20	D[13]	IO	MB08	8mA out	VDDIO1	
C1	LCD_D[14]/GP54	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
C2	MII_TXD0/GP117	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
C3	MII_TXD3/GP120	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
C4	MII_RXD0/GP121	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
C5	MII_RX_DV/GP113	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
C6	EOP/GP27	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
C7	FRE_/GP79	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO1	
C8	CS4_/GP86	IO	MUW02	2mA out, pull-up, pull-up on/off	VDDIO1	
C9	CS1_/GP83	IO	MUW02	2mA out, pull-up, pull-up on/off	VDDIO1	
C10	WE_	O	MT02	2mA out	VDDIO1	
C11	A[1]	O	MO02	2mA out	VDDIO1	
C12	A[20]	O	MO02	2mA out	VDDIO1	
C13	A[23]	O	MO02	2mA out	VDDIO1	
C14	DCS1_/GP82	IO	MUW08	8mA out, pull-up, pull-up on/off	VDDIO1	
C15	CAS_	O	MO08	8mA out	VDDIO1	
C16	D[0]	IO	MB08	8mA out	VDDIO1	
C17	D[4]	IO	MB08	8mA out	VDDIO1	
C18	D[7]	IO	MB08	8mA out	VDDIO1	
C19	D[14]	IO	MB08	8mA out	VDDIO1	
C20	D[15]	IO	MB08	8mA out	VDDIO1	
D1	LCD_D[10]/GP50	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
D2	LCD_D[12]/GP52	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
D3	MII_TX_EN/GP112	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
D4	MII_RXD1/GP122	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
D5	MII_COL/GP115	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
D6	VSSIO2	P	-	-	-	
D7	FRB_/GP81	IO	MUW04	4mA out, pull-up, pull-up on/off	VDDIO1	
D8	VDDIO1	P	-	-	-	
D9	VSSIO1	P	-	-	-	
D10	VDDcore	P	-	-	-	
D11	VSScore	P	-	-	-	
D12	A[19]	O	MO02	2mA out	VDDIO1	
D13	VSSIO1	P	-	-	-	
D14	VDDIO1	P	-	-	-	
D15	CKE	O	MO08	8mA out	VDDIO1	
D16	WE1_	O	MO08	8mA out	VDDIO1	

Ball#	Signal Name	I/O	IO Cell	IO Cell Characteristics	Power	Note
D17	D[3]	IO	MB08	8mA out	VDDIO1	
D18	RDWR_	O	MOL12	12mA out	VDDIO1	
D19	WE2_	O	MO08	8mA out	VDDIO1	
D20	WE3_	O	MO08	8mA out	VDDIO1	
E1	LCD_D[7]/GP47	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
E2	LCD_D[13]/GP53	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
E3	LCD_D[15]/GP55	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
E4	MII_RXD3/GP124	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
E17	A[2]	O	MOL12	12mA out	VDDIO1	
E18	A[3]	O	MOL12	12mA out	VDDIO1	
E19	A[4]	O	MOL12	12mA out	VDDIO1	
E20	A[5]	O	MOL12	12mA out	VDDIO1	
F1	LCD_D[6]/GP46	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
F2	LCD_D[9]/GP49	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
F3	LCD_D[11]/GP51	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
F4	MII_TXD2/GP119	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
F17	A[6]	O	MOL12	12mA out	VDDIO1	
F18	A[7]	O	MOL12	12mA out	VDDIO1	
F19	A[8]	O	MOL12	12mA out	VDDIO1	
F20	A[9]	O	MOL12	12mA out	VDDIO1	
G1	LCD_D[2]/GP42	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
G2	LCD_D[4]/GP44	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
G3	LCD_D[8]/GP48	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
G4	VSSIO2	P	-	-	-	
G17	A[10]	O	MOL12	12mA out	VDDIO1	
G18	A[11]	O	MOL12	12mA out	VDDIO1	
G19	A[12]	O	MOL12	12mA out	VDDIO1	
G20	A[13]	O	MOL12	12mA out	VDDIO1	
H1	LCD_PCLK/GP58	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
H2	LCD_D[1]/GP41	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
H3	LCD_D[5]/GP45	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
H4	VDDIO2	P	-	-	-	
H17	VSSIO1	P	-	-	-	
H18	A[14]	O	MOL12	12mA out	VDDIO1	
H19	A[15]	O	MOL12	12mA out	VDDIO1	
H20	A[16]	O	MOL12	12mA out	VDDIO1	
J1	LCD_VSYNC/GP56	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
J2	LCD_HSYNC/GP57	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
J3	LCD_D[0]/GP40	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
J4	LCD_D[3]/GP43	IO	DW04	4mA out, pull-up, pull-up on/off	VDDIO2	
J17	VDDIO1	P	-	-	-	

Ball#	Signal Name	I/O	IO Cell	IO Cell Characteristics	Power	Note
J18	D[16]	IO	MB08	8mA out	VDDIO1	
J19	D[17]	IO	MB08	8mA out	VDDIO1	
J20	D[18]	IO	MB08	8mA out	VDDIO1	
K1	LCD_CLS/GP61	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
K2	LCD_SPL/GP60	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
K3	LCD_DE/GP59	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
K4	VSScore	P	-	-	-	
K17	VDDcore	P	-	-	-	
K18	D[19]	IO	MB08	8mA out	VDDIO1	
K19	D[20]	IO	MB08	8mA out	VDDIO1	
K20	D[21]	IO	MB08	8mA out	VDDIO1	
L1	LCD_PS/GP62	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
L2	LCD_REV/GP63	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
L3	TAP_MD	I	IDS	Schmitt, pull-down	VDDIO2	
L4	VDDcore	P	-	-	-	
L17	VSScore	P	-	-	-	
L18	D[22]	IO	MB08	8mA out	VDDIO1	
L19	D[23]	IO	MB08	8mA out	VDDIO1	
L20	D[24]	IO	MB08	8mA out	VDDIO1	
M1	CIM_D[0]/GP0	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
M2	CIM_D[1]/GP1	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
M3	CIM_D[2]/GP2	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
M4	CIM_D[3]/GP3	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
M17	D[25]	IO	MB08	8mA out	VDDIO1	
M18	D[26]	IO	MB08	8mA out	VDDIO1	
M19	D[27]	IO	MB08	8mA out	VDDIO1	
M20	D[28]	IO	MB08	8mA out	VDDIO1	
N1	CIM_D[4]/GP4	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
N2	CIM_D[5]/GP5	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
N3	CIM_D[6]/GP6	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
N4	CIM_D[7]/GP7	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
N17	D[29]	IO	MB08	8mA out	VDDIO1	
N18	D[30]	IO	MB08	8mA out	VDDIO1	
N19	D[31]	IO	MB08	8mA out	VDDIO1	
N20	IOIS16_	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO1	
P1	CIM_MCLK/GP11	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
P2	CIM_PCLK/GP10	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	
P3	CIM_HSYNC/GP9	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
P4	CIM_VSYNC/GP8	IO	DW04	4mA out, pull-down, pull-down on/off	VDDIO2	

Ball#	Signal Name	I/O	IO Cell	IO Cell Characteristics	Power	Note
P17	VSSIO2	P	-	-	-	
P18	PCE2_/GP93	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO1	
P19	PCE1_/GP90	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO1	
P20	PSKTSEL/GP91	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO1	
R1	TEST_MD	I	IDS	Schmitt, pull-down	VDDIO2	
R2	VDDcore	P	-	-	-	
R3	USB_CLK/GP28	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
R4	VSScore	P	-	-	-	
R17	VDDIO1	P	-	-	-	
R18	INPACK_/GP88	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO1	
R19	PBVD2/GP89	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO1	
R20	UART0_TXD/GP127	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO1	
T1	OVC0	I	IS	Schmitt	VDDIO2	
T2	PPWR0/GP29	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
T3	DPLS1	IO	USB 1.1 PHY		VDDusb	
T4	DMNS1	IO	USB 1.1 PHY		VDDusb	
T17	NC	-	-	-	-	
T18	UART1_RXD/GP24	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
T19	UART2_RXD/GP111	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
T20	UART1_TXD/GP25	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
U1	DPLS0	A IO	USB 1.1 PHY		VDDusb	
U2	DMNS0	A IO	USB 1.1 PHY		VDDusb	
U3	VSSusb	P	-	-	-	
U4	NC	-	-	-	-	
U5	XTAL	AO	OSCO	Oscillator output	VDDIO2	
U6	TDO	O	T04	4mA out	VDDIO2	
U7	TRSTN_	I	IDS	Schmitt, pull-down	VDDIO2	
U8	SSI_DR/GP75	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
U9	VDDIO2	P	-	-	-	
U10	VSSIO2	P	-	-	-	
U11	VDDcore	P	-	-	-	
U12	VSScore	P	-	-	-	
U13	GP99	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
U14	GP108	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
U15	MSC_CMD/GP38	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
U16	MSC_DAT[1]/GP35	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
U17	NC	-	-	-	-	
U18	UART3_TXD/GP21	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	

Ball#	Signal Name	I/O	IO Cell	IO Cell Characteristics	Power	Note
U19	UART3_RXD/GP16	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
U20	UART0_RXD/GP126	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V1	VDDusb	P	-	-	-	
V2	VSSpll	P	-	-	-	
V3	NC	-	-	-	-	
V4	EXTAL	AI	OSCI	Oscillator input	VDDIO2	
V5	I2C_SCK	O	B04	4mA out	VDDIO2	
V6	TCK	I	IDS	Schmitt, pull-down	VDDIO2	
V7	BOOT_SEL[2]	I	IDS	Schmitt, pull-down	VDDIO2	
V8	SSI_CE1_/GP73	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V9	SYSCLK/GP68	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V10	SYNC/GP78	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V11	PWM1/GP95	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V12	SCC0_DATA/GP64	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
V13	GP103	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V14	GP98	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V15	GP109	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V16	GP105	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V17	MSC_DAT[3]/GP37	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
V18	UART3_RTS_/GP23	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
V19	NC	-	-	-	-	
V20	UART2_TXD/GP125	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W1	VDDpll	P	-	-	-	
W2	RTCCLK	I	ICD	Pull-down, pull-down on/off	VDDIO2	
W3	RESETP_	I	IS	Schmitt	VDDIO2	
W4	RESETOUT_	O	O04	4mA out	VDDIO2	
W5	TDI	I	IUS	Schmitt, pull-up	VDDIO2	
W6	BOOT_SEL[0]	I	IDS	Schmitt, pull-down	VDDIO2	
W7	BOOT_SEL[1]	I	IDS	Schmitt, pull-down	VDDIO2	
W8	SSI_DT/GP74	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W9	SDATA_OUT/GP70	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W10	ACRESET_/GP69	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W11	PS2_CLK/GP32	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W12	SCC0_CLK/GP66	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
W13	SCC1_DATA/GP65	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
W14	GP101	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W15	GP97	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W16	GP106	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
W17	GP104	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	

Ball#	Signal Name	I/O	IO Cell	IO Cell Characteristics	Power	Note
W18	MSC_DAT[0]/GP34	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
W19	NC	-	-	-	-	
W20	UART3_CTS_/GP17	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y1	NC	-	-	-	-	
Y2	NC	-	-	-	-	
Y3	NC	-	-	-	-	
Y4	I2C_SDA	O	B04	4mA out	VDDIO2	
Y5	TMS	I	IUS	Schmitt, pull-up	VDDIO2	
Y6	BOOT_SEL[3]	I	IDS	Schmitt, pull-down	VDDIO2	
Y7	SSI_CE2_/GP76	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y8	SSI_CLK/GP72	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y9	BITCLK/GP77	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y10	SDATA_IN/GP71	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y11	PWM0/GP94	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
Y12	PS2_DATA/GP33	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y13	SCC1_CLK/GP67	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
Y14	GP102	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y15	GP100	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y16	GP96	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y17	GP110	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y18	GP107	IO	UW02	2mA out, pull-up, pull-up on/off	VDDIO2	
Y19	MSC_CLK/GP39	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	
Y20	MSC_DAT[2]/GP36	IO	UW04	4mA out, pull-up, pull-up on/off	VDDIO2	

Notes:

1. IO cells power supplied by VDDIO1 are regular IO cells. DC specification of them is described in Table 3-2 and Table 3-3
2. IO cells power supplied by VDDIO2 are standard IO cells. DC specification of them is described in Table 3-4
3. The meaning of phases in IO cell characteristics are
   a) 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12mA
   b) Pull-up: The IO cell contains a pull-up resistor
   c) Pull-down: The IO cell contains a pull-down resistor
   d) Pull-up on/off: The IO cell's pull-up resistor can be turned on or off by software. If this does not appear, the resistor is always on
   e) Pull-down on/off: The IO cell's pull-down resistor can be turned on or off by software. If this does not appear, the resistor is always on
   f) Schmitt: The IO cell is Schmitt trig input

3 Electrical Specifications

3.1 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

3.1.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
T_{stg}	Storage Temperature	-65	125	°C
T_{opt}	Operation Temperature	-40	125	°C
	VDDIO1 power supplies voltage	-0.5	4.6	V
	VDDIO2 power supplies voltage	-0.5	4.6	V
	VDDUSB power supplies voltage	-0.5	4.6	V
	VDDcore power supplies voltage	-0.5	2.5	V
	VDDPLL power supplies voltage	-0.5	2.5	V
VI_{IO1}	Input voltage to VDDIO1 supplied non-supply pins	-0.5	4.6	V
VI_{IO2}	Input voltage to VDDIO2 supplied non-supply pins	-0.5	6.0	V
VI_{USB}	Input voltage to VDDUSB supplied non-supply pins	-0.5	6.0	V
VO_{IO1}	Output voltage from VDDIO1 supplied non-supply pins	-0.5	4.6	V
VO_{IO2}	Output voltage from VDDIO2 supplied non-supply pins	-0.5	4.6	V
VO_{USB}	Output voltage from VDDUSB supplied non-supply pins	-0.5	4.6	V
V_{ESD}	Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.1.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for VDDIO1 pins in 3.3V application

Symbol	Description	Min	Typical	Max	Unit
V_{IO1}	VDDIO1 voltage	2.97	3.3	3.63	V
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_T	Threshold point	1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point	1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.88	0.94	0.99	V
I_L	Input Leakage Current			±10	μA
I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	50	65	100	kΩ
R_{PD}	Pull-down Resistor	40	56	107	kΩ
V_{OL}	Output low voltage @I_{OL}=2, 4, 8, 12mA			0.4	V
V_{OH}	Output high voltage @I_{OH}=2, 4, 8, 12mA	2.4			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	2.2	3.7	4.6	
	4mA	4.4	7.4	9.2	
	8mA	8.9	14.7	18.4	
	12mA	13.3	22.1	27.5	
I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	2.5	5.1	7.9	
	4mA	5.0	10.2	15.9	
	8mA	10.0	20.4	31.7	
	12mA	15.0	30.6	47.6	

Table 3-3 Recommended operating conditions for VDDIO1 pins in 1.8V application

Symbol	Description	Min	Typical	Max	Unit
V_{IO1}	VDDIO1 voltage	1.62	1.8	1.98	V
V_{IH}	Input high voltage	0.65 * V_{IO1}		V_{IO1} + 0.3	V
V_{IL}	Input low voltage	-0.3		0.35 * V_{IO1}	V
V_T	Threshold point	0.87	0.92	0.98	V
V_{T+}	Schmitt trig low to high threshold point	0.95	0.99	1.00	V
V_{T-}	Schmitt trig high to low threshold point	0.56	0.58	0.60	V
I_L	Input Leakage Current			±10	μA

I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	94	148	261	kΩ
R_{PD}	Pull-down Resistor	77	135	312	kΩ
V_{OL}	Output low voltage @I_{OL}=2, 4, 8, 12mA			0.45	V
V_{OH}	Output high voltage @I_{OH}=2, 4, 8, 12mA	V_{IO1} – 0.45			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	0.9	1.9	3.0	
	4mA	1.8	3.8	6.0	
	8mA	3.6	7.6	12.0	
	12mA	5.4	11.4	18.0	
I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	0.9	1.6	2.2	
	4mA	1.8	3.1	4.5	
	8mA	3.7	6.2	9.0	
	12mA	5.5	9.3	13.4	

Table 3-4 Recommended operating conditions for VDDIO2 pins

Symbol	Description	Min	Typical	Max	Unit
V_{IO2}	VDDIO2 voltage	2.97	3.3	3.63	V
V_{IH}	Input high voltage	2.0		5.5	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_T	Threshold point	1.45	1.58	1.74	V
V_{T+}	Schmitt trig low to high threshold point	1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.88	0.94	0.99	V
I_L	Input Leakage Current			±10	μA
I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	39	65	116	kΩ
R_{PD}	Pull-down Resistor	40	56	108	kΩ
V_{OL}	Output low voltage @I_{OL}=2, 4mA			0.4	V
V_{OH}	Output high voltage @I_{OH}=2, 4mA	2.4			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	2.4	4.0	5.0	
	4mA	4.7	8.0	10.0	
I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	2.8	5.9	9.5	
	4mA	5.6	11.9	19	

Table 3-5 Recommended operating conditions for VDDUSB pins

Symbol	Description	Min	Typical	Max	Unit

V_{USB}	VDDUSB voltage	2.97	3.3	3.63	V
V_{ILH}	Input voltage range	0		V_{USB}	V
V_{OLH}	Output voltage range	0		V_{USB}	V
V_{DI}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single ended receiver threshold	0.8		2.0	V
I_{OZ}	Tri-State leakage current			±10	μA
Z_{DRV}	Driver output resistance, including damping resistor	24		44	Ω
V_{OL}	Static output low voltage			0.3	V
V_{OH}	Static output high voltage	2.8			V

Table 3-6 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		70	°C
V_{CORE}	Core voltage	1.62	1.8	1.98	V
V_{PLL}	PLL analog voltage	1.62	1.8	1.98	V

3.1.3 Power Consumption Specifications

Power consumption depends on the operating voltage, peripherals enabled, external switching activity, and external loading.

The maximum power consumption specification is determined by all units running at their maximum: processor speed, voltage, and loading conditions. This method generates a conservative power consumption value; however, power supply and thermal management design requires the highest possible power consumption for robust design. The Jz4730 processor's maximum power consumption is calculated using the following conditions:

- All peripheral units operating at maximum frequency and size configuration
- All I/O loads maximum (50pF for Memory interface, 100pF for peripherals)
- Core operating at worst case power scenario (hit rates adjusted for worst power)
- All voltages at maximum of range

Do not exceed the maximum package power rating or T_{case} temperature.

But for most of applications, a more optimal system design requires more typical power-consumption figures. These figures are important when considering battery size and

optimizing regulator efficiency. Typical systems operate with fewer modules active and at nominal voltage and load. The typical power consumption for the Jz4730 processor is calculated using these conditions:

- All voltage at nominal value
- Nominal case temperature

Table 3-7 Power Consumption Specifications

Symbol	Description	Typical	Max	Unit
400MHz normal mode; Maximum: V(core)= 2.2V, V(IO1)=V, V(IO2)=3.6V, Temp=100°C Typical: V(core)=1.8V, V(IO1)=1.8V, V(IO2)=3.3V, Temp=Room				
				mW
				mW
				mW
				mW
				mW
				mW
				mW
				mW
				mW

3.2 AC Specifications

A pin's AC Characteristics include input and output capacitance. These determine loading for external drivers or other load analysis. The AC Characteristics also include a de-rating factor, which indicates how much faster or slower the AC timings get with different loads. The AC Operating Conditions for all input, output, and I/O pins are shown in Table 3-8. All AC specification values are valid for entire temperature range of the device.

Table 3-8 Standard Input, Output, and I/O Pin AC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
C_{IN}	Input Capacitance, all input and IO pins	3	5	10	pF
C_{OUT_G12}	Output Capacitance, 12mA output and IO pins				pF
C_{OUT_G8}	Output Capacitance, 8mA SDRAM output and IO pins				pF

NOTE: AC Specifications guaranteed for loads in this range. All testing is done at 50pF

3.3 Oscillator Electrical Specifications

The processor contains two oscillators, each for a specific crystal: a 32.768KHz oscillator and a 3.6864MHz oscillator. When choosing a crystal, match the crystal parameters as closely as possible.

3.3.1 32.768KHz Oscillator Specifications

3.3.2 3.6864MHz Oscillator Specifications

3.4 Reset and Power AC Timing Specifications

The Jz4730 processor asserts the RESETOUT_ pin in one of several modes:

- Power On Reset (RESETP_)
- Watch Dog Reset (internal controlled)

The following sections provide the timing and specifications for the entry and exit of these modes.

3.4.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the Jz4730 processor with a specific sequence of power and resets to ensure proper operation. ? shows this sequence and is detailed in ?.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1. VDDIO1 & VDDIO2 & VDDUSB
2. VDDCORE & VDDPLL

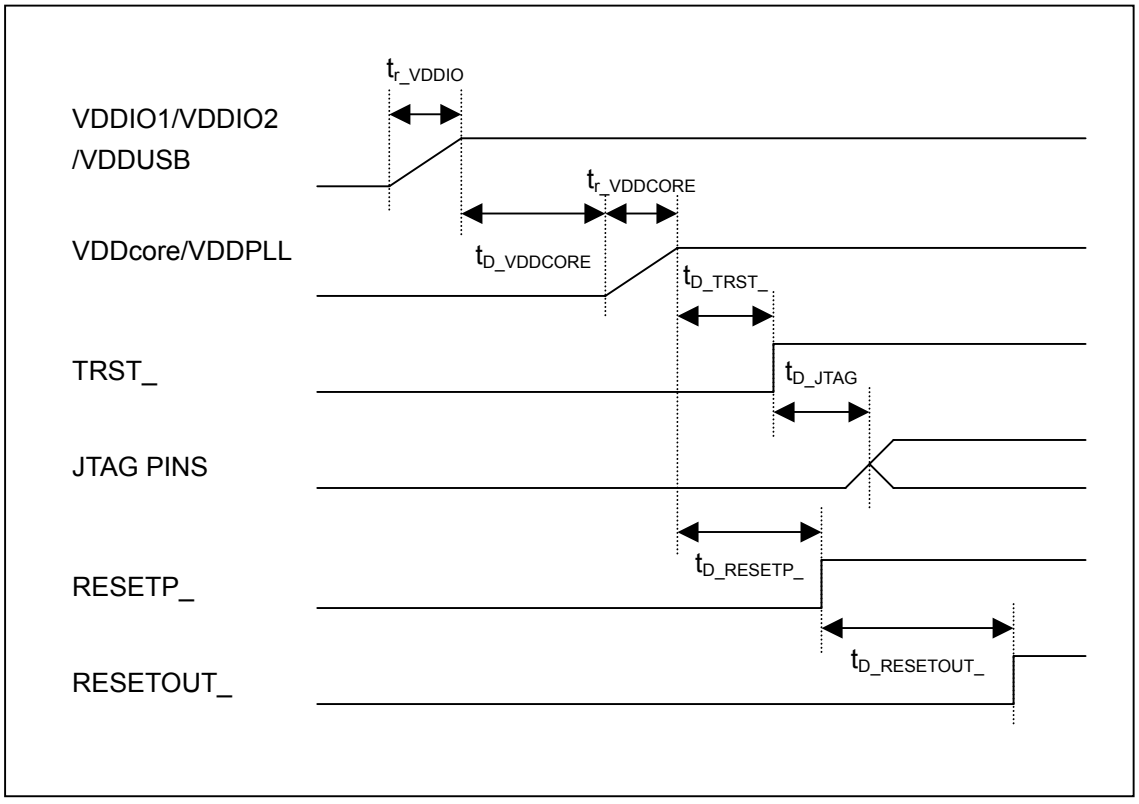


Figure 3-1 Power-On Timing Diagram

Table 3-9 Power-On Timing Parameters

Symbol	Description	Min	Typical	Max	Unit
t_{r_VDDIO}	VDDIO1/VDDIO2/VDDUSB Rise / Stabilization time	0.01	–	100	ms
$t_{D\_VDDCORE}$	Delay between VDDIO1/VDDIO2/VDDUSB stable and VDDCORE/VDDPLL applied	0	–	–	ms
$t_{r\_VDDOCRE}$	VDDOCRE/VDDPLL Rise / Stabilization time	0.01	–	100	ms
$t_{D\_TRST\_}$	Delay between VDDCORE, VDDPLL stable and JTAG reset TRST_ deasserted	10	–	–	ns
t_{D_JTAG}	Delay between TRST_ deasserted and other JATG pins active	10	–	–	ns
$t_{D\_RESETP\_}$	Delay between VDDCORE, VDDPLL stable and RESETP_ deasserted	0.2(1)	–	–	ms
$t_{D\_RESETOUT\_}$	Delay between RESETP_ deasserted and RESETOUT_ deasserted	117.2	–	117.3	ms

3.4.2 Hardware Reset Timing

The timing sequences for input signals RESETP_ and output signals RESETOUT_, are shown in Figure 3-2 and Table 3-10, assumes the power supplies are stable at the assertion of RESETP_.

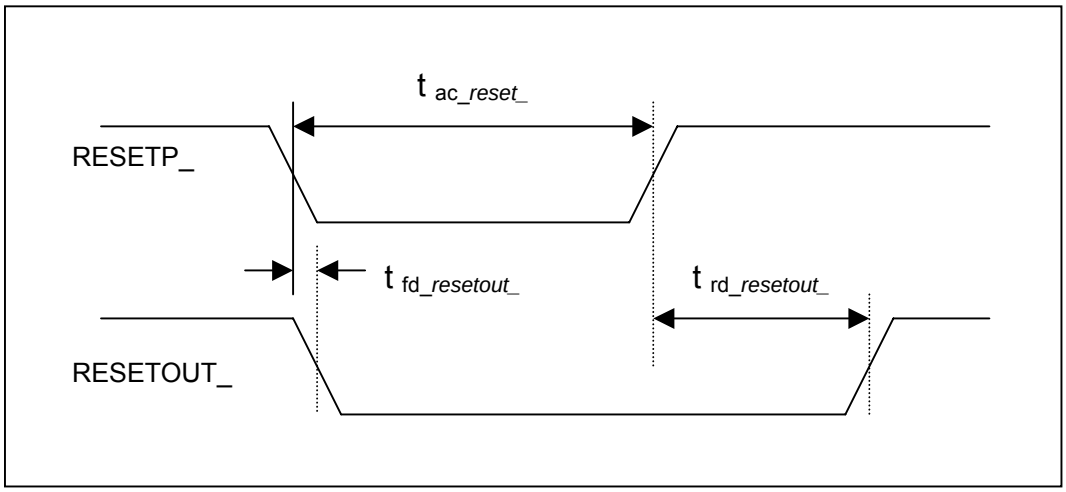


Figure 3-2 Hardware Reset Timing Diagram

Table 3-10 RESETP_ to RESETOUT_ Timing Parameters

Symbol	Description	Min	Typical	Max	Unit
$t_{ac\_RESETP\_}$	Minimum assertion time of RESETP_	0.2(1)	–	–	ms
$t_{fd\_RESETOUT\_}$	Delay between RESETP_ Asserted and RESETOUT_ Asserted	3	7	20	ns
$t_{rd\_RESETOUT\_}$	Delay between RESETP_ deasserted and RESETOUT_ deasserted	117.2	–	117.3	ms

3.5 Memory Bus and PCMCIA AC Specifications

This section provides the timing information for these types of memory:

- SRAM / ROM / Flash
- Card interface (PCMCIA or Compact Flash)
- SDRAM

3.6 Peripheral Module AC Specifications

3.6.1 LCD Module Timing

3.6.2 CIM Module Timing

3.6.3 SPI Module Timing

3.6.4 External DMA Request and Grant