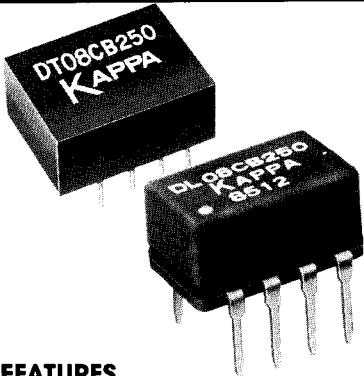


**SERIES DL08CB/DT08CB TTL SCHOTTKY  
5-TAP TTL DELAY LINE (8-PIN)**



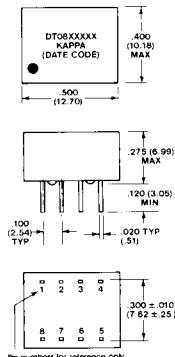
## FEATURES

- TTL Schottky Interfaced
  - 8-pin package
  - 5 equally-spaced taps
  - Total delays from 25-1000 ns

## **MARKINGS AND DIMENSIONS, in (mm)**

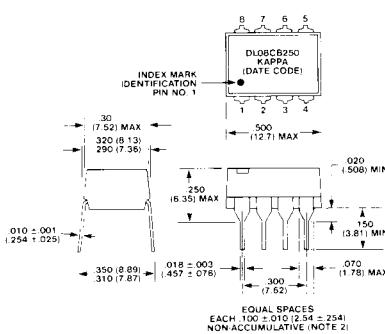
RECOMMENDED OPERATING CONDITIONS		MIN	TYP	MAX	UNIT
$V_{CC}$	Supply Voltage	4.75	5.00	5.25	V
$V_{IH}$	High-Level Input Voltage	2.0			V
$V_{IL}$	Low-Level Input Voltage			0.8	V
$I_{IK}$	Input Clamp Current			-18	mA
$I_{OH}$	High-Level Output Current			-1.0	mA
$I_{OL}$	Low-Level Output Current			20	mA
$T_A$	Operating Free-Air Temperature	0	+25	+70	°C

DC ELECTRICAL CHARACTERISTICS		TEST CONDITIONS			
$V_{OH}$	High-Level Output Voltage	$V_{CC} = \text{min.}$ , $V_{IH} = \text{min.}$ , $I_{OH} = \text{max.}$	2.7	3.4	V
$V_{OL}$	Low-Level Output Voltage	$V_{CC} = \text{min.}$ , $V_{IL} = \text{max.}$ , $I_{OL} = \text{max.}$		0.5	V
$V_{IK}$	Input Clamp Voltage	$V_{CC} = \text{min.}$ , $I_i = I_{IK}$		-1.2	V
$I_{IH}$	High-Level Input Current	$V_{CC} = \text{max.}$ , $V_{IN} = 2.7V$		50	$\mu A$
$I_{IL}$	Low-Level Input Current	$V_{CC} = \text{max.}$ , $V_{IN} = 5.25V$		1.0	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{max.}$ , $V_{IN} = 0.5V$		-2	mA
		$V_{CC} = \text{max.}$ , $V_{OUT} = 0,$ one output at a time	-40	-100	mA
$I_{CH}$	High-Level Supply Current	$V_{CC} = \text{max.}$ , $V_{IN} = \text{OPEN}$		30	mA
$I_{CL}$	Low-Level Supply Current	$V_{CC} = \text{max.}$ , $V_{IN} = 0$		65	mA
$N_H$	Fanout High-Level Output	$V_{CC} = \text{max.}$ , $V_{OH} = 2.7V$		20	TTL load
$N_L$	Fanout Low-Level Output	$V_{CC} = \text{max.}$ , $V_{OL} = 0.5V$		10	TTL load

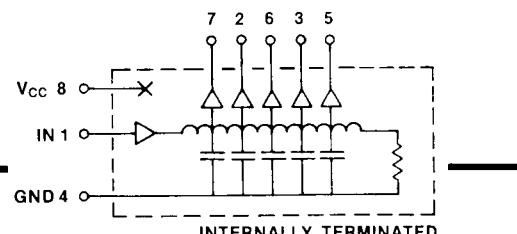


AC ELECTRICAL CHARACTERISTICS						
$T_{PLH}$ Low-to-High Level Delay Time	$V_{CC} = typ$ , $T_A = typ$ , $E_{IN} = typ$ $T_W = typ$ , $d = typ(1)(2)(6)$	-5		+5	%	
$T_{PCC}$ $V_{CC}$ Coefficient of Delay	$V_{CC} = min\text{-to-}max$ , $T_A = typ$ $E_{IN} = typ$ , $T_W = typ$ , $d = typ(1)(2)(4)(6)$		-.016		%/mV	
$T_{RO}$ Output Risetime	$V_{CC} = typ$ , $T_A = typ$ , $E_{IN} = typ$ $T_W = typ$ , $d = typ(5)(6)$		3	4	ns	

INPUT PULSE TEST CONDITIONS		3.1	3.2	3.3	V
$E_{IN}$	Pulse Voltage				
$T_{RI}$	Pulse Rise-Time			2.0	ns
$T_W$	Pulse Width, or Total Delay	40	100		%
d	Duty Cycle		33.3	50	%



PART NUMBER <sup>(7)</sup>	Total Delay (ns) <sup>(1) (2)</sup>	Tap Delay (ns) <sup>(1) (2)</sup>	Notes:
DL08/DT08CB250	25	5	1. Delays measured at 1.5V level on leading edge only. 2. Delay tolerances: $\pm 5\%$ or $\pm 2$ ns, whichever is greater, referenced from input and guaranteed only under the following test conditions: $V_{CC} = TYP.$ , $T_A = TYP.$ , $E_{IN} = TYP.$ , $T_{RI} = MAX.$ , $T_W = TYP.$ , $P_{RR} = 1MHz$ (or d/tw, whichever is less), $RL = 1$ megohm and $CL = 2pf$ .
DL08/DT08CB500	50	10	
DL08/DT08CB750	75	15	3. Temperature coefficient of delay will vary, depending upon total delay, according to the formula: $T_{PTA} = (100 + (25,000/T_{PLH}))$ .
DL08/DT08CB101	100	20	4. Delay will vary about 4% for every 5% change in supply voltage.
DL08/DT08CB251	250	50	5. Risetime measured from 0.75V to 2.4V level.
DL08/DT08CB501	500	100	6. Measured with no loads on taps. 7. Other delays also available upon request.



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