M02069

3.3 or 5 Volt VCSEL/FP Laser Driver IC for Applications to 4.3 Gbps

The M02069 is a highly integrated, programmable VCSEL driver intended for SFP/SFF modules to 4.3 Gbps. Using differential PECL data inputs, the M02069 supplies the bias and modulation current required to drive a VCSEL or edge-emitting laser. The modulation output can be AC or DC-coupled to a FP laser diode or AC coupled to a common anode or common cathode VCSEL

Peaking adjustment is available to improve VCSEL fall time.

EPON burst mode operation is supported with no extra components.

Integrated safety circuitry detects faults and provides latched bias and modulation current shutdown.

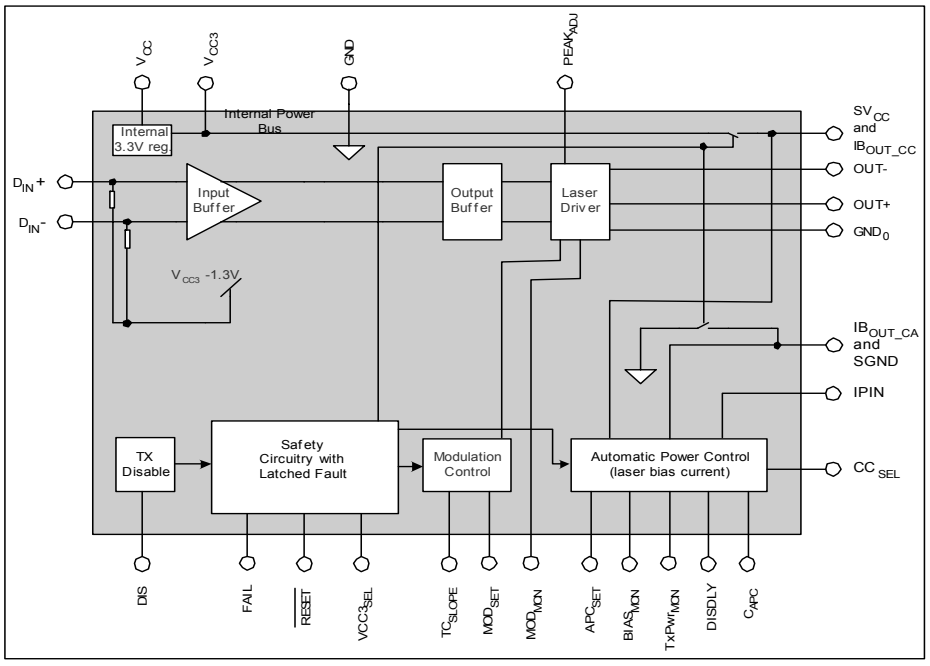
Applications

- EPON FTTH modules
- Gigabit Ethernet modules
- 1G/2G/4G Fibre Channel modules

Features

- High speed operation; suitable for SFP/SFF applications from 155Mbps to 4.3 Gbps.
- Supports Common Anode VCSEL, Common Cathode VCSEL, or FP LASER. May be used with or without a monitor photodiode.
- Programmable temperature compensation. Modulation output and bias output can be controlled using the programmable module controller M02080 or a few discrete resistors.
- Supports DDMI (SFF-8472) diagnostics.
- DC or AC coupled modulation drive.
- Peaking circuit to optimize VCSEL response.
- Low overshoot allows high extinction ratio with low jitter.
- Supports E-PON burst mode with no extra components
- Automatic Laser Power Control, with “Slow-Start”.
- 3.3V or 5V operation

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Temperature
M02069-11	QFN24	
M02069-EVM	Combination Electrical and Optical Evaluation board	

Revision History

Revision	Level	Date	ASIC Revision	Description
A	Advance	October 2003	x	Initial Release.
B	Advance	November 2003	x	Revision B Release.
C	Preliminary	February 2004	x	Revision C Release, Preliminary.

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1.0 Functional Description

1.1 Overview

The M02069 is a highly integrated laser driver intended for applications to 4.3 Gbps.

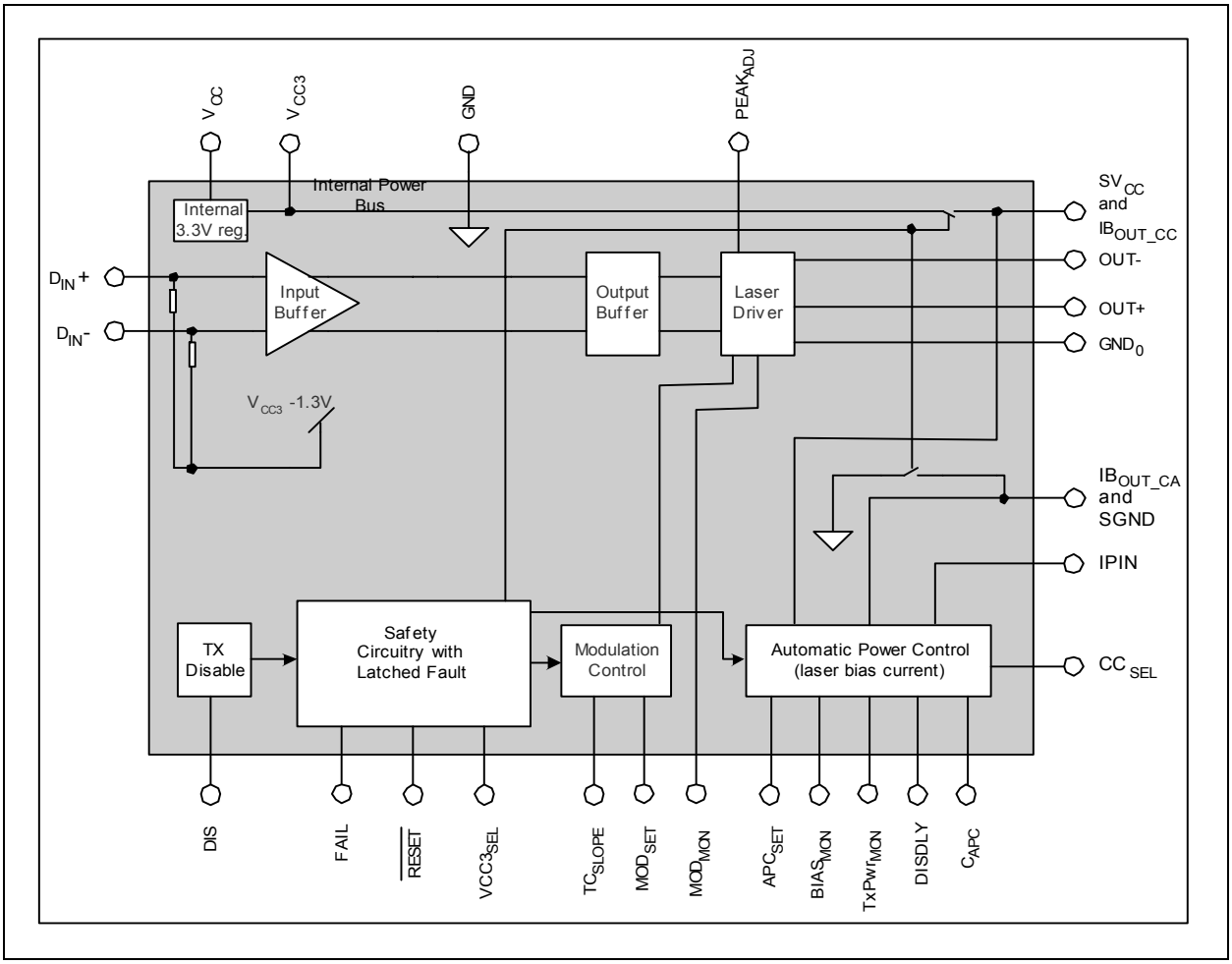
Many features are user-adjustable, including common anode or common cathode laser mode, the APC (automatic power control) loop bias control (via a monitor photodiode), modulation current, temperature compensation control of modulation current, and peaking adjustment. The part may be operated from a 3.3V or 5V supply.

For E-PON and other burst-mode applications, the part supports fast and accurate turn-on and turn-off of the laser bias and modulation currents.

Safety circuitry is also included to provide a latched shut-down of laser bias and modulation current if a fault condition occurs. An internal VCC switch provides redundant shutdown when operating the device in common anode configuration. An internal ground switch provides redundant shutdown when operating the device in common cathode configuration.

Modulation, bias, and transmit power monitor current mirrors are provided for DDMI applications and allow monitoring without disturbing the analog signal path.

Figure 1-1. M02069 Block Diagram Example



1.2 Features

- High speed operation; suitable for SFP/SFF applications from 155Mbps to 4.3 Gbps.
- Supports Common Anode VCSEL, Common Cathode VCSEL, or FP LASER. May be used with or without a monitor photodiode.
- Programmable temperature compensation. Modulation output and bias output can be controlled using the programmable module controller M02080 or a few discrete resistors.
- Supports DDMI (SFF-8472) diagnostics.
- DC or AC coupled modulation drive.
- Peaking circuit to optimize VCSEL response.
- Low overshoot allows high extinction ratio with low jitter.
- Supports E-PON burst mode with no extra components
- Automatic Laser Power Control, with “Slow-Start”.
- 3.3V or 5V operation

1.3 General Description

1.3.1 Detailed Description

The M02069 laser driver consists of the following circuitry: an internal regulator, common anode/common cathode configuration control, bias current generator and automatic power control, data inputs, peaking adjust, modulation current control, modulator output, laser fail indication, disable control, and monitor outputs for the bias current, modulation current, and transmitted power.

1.3.2 Internal Regulator

The M02069 contains an internal 3.3V regulator so high bit rate performance can be achieved with 5V or 3.3V power supply.

When operating from a 5V supply (V_{CC} is connected to +5V), an internal regulator provides a voltage of approximately 3.3V to the majority of the on-chip circuitry. The on-chip regulator is internally compensated, requiring no external components. When a 3.3V supply is used (V_{CC} and V_{CC3} connected to 3.3V) the regulator is switched off and the internal circuitry is powered directly through the V_{CC3} supply pin. The decision as to whether or not the internal regulator is required is made via the $VCC3_{SEL}$ pin, which also determines whether the safety circuitry needs to monitor for proper +5V supply voltage.

SV_{CC} is sourced from V_{CC3} through a switch for common anode applications (this pin becomes IB_{OUT_CC} in common cathode applications). When a fault condition is present, FAIL will assert and the switch sourcing SV_{CC} will open so no current can pass through the laser. SV_{CC} does not need any external capacitance, if capacitance to ground is added at SV_{CC} it should be less than or equal to 100pF.

V_{CC} and V_{CC3} status are internally monitored by the M02069 during power-up and normal operation. During power-up the "slow-start" circuitry requires that V_{CC} and V_{CC3} each reach an acceptable level before enabling bias or modulation current.

Table 1-1. Pin Connection for 3.3V and 5V V_{CC}

		Pin Connection For:	
		V_{CC} = 3.3V	**V_{CC} = 5V**
Pins Dependent on V_{CC} Voltage	**V_{CC3} (pin 21)**	Connect to V_{CC}	Reference for C_{APC} and $PEAK_{ADJ}$
	C_{APC} (pin 20)	Capacitor between C_{APC} and V_{CC3} or V_{CC}	Capacitor between C_{APC} and V_{CC3} (not V_{CC})
	$PEAK_{ADJ}$ (pin 22)	Connect to V_{CC3} or V_{CC} to disable	Connect to V_{CC3} to disable (not V_{CC})
	$VCC3_{SEL}$ (pin 4)	Connect to V_{CC3} or V_{CC}	Connect to GND

1.3.3 Common Cathode/Common Anode Configuration Control

When CC_{SEL} is programmed high, the M02069 is configured for common cathode lasers. When CC_{SEL} is low, the M02069 is configured for common anode lasers.

The state of the CC_{SEL} pin determines:

1. whether bias current is sourced or sunk
2. whether monitor photodiode current is sunk or sourced
3. whether internal termination resistors at OUT+ and OUT- are active
4. whether the redundant safety switch disconnects VCC or GND from the output circuitry.

The affected pins are OUT+, OUT-, SV_{CC}/IB_{OUTCC}, and $SGND/IB_{OUTCA}$. The Table 1-2 below shows the configuration of each pin for the 2 states of CC_{SEL}.

Table 1-2. Pin Connection for Common Anode and Common Cathode Laser Modes

			Pin Connection When:	
			CC_{SEL} = High	CC_{SEL} = Low
Pins Dependent on CC_{SEL} Setting	Pin 18	SV_{CC}	Inactive	Supply for laser and all output load components.
		IB_{OUTCC}	Laser bias source current. Also add 1.5k ohm to ground at this pin for correct safety logic power-up timing.	Inactive
	Pin 14	SGND	Ground for laser and all output load components	Inactive
		IB_{OUTCA}	Inactive	Laser bias sink current.
	Pin 13	I_{PIN}	Monitor photodiode source current	Monitor photodiode sink current
	Pin 22	$PEAK_{ADJ}$	Controls Negative going edge of OUT-	Controls Negative going edge of OUT-, (do not use)
	Internal 50Ω pull-up resistors on OUT+ and OUT-		Active	Inactive
	Ratio of Bias current to $BIAS_{MON}$ current		15:1	50:1
	Ratio of Modulation current to MOD_{MON} current		30:1	65:1

1.3.4 Bias Current Generator and Automatic Power Control

The M02069 can either source or sink bias current for the laser diode depending on whether it is in common anode or common cathode mode. In common cathode mode (CC_{SEL} high) IB_{OUTCC} will source current. In common anode mode (CC_{SEL} low) IB_{OUTCA} will sink current.

Regardless of whether the M02069 is configured for common anode or common cathode mode, the following information applies.

To maintain constant average optical power, the M02069 incorporates a control loop to compensate for the changes in laser threshold current over temperature and lifetime. The bias current will be determined by the value of the external resistor R_{APCSET} and the transfer efficiency between the laser and monitor photodiode.

The photo current from the monitor photodiode mounted in the laser package is sunk or sourced at I_{PIN}. This photo current is mirrored and an equivalent current is sourced from pins $TxPwr_{MON}$ and APC_{SET}. The APC loop adjusts the laser bias current (hence the monitor diode photo current) to maintain a voltage of 1.3V at APC_{SET}.

$R_{APCSET} * I_{PIN} = 1.3\ V$

The APC loop has a time constant determined by C_{APC}, R_{APCSET} and the transfer efficiency between the laser and monitor photodiode. The larger the C_{APC} capacitor the lower the bandwidth of the loop and the larger the R_{APCSET} resistor the lower the bandwidth of the loop.

In general, it is recommended that at least 2.2 nF of external capacitance be added externally between C_{APC} and V_{CC3} to assure loop stability. With use of a 2.2 nF capacitor, the bias current can reach 90% of its final value within 1 millisecond.

In Common Anode mode with a 2.2nF C_{APC} capacitor the APC loop bandwidth is less than 30 kHz for almost all combinations of R_{APCSET} and transfer efficiency., which should be adequate for bit rates of 155Mbps. (and all higher bit rates).

In Common Cathode mode with a 2.2nF C_{APC} capacitor the APC loop bandwidth will be slightly higher, but should be less than 40 kHz for almost all combinations of R_{APCSET} and transfer efficiency. Contact the factory with your specific values of C_{APC}, R_{APCSET}, and transfer efficiency to determine the maximum APC loop bandwidth in your application.

The bias generator also includes a bias current monitor mirror ($BIAS_{MON}$), whose output current is typically 1/50th of the bias current in common anode mode (CCSEL = low) or 1/15th of the bias current in common cathode mode (CCSEL = high). This pin can be connected directly to an M02080 DDMI module controller or through a resistor to ground. If this function is not needed this pin can be left open.

The M02069 can be used without a monitor photodiode by connecting $BIAS_{MON}$ to APC_{SET} (*see Fig. 4)*. In this case the M02069 will increase the bias current (hence the $BIAS_{MON}$ current) to the laser until the voltage at APC_{SET} is approximately 1.3V.

1.3.5 Data Inputs

The inputs to the data buffers are self-biased through 4 kΩ resistors to an internal voltage VTT which is approximately V_{CC3} - 1.3V. Both CML and PECL inputs signals can be AC coupled to the M02069, or in 3.3V applications PECL inputs can be DC coupled to the data inputs. In most applications the data inputs are AC coupled with controlled impedance pcb traces which will need to be terminated externally with a 100Ω or 150Ω resistor between the + and - inputs.

1.3.6 Peak Adjust

Some VCSELs do not turn off quickly without peaking the negative going edge.

In common cathode applications, peaking on this edge can be added with a resistor connected between the $PEAK_{ADJ}$ input and GND. The amount of peaking is approximately

Peaking current = 5 * (1.3V / 2 KΩ + resistance to ground).

The resistance to ground should be between 2 KΩ and 20 KΩ. (Which will result in a peaking currents from 2.6mA to 260 μA.)

Peaking control can be disabled by connecting $PEAK_{ADJ}$ to V_{CC3}, resulting in no peaking current and reducing supply current by approximately 2 mA.

In common anode configuration the $PEAK_{ADJ}$ pin should be connected to V_{CC3}.

Note: Unlike the rest of the signal currents in the M02069, the output Peak Adjust current is unbalanced (single-sided drive). The designer should be aware that the use of peaking may result in unwanted EMI emissions. If EMI problems are traced to the use of peaking, high frequency decoupling (10pF capacitor or smaller) may be needed on the V_{CC} line.

1.3.7 Modulation Control

There are 2 programmable control lines for controlling the modulation current and its temperature compensation. These inputs can be programmed simply with a resistor to ground or they can be digitally controlled by the Mindspeed module controller M02080.

The modulation current amplitude is controlled by the MOD_{SET} input pin. The modulation current is temperature compensated by the TCSLOPE input.

If the temperature compensation at TCSLOPE is disabled, the modulation output current is simply:

IOUT = 42 x (1.28V / R_{MODSET}) when CC_{SEL} is low

and

IOUT = 22 x (1.28V / R_{MODSET}) when CC_{SEL} is high and a 50Ω VCSEL is used.

Where R_{MODSET} is the resistance from pin MOD_{SET} to ground.

To temperature compensate the modulation current, choose $R_{TCSLOPE}$ to meet the following relationship:

$R_{TCSLOPE} = 19.5*(TC)^{-1.5}$, where TC is the desired slope of the modulation current from 25°C to 85°C in%/°C and $R_{TCSLOPE}$ is in kΩ. If no temperature compensation is desired, leave $R_{TCSLOPE}$ open.

In any case, $R_{TCSLOPE}$ will have negligible effect at M02069 case temperatures below 10°C.

For example:

Given a common cathode VCSEL with a desired modulation current at low temperatures of 10mA and a temperature coefficient of -0.5%/°C at high temperatures (which will require a laser driver temperature coefficient of +0.5%).

Choose R_{MODSET} = 22 x (1.28V / 10mA) = 2.8kΩ.

Choose $R_{TCSLOPE}$ =19.5(0.5)$^{-1.5}$ kΩ = 55kΩ.*

1.3.8 Modulator (Figure 1-2)

The output stages OUT+ and OUT- are designed to drive 25Ω output loads over a wide range of currents and circuit architectures. The VCSEL may be a common anode or common cathode device. The output can be AC, DC, or Differentially coupled depending on the supply voltage and laser configuration.

In a common anode configuration with a VCSEL (Figure 1-5), OUT+ should be connected through a capacitor to the VCSEL. A pull-up resistor should be added in parallel to the VCSEL from SVCC to the OUT+ output. The dynamic impedance of the parallel combination of the VCSEL and pull-up resistor should be roughly 25 ohms. A 24 ohm pull-up resistor should also be added from SVCC to OUT- so the currents and voltage swings in the two outputs are balanced.

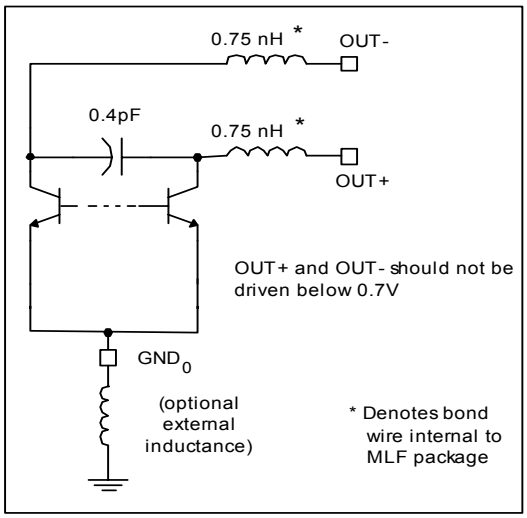
In a common anode configuration with a Fabry-Perot laser (Figure 1-8), OUT+ may be AC, DC, or Differentially coupled to the laser cathode. A resistor should be added in series with the laser such that the dynamic impedance of the series combination of the laser and resistor should be roughly 25 ohms. A 24 ohm pull-up resistor to SV_{CC} is needed on the OUT- output.

For common cathode operation with a VCSEL (Figure 1-6), internal 50 ohm terminations are switched in between the OUT+ and OUT- outputs and V_{CC3}. VCSELs with impedances from 25-75Ω can be simply AC coupled to the OUT- output with no additional load matching resistors. In this case OUT+ should be AC coupled to ground through 50Ω.

The VCSEL driver output stage is separately grounded from the rest of the circuitry (through GND_0). At higher data rates (above 2Gb/s) GND_0 may be connected to ground through a minimum of 2 nH of inductance to improve the

transient response. A ferrite can also provide the extra isolation (Murata BLM18HG471SN1 or equivalent recommended).

Figure 1-2. Modulator Output



1.3.9 Fail Output

The M02069 has a FAIL alarm output which is compatible with the TX_FAULT signalling requirements of common pluggable module standards.

The ESD protection on this pin provides a true open collector output that can withstand significant variation in V_{CC} when signalling between circuit boards. Also, if the M02069 loses power the FAIL output will signal a fail condition. In a simple static protection scheme used by other ICs the protection diodes would clamp the FAIL signal to ground when the chip loses power.

1.3.10 TX Disable and Disable Delay Control

The DIS pin is used to disable the transmit signal. When the transmit is disabled both the bias and modulation currents are off.

The DIS input is compatible with TTL levels regardless of whether VCC = 5V or VCC = 3.3V. In most module applications a pull-up resistor to VCC between 4.7kΩ and 10kΩ is required. Because this pin has an internal 7kΩ resistor to V_{CC}, no external pull-up resistor is required.

The DISDLY pin is used in conjunction with the DIS pin to control bias current enable time. (The modulation current enable time is always less than 600 ns). Unless the DISDLY pin is programmed for burst mode, the APC loop enable time will be slow (less than 1 ms with a C_{APC} = 2.2nF).

When a capacitor C is added to the DISDLY pin, the slow-start circuitry is disabled for typically

$T = 3 * 10^6$ (sec/F)* C (F)

following the DIS high transition. If DIS transitions low during this time, the bias current will quickly return to within 90% of its final value (within less than 500ns). If DIS transitions low after this time the slow-start circuitry will engage and the bias current will not return to its final value for approximately 1ms (depending on the C_{APC} capacitor).

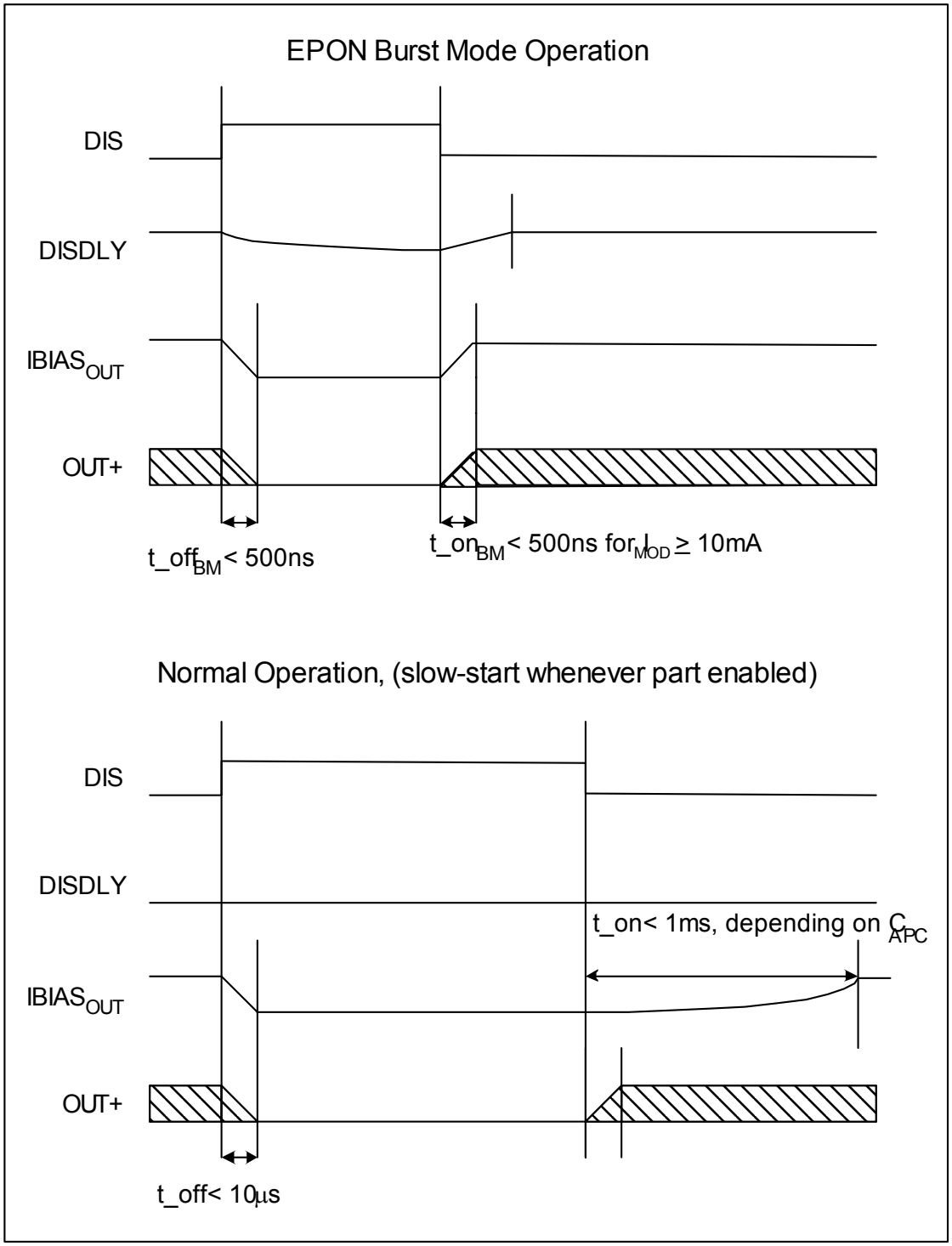
1.3.11 Burst Mode Operation (Figure 1-3)

The M02069 will meet the timing requirements of EPON with the addition of a capacitor at DISDLY (see paragraph above and Figure 1-3).

As shown in Figure 1-8, the laser should be DC coupled to OUT+. V_{CC} may be 3.3V or 5V.

If the M02069 is to be used in an APON or GPON application, external switches will be needed to satisfy the timing requirements. (See Mindspeed application note 0206X-APP-001.)

Figure 1-3. DIS and DISLY Timing



1.3.12 Current Monitors

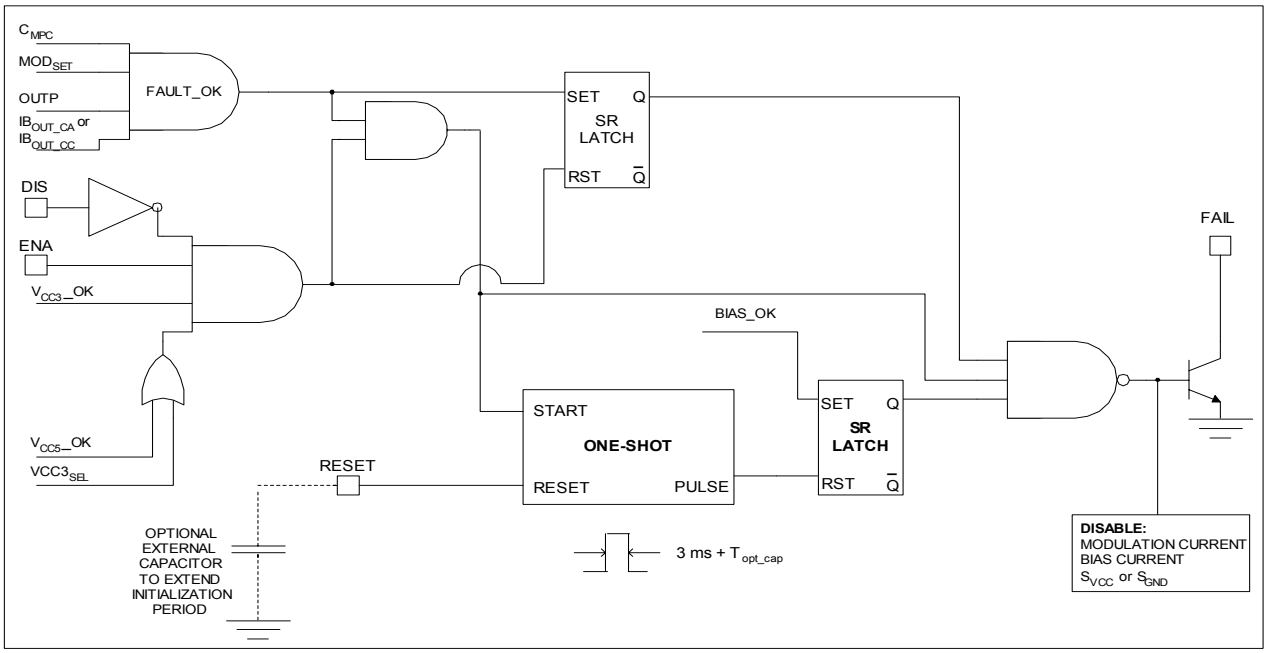
To facilitate complying with laser safety and DDMI[1] requirements, output monitors are provided for transmit power ($TxPwr_{MON}$), bias ($BIAS_{MON}$), and modulation current (MOD_{MON}).

These outputs will source current proportional to the emitted optical power ($TxPwr_{MON}$) the bias current ($BIAS_{MON}$) and modulation current (MOD_{MON}). These outputs may be connected directly to the corresponding pins on the M02080 module controller.

To use these pins without an M02080 they should be terminated with a resistor to ground that sets the desired full-scale voltage (not to exceed 2.5V).

If the outputs of these monitors are not needed, $TxPwr_{MON}$, $BIAS_{MON}$, and MOD_{MON} can all be left floating and the chip current consumption will be reduced by the value of the monitor currents.

Figure 1-4. Safety Circuit Block Diagram



1.4 Laser Eye Safety

Using this laser driver in the manner described herein does not ensure that the resulting laser transmitter complies with established standards such as IEC 825. Users must take the necessary precautions to ensure that eye safety and other applicable standards are met. Note that determining and implementing the level of fault tolerance required by the applications that this part is going into is the responsibility of the transmitter designer and manufacturer since the application of this device cannot be controlled by Mindspeed.

[1] Digital Diagnostic Monitoring Interface for Optical Tranceivers, defined in SFF-8472.

1.4.1 Safety Circuitry

Safety Circuitry in the M02069 will disable the modulation and bias current and assert the FAIL output immediately upon detecting a fault condition. In addition, the supply voltage that sources or sinks the laser current (SV_{CC} or SGND) will immediately go open circuit and prevent any current from passing through the laser.

Fault conditions checked by the M02069 include shorts to ground or V_{CC} of all pins which can increase the laser modulation or bias current.

For an initialization or power-up sequence to be successful, all the fault detection monitors must signal that the chip is “healthy”.

When DIS goes low, pins are checked for shorts to ground or V_{CC} and a FAIL condition is latched if there is a fault.

If the state of the pins is OK, a one-shot at the reset pin begins a countdown which will latch a FAIL condition if the bias current has not stabilized to an acceptable level during the one-shot time. The one-shot can be extended with an external capacitor connected from the RESET pin to ground.

The one-shot[1] width is approximately

$T_{ONE\text{-}SHOT}$ = 3 ms + (0.3 ms/pF)x(external capacitance).

1.5 Fault Conditions

This section describes the M02069 operating modes during fault conditions. Over voltage, under voltage, pins shorted to V_{CC} and pins shorted to ground are included in the fault Table 1-3.

Table 1-3. Circuit Response to Single-Point Fault Conditions

Pin Name	Circuit Response to Over-voltage Condition or Short to V_{CC}	Circuit Response to Under-Voltage Condition or Short to Ground
V_{CC}	Bias and modulation outputs are disabled once V_{CC} rises above the supply detection (high voltage) threshold (see Table 2-3)	Bias and modulation outputs are disabled once V_{CC} drops below the supply detection (low voltage) threshold
DIN+, DIN-	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.(1,2,3)	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.(1,2,3)
$VCC3_{SEL}$	Does not affect laser power.	Does not affect laser power.
DIS	Bias and modulation outputs are disabled. SV_{CC} is opened when CC_{SEL} is low or floating (or SGND is opened when CC_{SEL} is high)	Does not affect laser power (normal condition for circuit operation).
FAIL	Does not affect laser power.	Does not affect laser power.
RESET	Does not affect laser power.	Does not affect laser power.
MOD_{MON}	Does not affect laser power.	Does not affect laser power.
$BIAS_{MON}$	Does not affect laser power.	Does not affect laser power.
$TxPWR_{MON}$	Does not affect laser power.	Does not affect laser power.
APC_{SET}	A fault state occurs.(1)	A fault state occurs.(1)
I_{PIN}	A fault state occurs.(1)	A fault state occurs.(1)
$IBOUT_{CA}$(3)	The laser will be turned off, then a fault state occurs.(1)	A fault state occurs.(1)

1.The one-shot is actually comprised of an oscillator and 10-bit counter.

Table 1-3. Circuit Response to Single-Point Fault Conditions

Pin Name	Circuit Response to Over-voltage Condition or Short to V_{CC}	Circuit Response to Under-Voltage Condition or Short to Ground
$IBOUT_{CC}$[4]	A fault state occurs.[1]	The laser will be turned off, then a fault state occurs.[1]
OUT+[3]	Laser modulation is prevented; the APC loop will increase the bias current to compensate for the drop in laser power if it is DC coupled. If the set output power can not be obtained, a fault state occurs.[1,2]	A fault state occurs.[1]
OUT-[4]	Does not affect laser power during common cathode operation because output is AC coupled.	Does not affect laser power during common cathode operation because output is AC coupled.
SV_{CC}[3]	Does not affect laser power.	Laser bias current will be shut off and a fault state occurs.[1]
C_{APC}	Laser bias current will be shut off, then a fault state occurs.[1]	A fault state occurs.[1]
V_{CC3}	Bias and modulation outputs are disabled once V_{CC3} rises above the supply detection (high voltage) threshold	Bias and modulation outputs are disabled once V_{CC3} drops below the supply detection (low voltage) threshold
$PEAK_{ADJ}$	Does not affect laser power.	Does not affect laser power
CC_{SEL}	Normal operation for common cathode configuration. If the M02069 is configured for common anode drive, a fault state will occur.[1]	Normal operation for common anode configuration. If the M02069 is configured for common cathode drive, a fault state will occur.[1]
MOD_{SET}	When the laser is DC coupled in common anode configuration, the APC loop will attempt to compensate for the drop in output power. If the APC loop can not maintain the set average power, a fault state occurs.[1,2]	A fault state occurs.[1]
TC_{SLOPE}	Does not affect laser power.	When the laser is DC coupled in common anode configuration, the APC loop will attempt to compensate for any change in output power. If the APC loop can not maintain the set average power, a fault state occurs.[1,2]
DISDLY	Does not affect laser power.	Does not affect laser power.

Notes:
1. A fault state will assert the FAIL output, disable bias and modulation outputs and will either open the switch at SV_{CC} (CC_{SEL}=high) or S_{GND} (CC_{SEL}=low).
2. Does not affect laser power when the output is AC coupled to the laser.
3. Does not affect laser power during common cathode operation.
4. Does not affect laser power during common anode operation.

1.6 Applications

- EPON FTTH modules
- Gigabit Ethernet modules
- 1G/2G/4G Fibre Channel modules

Figure 1-5. Application Diagram, Common Anode VCSEL

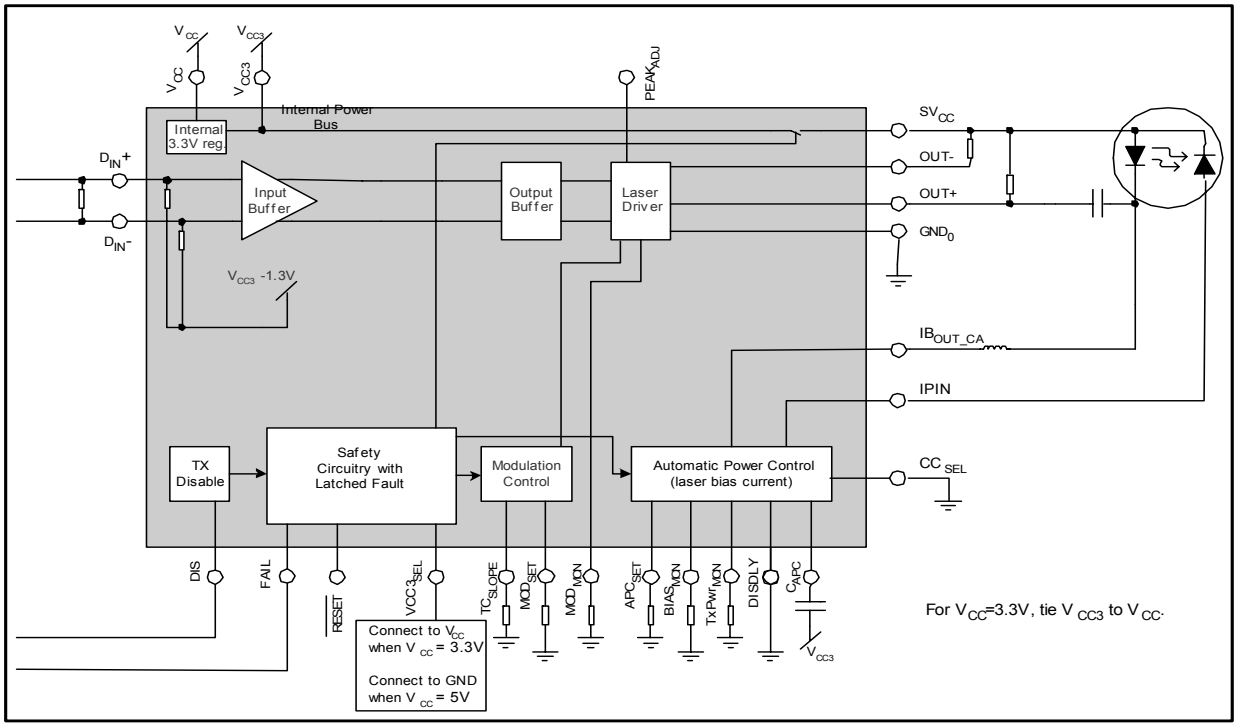


Figure 1-6. Application Diagram, Common Cathode VCSEL

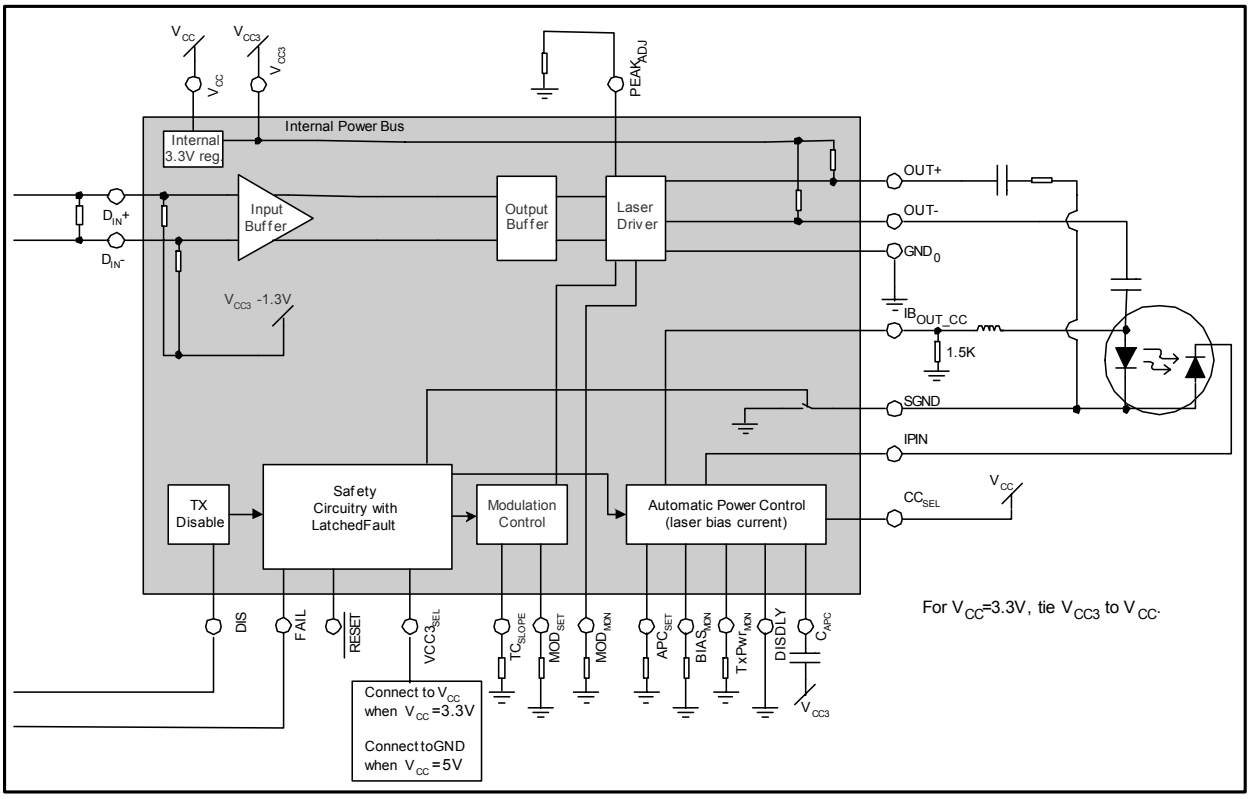


Figure 1-7. Application Diagram, Common Cathode VCSEL w/o Monitor Diode

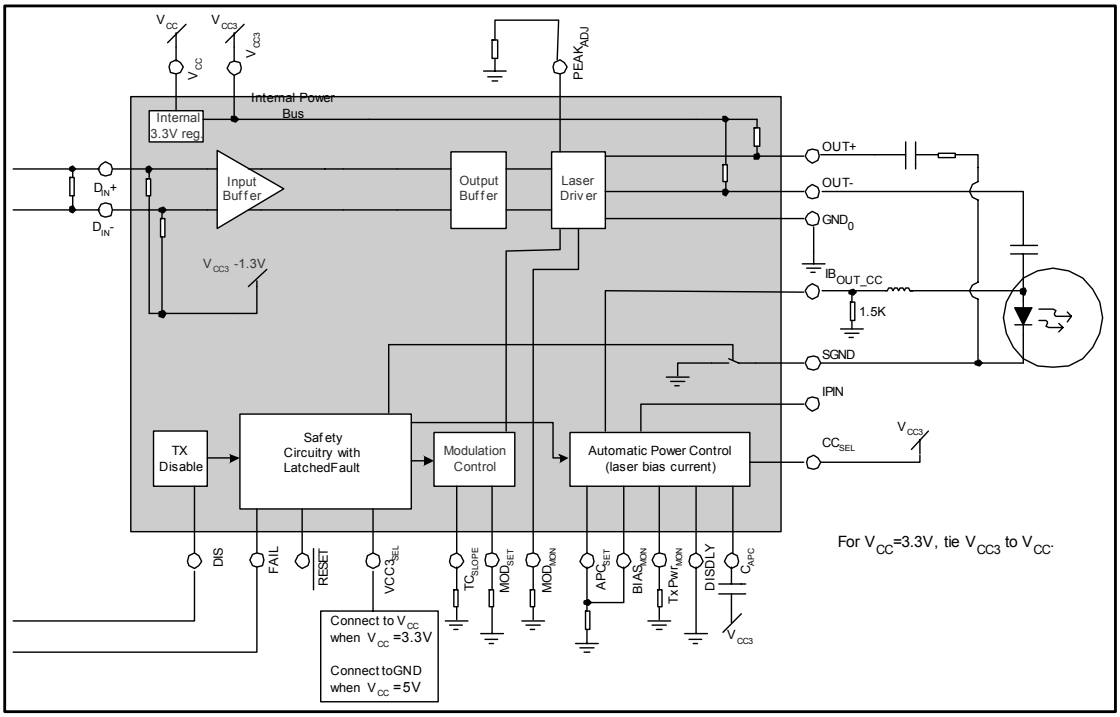
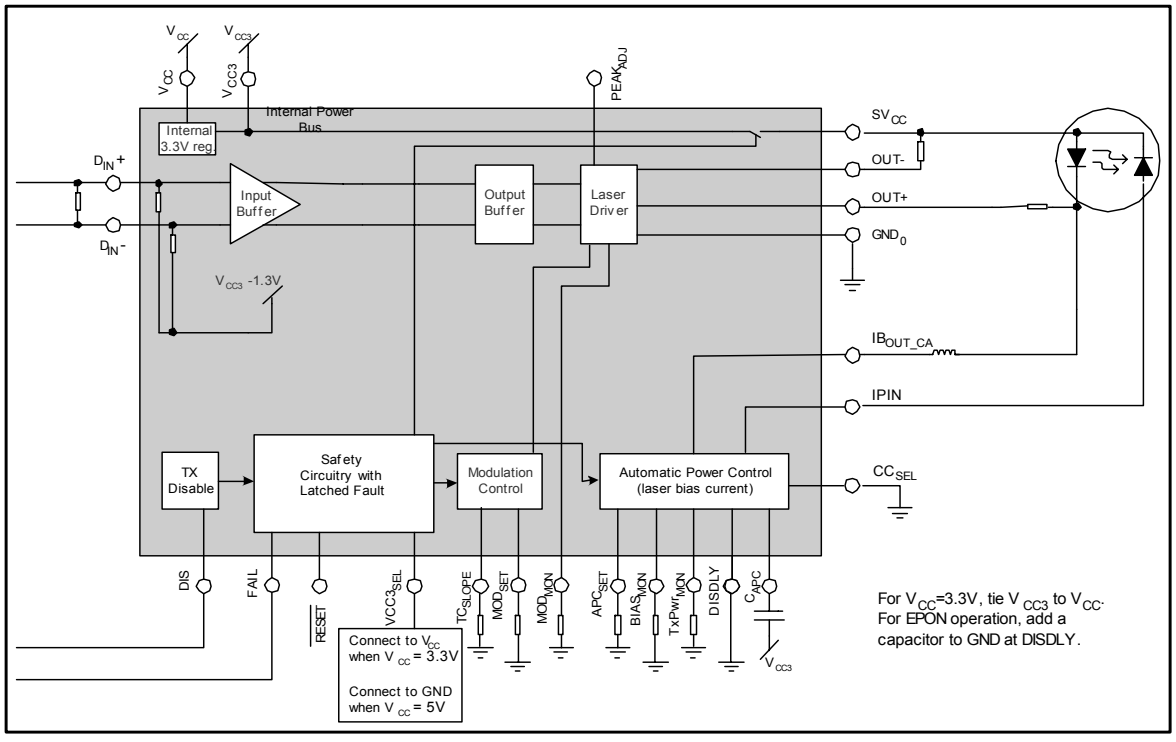


Figure 1-8. Application Diagram, Common Anode FP Laser, DC Coupling



1.7 Pin Definitions

Table 1-4. Pin Definitions

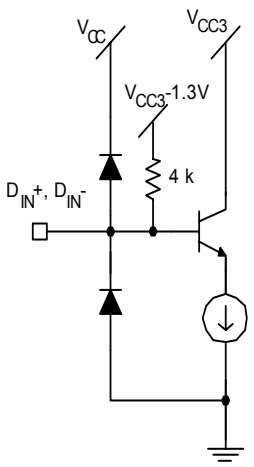
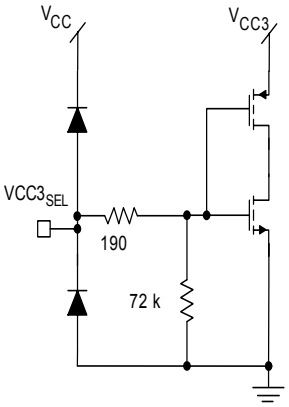
Pin Number	Pin Name	Pin equivalent load	Function
1	V_{CC}		Power supply, 5V or 3.3V.
2	$D_{IN}+$		Positive data input. Self biased. Compatible with AC coupled PECL, AC coupled CML, and DC-coupled PECL (when V_{CC} = 3.3V). When $D_{IN}+$ is high, OUT+ will sink current.
3	$D_{IN}-$	See $D_{IN}+$ drawing	Negative data input. Self biased Compatible with AC coupled PECL, AC coupled CML, and DC-coupled PECL (when V_{CC} = 3.3V).
4	$VCC3_{SEL}$		3.3V V_{CC} Select. Connect to V_{CC} for V_{CC} = 3.3V operation. Connect to GND for V_{CC} = 5V operation.

Table 1-4. Pin Definitions

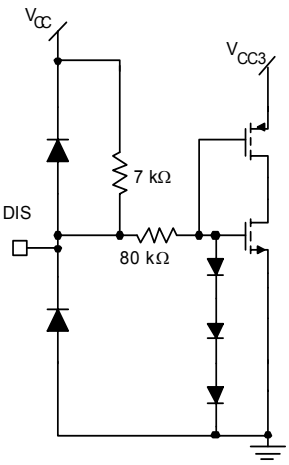
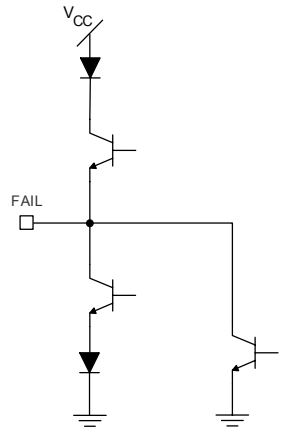
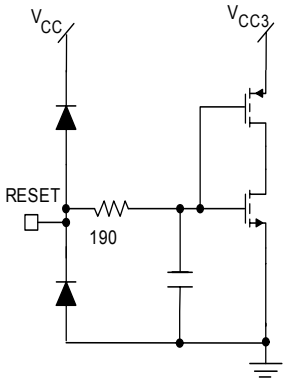
Pin Number	Pin Name	Pin equivalent load	Function
5	DIS		Bias and modulation output disable (TTL/CMOS). When high or left floating, the bias and modulation outputs are disabled. Set low for normal operation.
6	FAIL		Safety circuit fault output (TTL/CMOS). Goes high when a safety logic fault is detected. This output will also be high when DIS is high. Requires an external pull-up.
7	RESET		Safety circuit reset. Leave open for normal operation or add a capacitor to ground to extend the reset time. Connect to GND to disable window comparators at APC_{SET}

Table 1-4. Pin Definitions

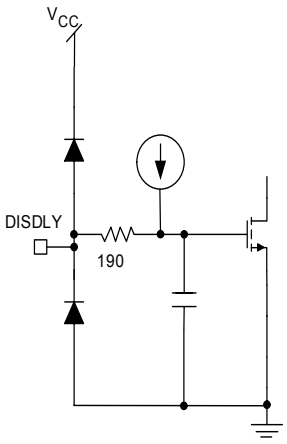
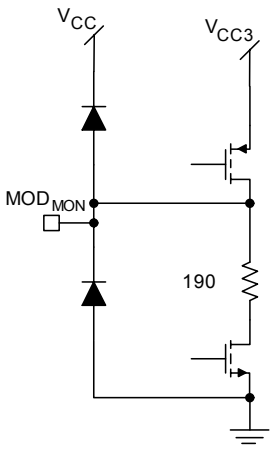
Pin Number	Pin Name	Pin equivalent load	Function
8	**DISDLY**		Disable delay control. Connect to ground for normal operation. In burst mode operation add a capacitor from this pin to ground to set the maximum disable time. Disable times greater than this maximum will engage the “slow-start” circuitry.
9	**MOD_{MON}**		Modulation Current Monitor. Connect to the corresponding pin on the M02080 or through a resistor to GND. The current through this pin is typically 1/50th of the MODULATION current to the laser when CC_{SEL} is low or 1/25th the MODULATION current when CC_{SEL} is high. This pin may be left open if the feature is not needed and the M02069 current consumption will be reduced by 0.5mA typically.
10	**$BIAS_{MON}$**	**See MOD_{MON} drawing**	Bias Current Monitor. Connect to the corresponding pin on the M02080 or through a resistor to GND. The current through this pin is typically: 1/50th of the BIAS current to the laser when CC_{SEL} is low 1/15th of the BIAS current to the laser when CC_{SEL} is high This pin may be left open if the feature is not needed and the M02069 current consumption will be reduced by 0.5mA typically.

Table 1-4. Pin Definitions

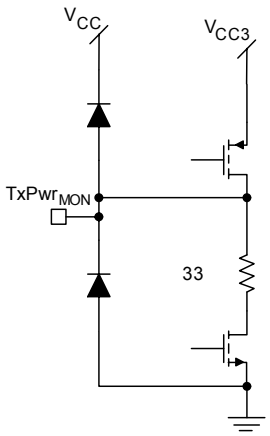
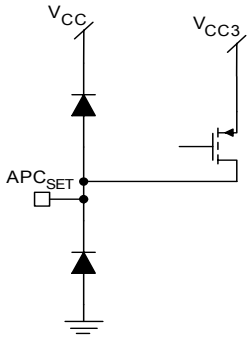
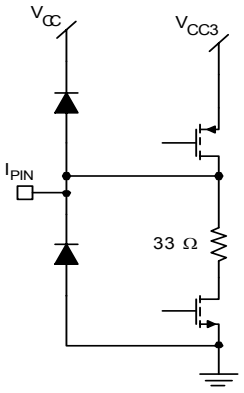
Pin Number	Pin Name	Pin equivalent load	Function
11	**$TxPwr_{MON}$**		Transmit Power Monitor. Connect to the corresponding pin on the M02080 or through a resistor to GND. The current through this pin is approximately the same as the photodiode current into I_{PIN}. The current out of this pin is low pass filtered (no external filtering required). This pin may be left open if the feature is not needed and the M02069 current consumption will be reduced by the I_{PIN} current.
12	**APC_{SET}**		Average Power Control, laser bias current adjustment. Connect to the corresponding pin on the M02080 or to a resistor between this pin and ground to set the bias current to the laser. The APC loop will adjust the laser bias current to maintain a voltage at APC_{SET} of approximately 1.3V. The current sourced from this pin is approximately the same as the current into I_{PIN}.
13	**I_{PIN}**		For CC_{SEL} low - Current input from monitor photodiode anode. The APC loop will adjust the laser bias current to maintain a voltage at APC_{SET} of approximately 1.3V and at this pin of approximately one V_{GS}. For CC_{SEL} high - Current source for monitor photodiode cathode. The APC loop will adjust the laser bias current to maintain a voltage at APC_{SET} of approximately 1.3V and at this pin of approximately one V_{GS} below V_{CC3}.

Table 1-4. Pin Definitions

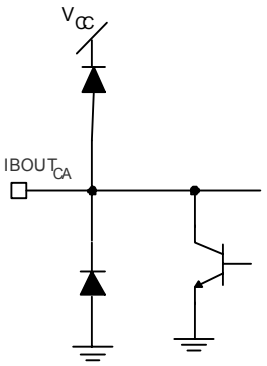
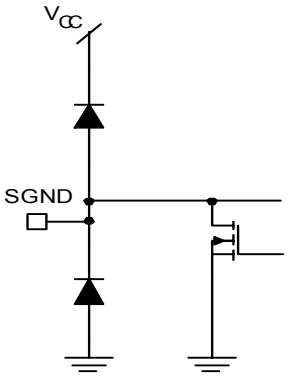
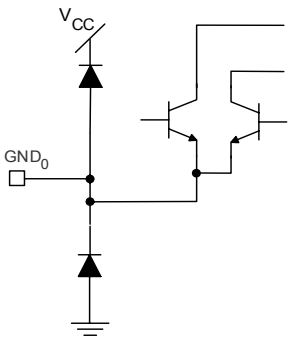
Pin Number	Pin Name	Pin equivalent load	Function
14	**IBOUT$_{CA}$ (CC$_{SEL}$ = low)**		Laser bias current output for common anode lasers (CC$_{SEL}$ must be low). Connect directly to laser cathode or at higher bit rates through a ferrite or a resistor to isolate the capacitance of this pin from the modulation drive, (~ 6pF). Maintain a voltage at least 0.7V above GND at this pin
	SGND (CC$_{SEL}$ = high)		Switched ground connection for common cathode lasers (CC$_{SEL}$ must be high). Provides redundant shutdown during a disable or fault condition. This switch is disabled during common anode operation.
15	**GND$_0$**		Ground for output stage. May be connected directly to circuit board ground. At high bit rates (>2Gb/s) an optional inductor or ferrite may be added to reduce switching transients.

Table 1-4. Pin Definitions

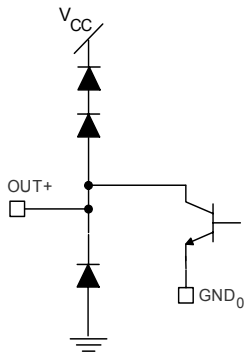
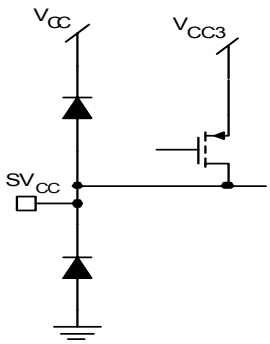
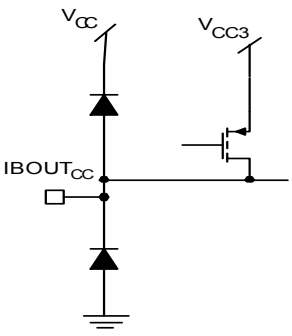
Pin Number	Pin Name	Pin equivalent load	Function
16	OUT+		Positive modulation current output (AC or DC coupled to cathode of laser in common anode designs). Sinks current when D_{IN}+ is HIGH. Maintain a voltage ≥ 0.7V at this pin.
17	OUT-	See OUT+ drawing	Negative modulation current output (AC coupled to anode of laser in common cathode designs). Sinks current when D_{IN}- is HIGH Maintain a voltage ≥ 0.7V at this pin.
18	SV_{CC} (CC_{SEL} = low)		Switched VCC. Supplies laser current for common anode designs. (CC_{SEL} must be LOW). Provides redundant shutdown during a disable or fault condition. This switch is disabled during common cathode operation.
	$IBOUT_{CC}$ (CC_{SEL} = high)		Laser bias current output for common cathode laser designs (CC_{SEL} must be high). Connect directly to laser anode or at higher bit rates through a ferrite or a resistor to isolate the capacitance of this pin from the modulation drive. Maintain a voltage of < 2.5V at this pin. In common cathode applications, also add 1.5k ohm to ground at this pin for correct safety logic power-up timing.

Table 1-4. Pin Definitions

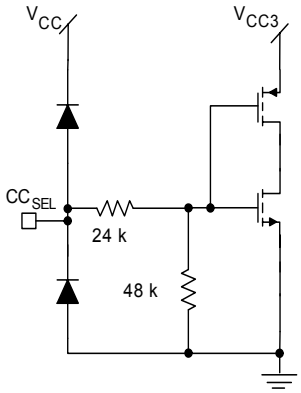
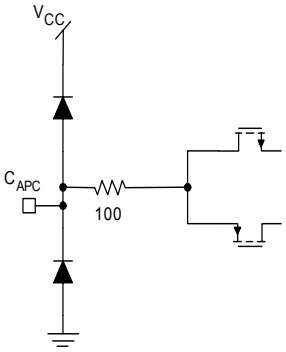
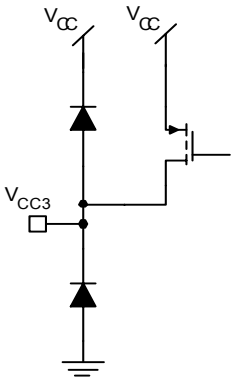
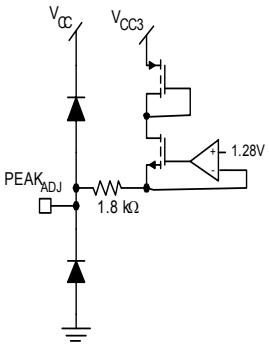
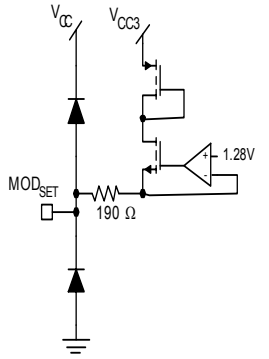
Pin Number	Pin Name	Pin equivalent load	Function
19	**CCSEL**		Laser select input. When high, common cathode operation is selected; $IBOUT_{CC}$ and SGND are functional and internal 50Ω output terminations are switched in at the modulation outputs OUT+ and OUT-. When low or floating, common anode operation is selected; $IBOUT_{CA}$ and SV_{CC} are functional and the 50Ω internal termination resistors at OUT+ and OUT- are disconnected.
20	**C_{APC}**		Automatic power control loop dominant pole capacitor. (Connect a capacitor between this pin and V_{CC3}.) A nominal capacitance of 2.2nF will give a bias current enable time of less than 1 ms.
21	**V_{CC3}**		3.3V applications - Power supply input. Connect to V_{CC}. 5V applications - Do not connect to 5V. Internally generated 3.3V power supply output. Do not attach to non-M02069 circuitry.

Table 1-4. Pin Definitions

Pin Number	Pin Name	Pin equivalent load	Function
22	$PEAK_{ADJ}$		Peaking adjustment input. A resistor (2kΩ to 20kΩ) between this pin and ground sets the amount of peaking current on OUT- to improve the fall time of the laser output. The peaking current is approximately (5 * (1.3V / 2 kΩ + resistance to ground)). Connect to V_{CC3} to disable peaking control.
23	MOD_{SET}		Modulation current control. Connect a resistor to ground to set the modulation current.
24	TC_{SLOPE}	See MOD_{SET} drawing	Modulation current temperature compensation slope adjustment. Connect a resistor to ground to set the temperature coefficient. Leave open to minimize the temperature compensation coefficient.
CENTER PAD	GND		Ground. Must be connected to ground for proper operation. This is the only package ground connection.

2.0 Product Specification

2.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	-0.4 to +6.0	V
V_{CC3}	3.3V power supply voltage	-0.4 to +4.0	V
T_A	Operating ambient temperature	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C
$I_{BIASOUTCA\ (MAX)}$	Maximum bias output current for common anode laser	75	mA
$I_{BIASOUTCC\ (MAX)}$	Maximum bias output current for common cathode laser	30	mA
$I_{MODCA\ (MAX)}$	Maximum modulation current for common anode laser	70	mA
$I_{MODCC\ (MAX)}$	Maximum modulation current for common cathode laser	30	mA
D_{IN}+/-	Data inputs	-0.4 to V_{CC3} + 0.4	V
DIS	Disable input	-0.4 to V_{CC} + 0.4	V
$BIAS_{MON}$, MOD_{MON}	Bias and modulation output current mirror compliance voltage	-0.4 to V_{CC3} + 0.4	V
I_{PIN}	Photodiode anode voltage	-0.4 to V_{CC3} + 0.4	V
I_{PIN}	Sink or Source current	2.0	A
FAIL	Status flag	-0.4 to V_{CC} + 0.4	V
APC_{SET}, MOD_{SET}	Set inputs	-0.4 to V_{CC3} + 0.4	V
TC_{SLOPE}	Temperature compensation slope	-0.4 to V_{CC3} + 0.4	V
OUT+, OUT-	Output	-0.4 to V_{CC} + 0.4	V

2.2 Recommended Operating Conditions

Table 2-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply (V_{CC}-GND)	3.3 ± 7.5% or 5.0 + 10%,-5%	V
Operating ambient	-40 to + 85	°C

2.3 DC Characteristics

(V_{CC} = +3.05V to +3.55V or 4.75V to 5.5V, T_A = -40 °C to +85 °C, unless otherwise noted)
Typical values for common anode are at V_{CC} = 3.3 V, $IBOUT_{CA}$ = 20 mA, I_{MOD} = 20 mA, T_A = 25 °C, unless otherwise noted.
Typical values for common cathode are at V_{CC} = 3.3 V, $IBOUT_{CC}$ = 5 mA, I_{MOD} = 5 mA, T_A = 25 °C, unless otherwise noted

Table 2-3. DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply current excluding I_{MOD} and I_{BIAS}	$PEAK_{ADJ}$ high (no peaking adjust)	–			mA
		Common anode operation(1)	–	28	48	
		Common cathode operation(1)	–	35	55	
		Additional current when $PEAK_{ADJ}$ is used.	–	–	7	
		Additional current when operating from a 5V supply(2)		4	TBD	
$IBOUT_{CA}$	Bias current adjust range, common anode mode	$V(I_{BIASOUT})$ > 0.7V	1		50	mA
$IBOUT_{CC}$	Bias current adjust range, common cathode mode	$V(I_{BIASOUT})$ < 2.5V	0.5		15	mA
IB_{OFF}	Bias current with optical output disabled	DIS = high $V(IBOUT_{CA}) = V_{CC3}$ for common anode operation. $V(IBOUT_{CC})$ = 0V for common cathode operation.	–	–	150	µA
	Ratio of I_{BIAS} current to $BIAS_{MON}$ current	CC_{SEL} low, common anode mode CC_{SEL} high, common cathode mode	–	50 15	–	A/A
V_{MD}	Monitor diode reverse bias voltage	V_{CC} =3.3V	1.7	–	–	V
I_{MD}	Monitor diode current adjustment range	Adjusted with R_{APCSET}	10	–	1500	µA
	Ratio of $TxPwr_{MON}$ current to monitor photodiode current			1		A/A

Table 2-3. DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{MD_MAX}	Maximum monitor photodiode capacitance for APC loop stability. Includes all associated parasitic capacitances.				100	pF
	TTL/CMOS input high voltage (DIS)		2.0	–	5.5	V
	TTL/CMOS input low voltage (DIS)		–	–	0.8	V
	CMOS input high voltage ($VCC3_{SEL}$)		2.4			V
	CMOS input low voltage ($VCC3_{SEL}$)				1.2	V
	Logic output high voltage (FAIL)	With external 10kΩ pull-up to V_{CC}.	V_{CC} - 0.6	–	–	V
	Logic output low voltage (FAIL)	sink current = 1.5mA	–	–	0.4	V
R_{IN}	Differential input impedance	Data inputs	--	8000	–	W
V_{SELF}	Self-biased common-mode input voltage		--	V_{CC3} - 1.3	--	V
V_{INCM}	Common-mode input compliance voltage	Data inputs	t.b.d.	–	V_{CC3}-[$V_{IN(Diff)}$]/4	V
$V_{IN(DIFF)}$	Differential input voltage	= 2 x ($D_{IN+HIGH}$ - D_{IN+LOW})	200	–	2400	mVpp
V_{CC3THL}(3)	3.3V supply detection, lower threshold		2.6	2.8	2.9	V
V_{CC3THH}(3)	3.3V supply detection, upper threshold		3.65	3.8	4.0	V
V_{CC5THL}	5V supply detection, lower threshold		4.3	4.5	4.65	V
V_{CC5THH}	5V supply detection, upper threshold		5.6	5.8	6.0	V
V_{REF1}	Reference voltage for MOD_{SET}		1.1	1.3	1.4	V
V_{APCSET}	Reference voltage for APC_{SET}			1.3		V
V_{BL}	Bias_OK lower voltage threshold			1.0		V

Table 2-3. DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{BH}	Bias_OK upper voltage threshold			1.6		V
V_{FAULTL}(4)	Lower voltage threshold for fault inputs $IBOUT_{CA}$, OUT+, C_{APC}, and MOD_{SET}	FAIL asserts if any of these signals fall below this value.		300	375	mV
V_{FAULTH}(5)	Upper voltage threshold for fault inputs $IBOUT_{CC}$	FAIL asserts if any of these signals fall above this value.	2.6	2.7		V
V_{SELFL}	Self bias voltage for $IBOUT_{CA}$ and OUT+	During disable state	0.5	1.6	1.8	V
V_{SELFH}	Self bias voltage for $IBOUT_{CC}$	During disable state		1.6	2.2	V

Notes:
1. Excludes bias and modulation currents.
2. Bias and modulation currents add directly to power supply current in 5V applications. The additional supply current noted excludes these currents.
3. V_{CC3} "supply OK" circuitry monitors the internally regulated 3.3V supply when V_{CC} = 5V ($VCC3_{SEL}$ =low). When V_{CC} = 3.3V, V_{CC3} "supply OK" circuitry monitors V_{CC} ($VCC3_{SEL}$ =high).
4. A low level at $IBOUT_{CA}$ does not trigger a fault condition during common cathode operation.
5. A low level at $IBOUT_{CC}$ does not trigger a fault condition during common anode operation.

2.4 AC Characteristics

(V_{CC} = 3.05 V to 3.55V or 4.7V to 5.5V, TA = -40 °C to +85 °C, unless otherwise noted)
Typical values for common anode are at V_{CC} = 3.3 V, IBOUTCA = 20 mA, IMOD = 20 mA, TA = 25 °C, unless otherwise noted.
Typical values for common cathode are at V_{CC} = 3.3 V, IBOUTCC = 5 mA, IMOD = 5 mA, TA = 25 °C, unless otherwise noted.

Table 2-4. AC Characteristics – Logic Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
I_{MOD}	Modulation current adjust range	Common Cathode Mode OUT+ and OUT- AC coupled into 50Ω load. Common Anode Mode OUT+ and OUT- DC coupled into 25Ω load.(1)	1 3	–	15 45	mA
$I_{MOD(OFF)}$(2)	Modulation current with output disabled	DIS = high	–	–	150	µA
	Ratio of modulation current to MOD_{MON} current	CC_{SEL} = high, RLOAD = 50Ω CC_{SEL} = low	–	30 65	–	A/A
I_{MOD-TC}	Programmable range for modulation current temperature coefficient	Adjustable using TC_{SLOPE}	0	–	10^4	ppm/°C
$T_{TCSTART}$	Temperature at which modulation current TC compensation enables			20		°C

Table 2-4. AC Characteristics – Logic Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
tr	Modulation output rise time	20% to 80% into 25 Ω[3]. (I_{MOD} = 28 mA). Measured using 11110000 pattern at 2.5Gbps	–	TBD	80	ps
tf	Modulation output fall time		–	TBD	80	ps
OS_{OFF}	Overshoot of modulation output current in the "off" direction	into 25 Ω load	--	1	2	%
RJ	Random jitter		–	0.8	–	ps_{rms}
DJ	Deterministic jitter	Measured into 25Ω load, 2^{31} - 1 PRBS at 2.7 Gbps K28.5 pattern at 4.3 Gbps (includes pulse width distortion[4])		10 10	25 23	ps_{pp}

Notes:
1. Minimum voltage at OUT+ > 0.7V.
2. The current through the laser in this state can be made negligible by adding a 1kΩ or less resistor in parallel with the laser.
3. The M02069 is designed to drive 25Ω loads. External resistance should be added in series or parallel to the Laser to create this load impedance. In common cathode mode, 50Ω resistors internal to the M02069 are in parallel with the laser.
4. Pulse width distortion is measured single-ended.

2.5 Safety Logic Timing

(V_{CC} = 3.05 V to 3.55V or 4.7V to 5.5V, T_A = -40 °C to +85 °C, unless otherwise noted)
Typical values for common anode are at V_{CC} = 3.3 V, $IBOUT_{CA}$ = 20 mA, I_{MOD} = 20 mA, T_A = 25 °C, unless otherwise noted.
Typical values for common cathode are at V_{CC} = 3.3 V, $IBOUT_{CC}$ = 5 mA, I_{MOD} = 5 mA, T_A = 25 °C, unless otherwise noted.

Table 2-5. Safety Logic Timing

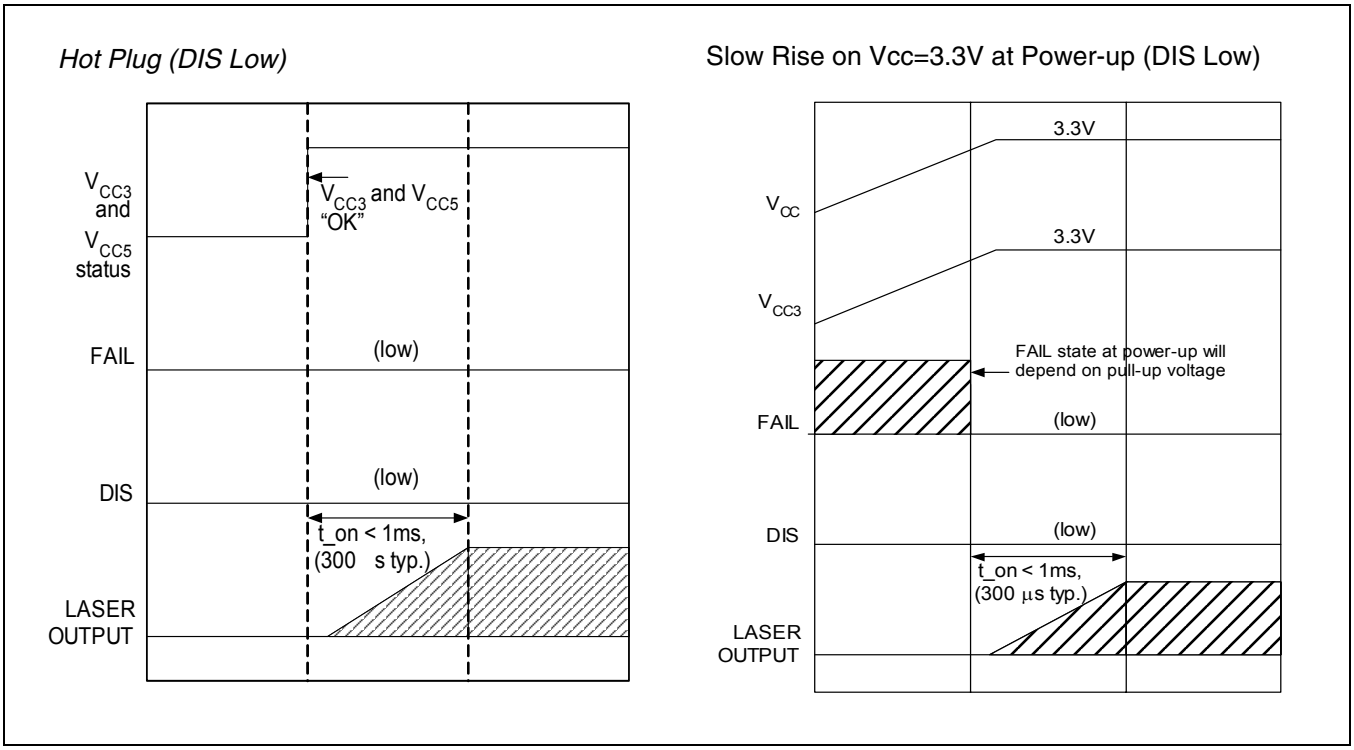
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
t_off	DIS assert time	Rising edge of DIS to fall of output signal below 10% of nominal[1]			10	µs
t_on	DIS negate time	Falling edge of DIS to rise of output signal above 90% of nominal[1]			1	ms
t_init	Time to initialize[2]	Includes reset of FAIL; from power on after Supply_OK or from negation of DIS during reset of FAIL condition	2	3	5	ms

Table 2-5. Safety Logic Timing

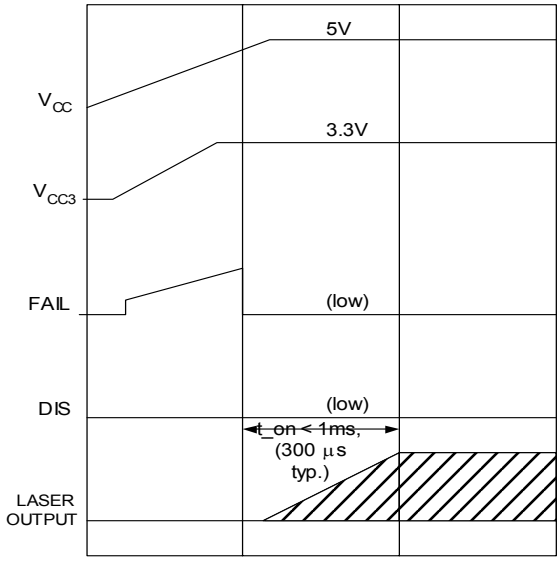
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
t_fault	Laser fault time - from fault condition to assertion of FAIL	From occurrence of fault condition or when Supply_OK is beyond specified range			100	µs
t_reset	DIS time to start reset	DIS or ENA pulse width required to initialize safety circuitry or reset a latched fault			10[3]	µs
t_{VCC_OK}	Supply_OK delay time	Delay between Supply_OK condition and when outputs are enabled	10	20		µs
t_on_{BM}	DIS negate (turn-on) time during burst-mode operation	Using integrated switch at SVCC (3.3V operation) [4]		300	500	ns
t_off_{BM}	DIS assert (turn-off) time during burst-mode operation	Using integrated switch at SVCC (3.3V operation)[4]		200	500	ns

Notes:
1. With CAPC = 2.2nF
2. User-adjustable. Specifications reflect timing with no external RESET capacitor.
3. With ≤ 1nF capacitor from RESET pin to ground.
4. Imod > 12mA

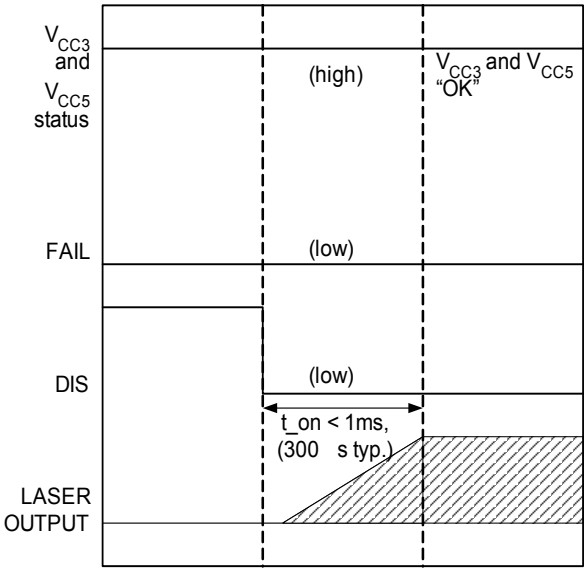
Figure 2-1. Safety Logic Timing Characteristics



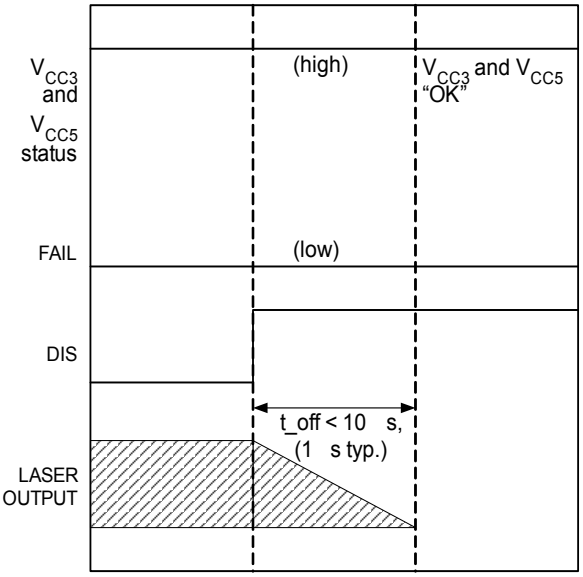
Slow Rise on Vcc=5V at Power-up (DIS Low)



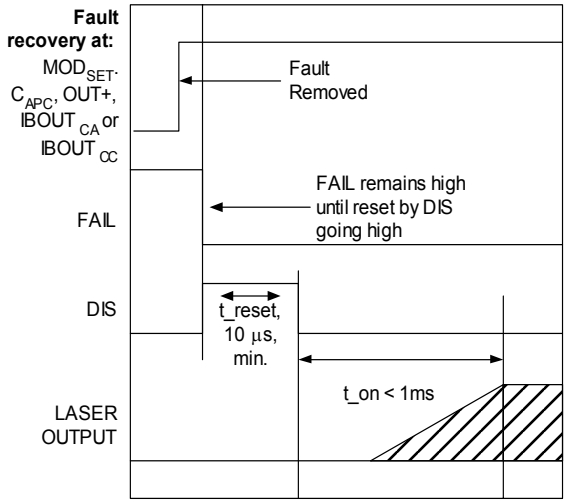
Transmitter Enable (DIS transition Low)



Transmitter Disable (DIS transition high)



Fault Recovery Behaviour



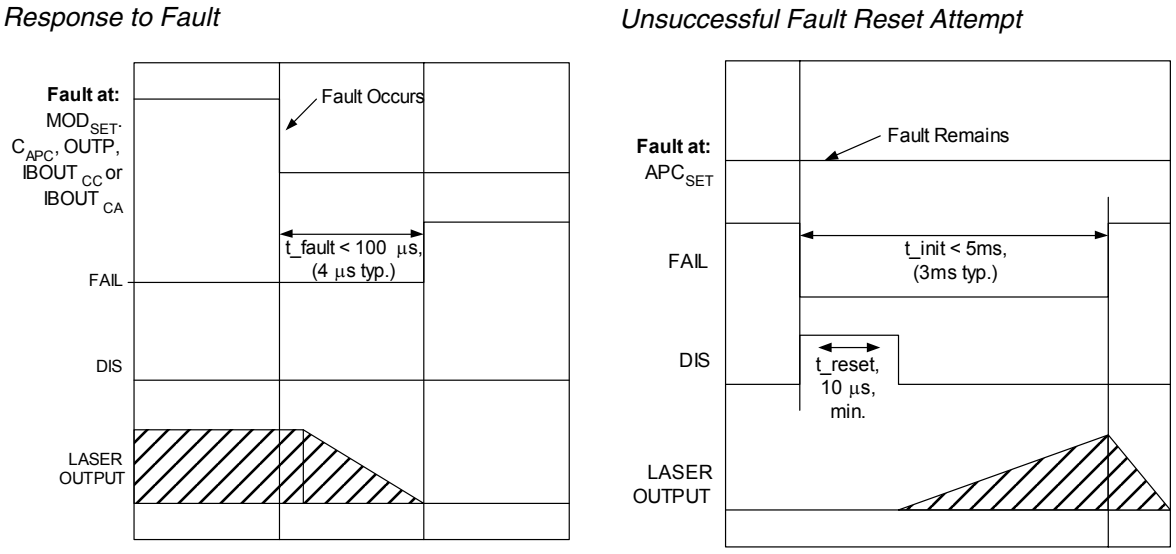
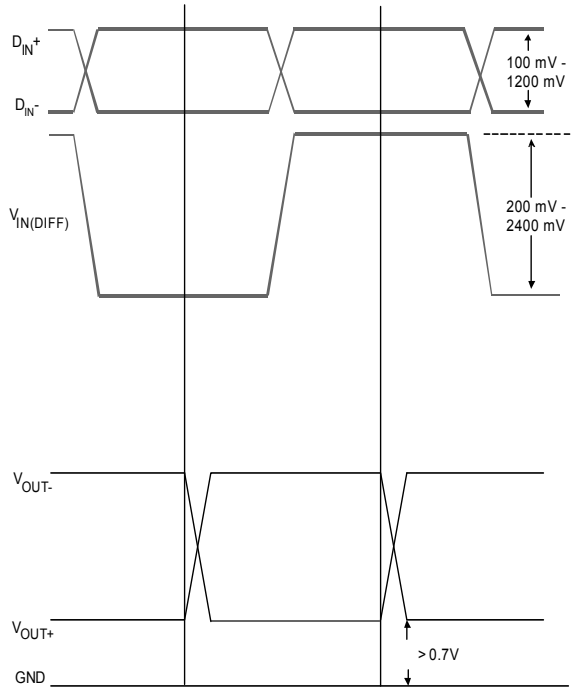


Figure 2-2. Relationship Between Data Inputs and Modulation Outputs

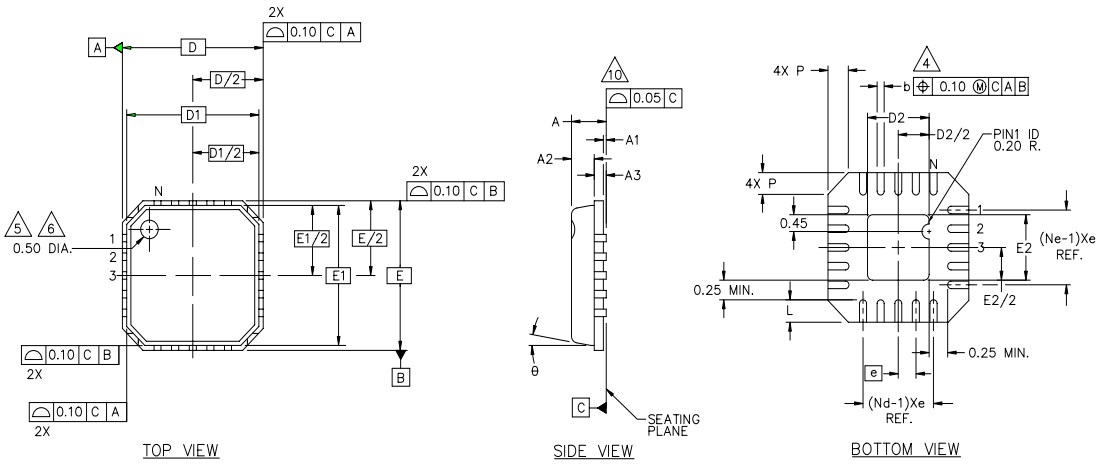


2.6 Package Specification

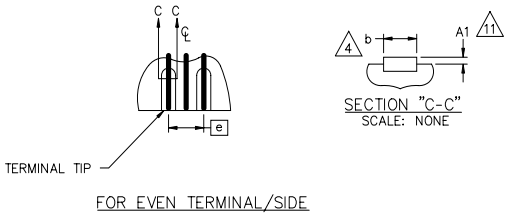
2.6.1 Mechanical Description

2.6.1.1 Package Details

Figure 2-3. QFN24 Package Information



Note: View is for a 20 pin package. All dimensions in the tables apply for the 24 pin package



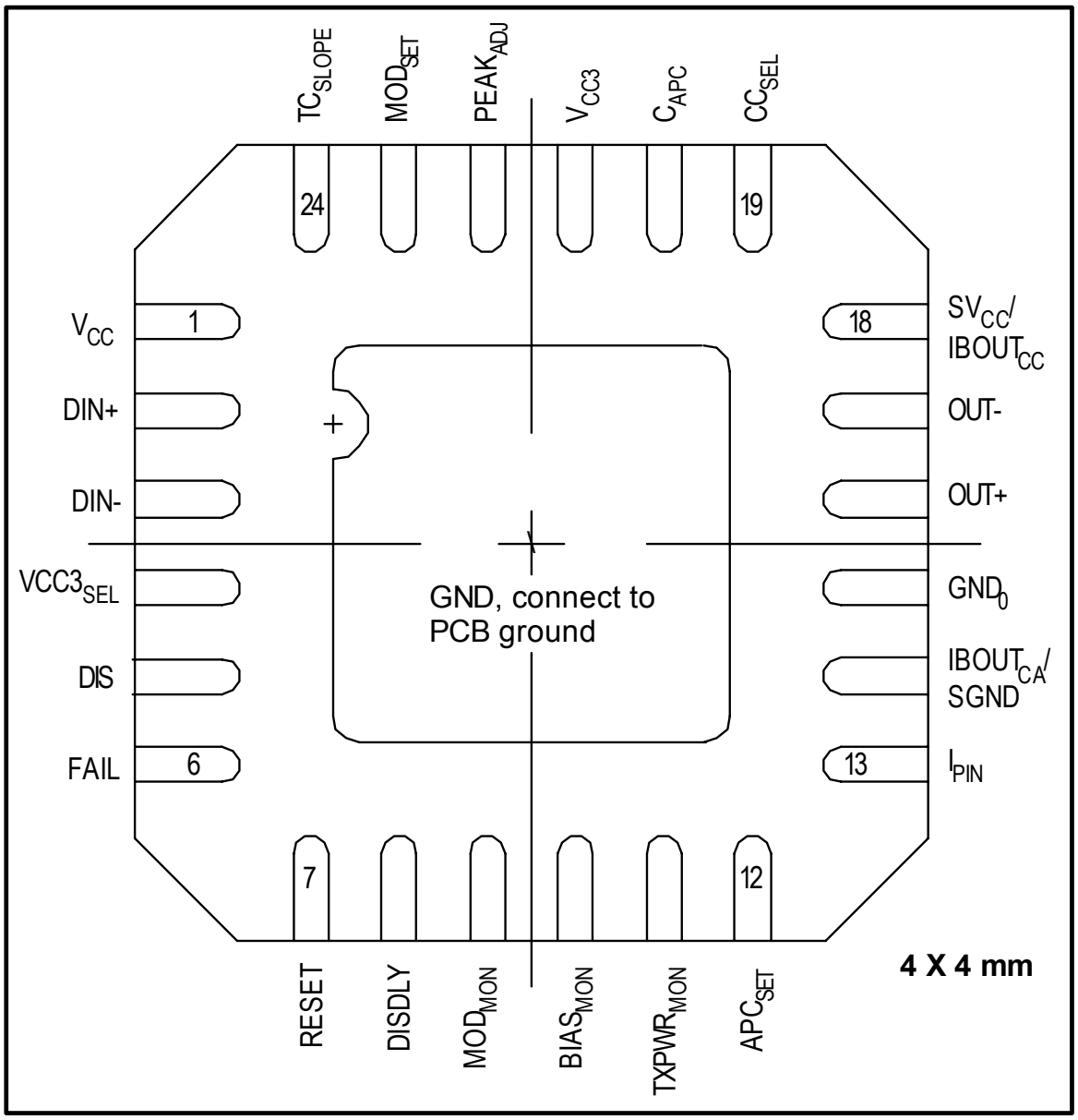
SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		24		3
Nd		6		3
Ne		6		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	2.19	2.34	2.49	
E2	2.19	2.34	2.49	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

Figure 2-4. Pin Assignments for M02069 Device



2.7 Thermal Characteristics

t/b/d

2.8 Manufactureability

2.8.1 Electrostatic Discharge

t/b/d

2.8.2 Peak Reflow Temperature

t/b/d

2.8.3 Moisture Sensitivity Level (MSL)

t/b/d

2.9 Design Considerations

t/b/d

2.9.1 Component Placement and Layout

t/b/d

2.9.2 Routing Considerations

t/b/d

2.9.3 Thermal Considerations

t/b/d

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