AMERICAN MICROSYSTEMS, INC.

WavePlex™ Wireless Products

SX048
High Data Rate
Spread Spectrum Receiver

January, 1997

PRODUCT DESCRIPTION

General Description

The SX048 Spread Spectrum Receiver is a highly programmable baseband CMOS integrated circuit that simplifies the design of direct sequence spread spectrum modems. Used to create very low cost receive-only remote wireless links, the SX048 is designed to serve as the collection host for a large group of SX047 transmitters or SX049 transceivers. Connected to a standard 8 bit microcontroller data bus, the SX048 allows the user to manage internal receive functions including the type and length of PN codes, data rates, chipping rates, slip rates, tracking rates, preamble, transmission protocols, and type of redundancy checks, as well as manage the external circuitry for signal reception.

Features

- Supports multiple SX047 transmitters or SX049 transceivers as system collector host link
- PN clock programmable up to 64M chips per second
- Up to 30dB processing gain; PN code lengths from 3 to 2047 chips
- Data and PN code streams available either separately or combined
- Supports BPSK, DBPSK, QPSK, DPQSK, and QAM modulation schemes
- Supports RF reception in any frequency band
- CRC-32 or CRC-16 decoding and error checking selectable
- Provides selectable code descrambling for spectral whitening
- Address/data bus timing allows interface to many popular 8 bit microcontrollers
- Supports packetized synchronous protocol (HDLC)
- 16 Byte receive data FIFOs reduces interrupt overhead
- Data rates from 100bps to 4Mbps (BPSK or 8Mbps (QPSK) or 12MBPS (QAM8) or 16Mbps (QAM16)
- Low power 5 volt operation
- Power down modes for minimum power usage

Figure 1: BLOCK DIAGRAM

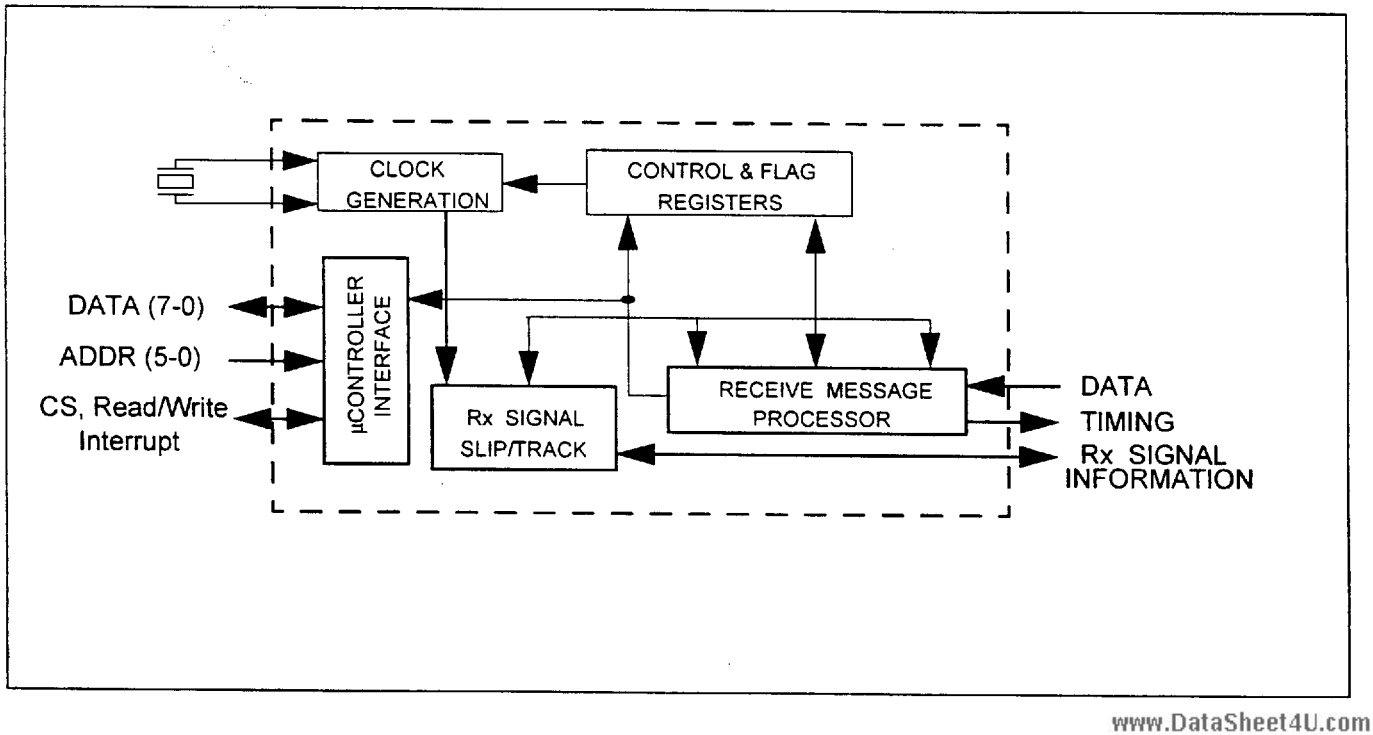

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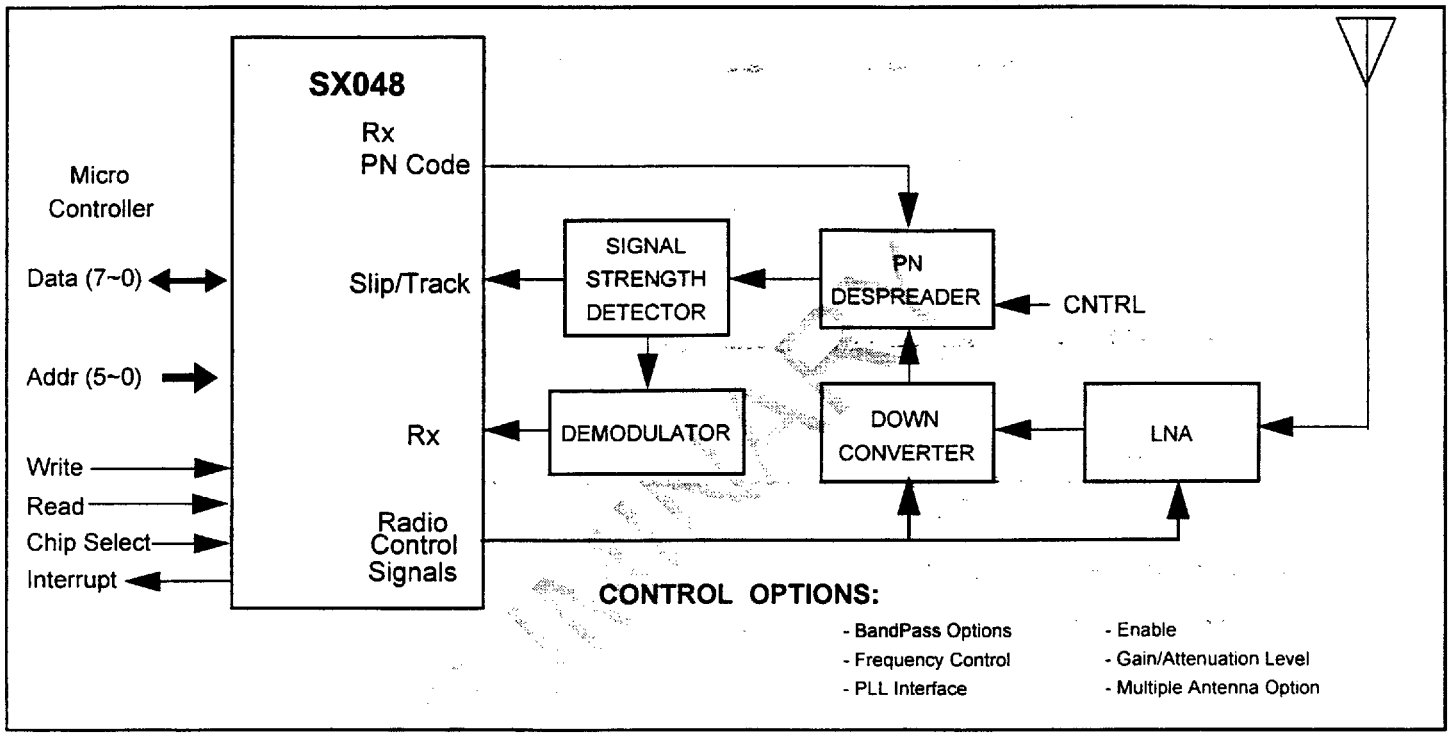
Figure 2. SYSTEM INTERFACE DIAGRAM



Functional Block Overview

The SX048 Block Diagram in Figure 1 details the major functional blocks of the device. The microcontroller manages the Message Processors through various control and flag registers on the IC.

The microcontroller can also use registers in the SX048 to control various radio functions. Figure 2 above represents the full radio implementation using the SX048.

MICROCONTROLLER INTERFACE: The device has a simple bus interface consisting of a bi-directional tri-state eight-bit data bus , a seven-bit address bus, read, write, and chip select inputs, and a general interrupt output. Target microcontrollers for this interface include the 68HC11, 68HC05, 6502, Z8, 8051, 16C5x, and 16C7x.

Power Manager: The user can select one of several power options to minimize power usage.

CONTROL AND FLAG REGISTERS: The SX048 has 33 registers available to the microcontroller. These registers allow programmable control over most characteristics of the receive channels (See Control Options in Figures 3), as well as off-chip control of the radio portion of the design. (See Control Options in Figure 2)

The SX048 includes a programmable 8 to 96 bit variable RF synthesizer interface. This interface supports any of the three popular serial data transfer styles in RF synthesizers: pulsed transfer, active enable transfer, or clock and data only. Or it can be set to a fourth 'user defined' mode. Extra control lines are also available for external circuits that require gain or attenuation level selection, pass band range selection, multiple antenna selection, etc..

In Packet Mode, the SX048 can receive a repeating preamble code, HDLC protocols, destination address and control commands, CRC-16 or CRC-32 error detection coding, and end codes as selected by the control registers. A packet mode frame format is shown below:

START FLAG	ADDRESS	CONTROL	INFORMATION	CRC	END FLAG
8 bits	8 bits	8 bits	8 * N bits (any length)	16 / 32 bits	8 bits

Rx SIGNAL SLIP / TRACK: The SX048 uses a 'shift and compare' approach to sync up with the receive signal. Using the 4MHz Tx_Clk for the Rx Phase Lock Loop (see Figure 4) during the capture or 'Slip' mode, the SX048 generates the expected PN code (mixed with Preamble) and sends it to the external PN Despreader circuit (see Figure 2). If the generated PN code is synchronized perfectly with the PN code in the receive signal, then the

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Signal Strength Detector will return a threshold energy level above a programmable threshold that indicates the match. Otherwise, the PN code will be delayed (shifted) by one half PN chip time period and the procedure is repeated. In this way the Rx PN code is slipped in time until it matches the EPOCH period of the received signal.

Once synchronization is achieved, the SX048 transfers to a Tracking mode that uses the Receive Signal Strength input to drive the PLL, and dithers the PN Code delay in small steps around the synchronized signal to maintain solid tracking.

An internal "Track_on" signal alerts the Receive channel that a readable data stream is being presented to the IC.

RECEIVE MESSAGE PROCESSOR: The Receive channel (Figure 3) processes the receive message and delivers bytes of data to the microcontroller.

Word Detect: The Word Detect circuit reconstructs a single data stream from the incoming data streams processed by the external demodulator. BPSK, QPSK, DBPSK, DQPSK, or QAM results from the demodulator are presented on the RxD0 and RxD1 pins.

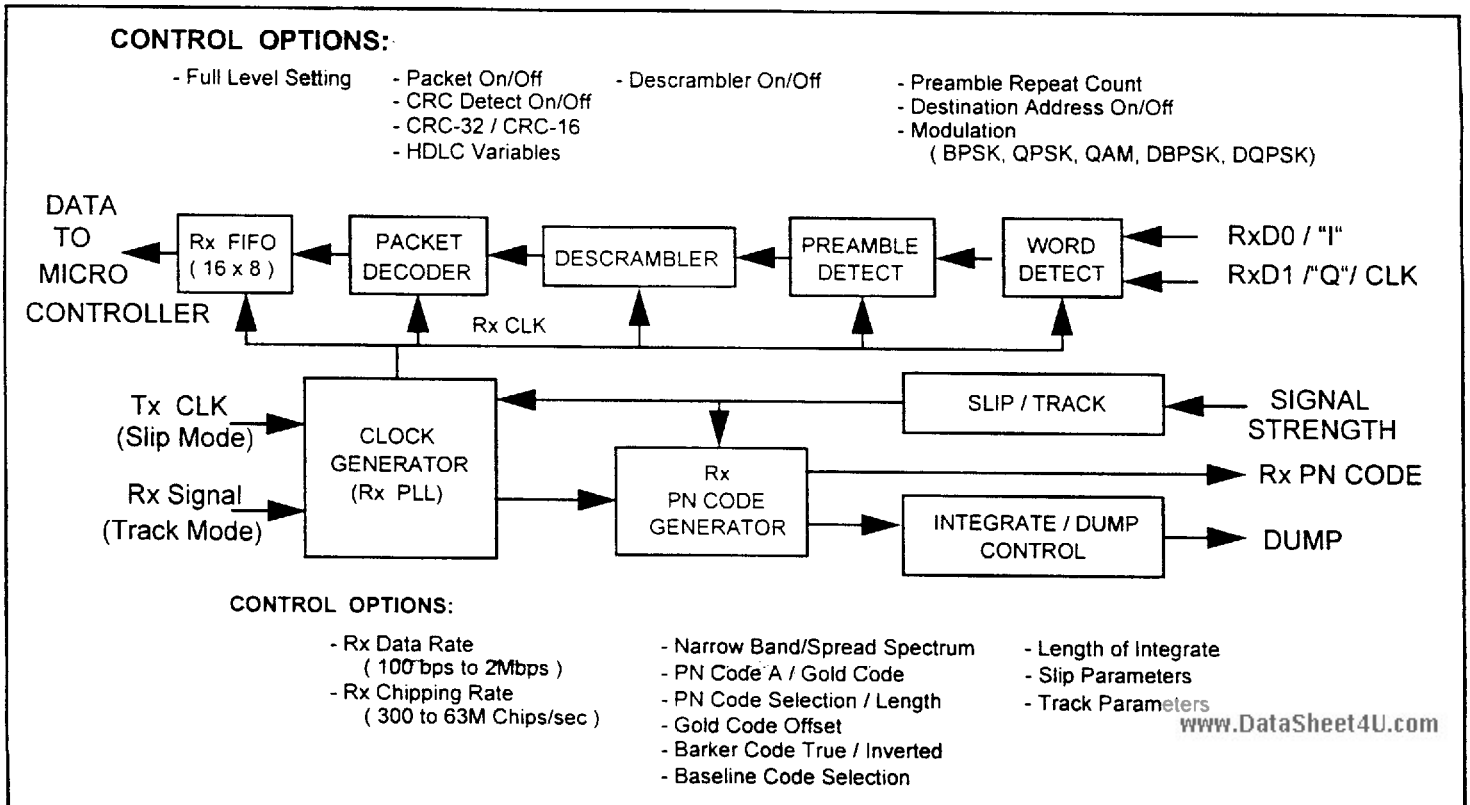
Preamble Detect: The Preamble Detect searches the incoming stream for the expected repeating preamble code followed by the end-of-preamble code. It then flags the Receive channel and microcontroller that a valid message is being received.

Descrambler: The Descrambler recovers the data that was scrambled in the Transmit channel. The descrambler can be programmed on or off.

Packet Decoder: The Packet Decoder verifies the destination address and then recaptures the raw data for the microcontroller. Programmed with the matched settings of preamble, protocol, and error detection of the Transmitter, the decoder alerts the controller of any receive errors, abort codes, lost tracking, and end-of-message information via interrupts and status registers.

Rx FIFO: Byte-wide data for the microcontroller is placed in a 16-byte deep Rx FIFO. The 'FIFO near-full' detect level can be programmed at bytes 0, 2, 4, or 8. The FIFO relays status to the microcontroller by means of the interrupt pin and control registers.

Figure 3. RECEIVE MESSAGE PROCESSOR



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The SX048 can achieve data rates dependent on the PN code lengths used. These are shown below for each modulation scheme (nominal).

BPSK and DBPSK:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15	4M	4M
31	2M	2M
63	1M	1M
127	500K	500K
255	250K	250K
511	125K	125K
1023	62K	62K
2047	31K	31K

QPSK, DQPSK, QAM **:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15	8M	4M
31	4M	2M
63	2M	1M
127	1M	500K
255	500K	250K
511	250K	125K
1023	125K	62K
2047	62K	31K

* The 11 bit Barker code (1, 0,1,1,0,1,1,1,0,0,0).

** QAM requires external ADCs and DACs. Data is transferred serially.

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Pin Description

NAME:	TYPE:	FUNCTION:
AGND1	Analog ground	
GND1	ground	
VDD1	Vdd	
OSC1	input	Crystal Oscillator or external reference input. This input is divided by OSCDIV to generate the reference clock for the transmit PLL.
OSC2	padosc	Xtal Osc output.
PLL[0:3]	output	Off-Chip PLL programming; bit0, Enable1; bit1, Sclk; bit2, Enable0; bit3, Sdata.
GND2	ground	
EXT[0:7]	output	External Control port (lower bits), User Defined Functions for radio control.
VDD2	Vdd	
INT	output	Active high. Initiates an interrupt to the microprocessor.
RESET	input	Active low. Sets all registers to default values and forces the SX048 into its standby state.
CS	input	Active low. Selects the chip for reading and writing via the uP interface
RD	input	Active low. Initiates a read operation via the uP interface.
WR	input	Active low. Initiates a write operation via the uP interface.
GND3	ground	
DATA[0:7]	BiDirection	uP Interface data bus.
ADDR[0:6]	input	uP Interface address bus.
VDD3	Vdd	
GND4	ground	
DUMP	output	Integrate & Dump Control logic output.
PN2	output	Receive PN Generator output.
RCVRY	BiDirection	Clock recovery input for Narrow Band Mode. Track-On (active high) output for Spread Spectrum Mode. Indicates to external circuitry that the SX048 is locked and tracking the received PN code.
RXD1	Analog I/O	Receive data input 'Q' or QAM mode output clock to external shift register.

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NAME:	TYPE:	FUNCTION:
RXD0	Analog In	Receive data input 'I'.
VREFD	Analog In	Reference voltage for integrate and dump comparators and switches.
AGND2	Analog ground	
VCO2	Analog Input	Receive VCO control voltage input
AVDD2	Analog VDD	
DACOUT1	Analog Output	Receive DAC output during TRACK operation. Note: DACOUT0 and DACOUT1 are provided in the event separate gain control is necessary for SLIP and TRACK operation.
DACOUT0	Analog Output	Receive PLL DAC output during SLIP operation.
RBIAS	Analog Input	Current reference for DACs and analog buffers. Nominal resistor value of 30K ohm for 5 volt VDD.
VREF	Analog Input	Reference voltage for ADC and DACs. Value is mid-scale between VDD and GND
AGND3	Analog ground	
RSSI1	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC).
RSSI2	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC). This input is not usable in "Slip" mode.
AVDD3	Analog VDD	
AVDD1	Analog VDD	
VCO1	Analog I/O	Master VCO voltage control input.

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The SX047 Spread Spectrum Transmitter is a highly programmable baseband CMOS integrated circuit that simplifies the design of direct sequence spread spectrum modems. Used to create very low cost transmit-only remote wireless links, the SX047 is designed to interface easily with the SX048 Receiver or the SX049 Transceiver such that multiple SX047 nodes can supply data to a single SX048 or SX049 collector host. Connected to a standard 8 bit microcontroller data bus, the SX047 allows the user to manage internal transmit functions including the type and length of PN codes, data rates, chipping rates, preamble, transmission protocols, power levels, and type of redundancy checks, as well as manage the external circuitry for signal transmission.

Features

- All baseband digital circuitry for direct sequence coded transmissions
- PN clock programmable up to 64M chips per second
- Easy node link interface to AMI's SX048 or SX049
- Psuedorandom noise rates up to 64M chips per second
- Programmable up to 30dB processing gain; PN code lengths from 3 to 2047 chips
- Data and PN code streams available either separately or combined
- Supports BPSK, DBPSK, QPSK, and DPQSK modulation schemes
- Supports RF transmission in any frequency band
- Data rates from 100bps to 4Mbps (BPSK), or 8Mbps (QPSK).
- CRC-32 or CRC-16 redundancy checking available
- Selectable code scrambling for spectral whitening (127 bit data scrambler)
- Address/data bus timing allows interface to many popular 8 bit microcontrollers
- Supports packetized synchronous protocol (HDLC)
- 16 Byte data FIFO reduces interrupt overhead
- Low power 5 volt operation

Figure 1: BLOCK DIAGRAM

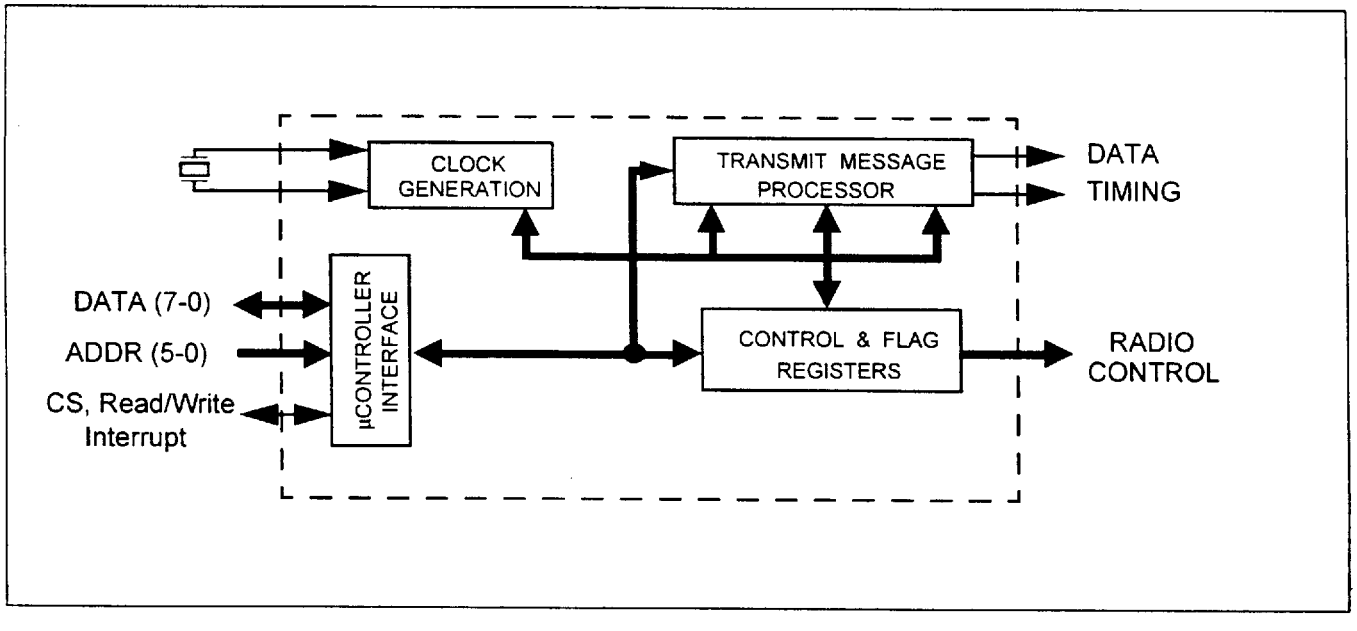

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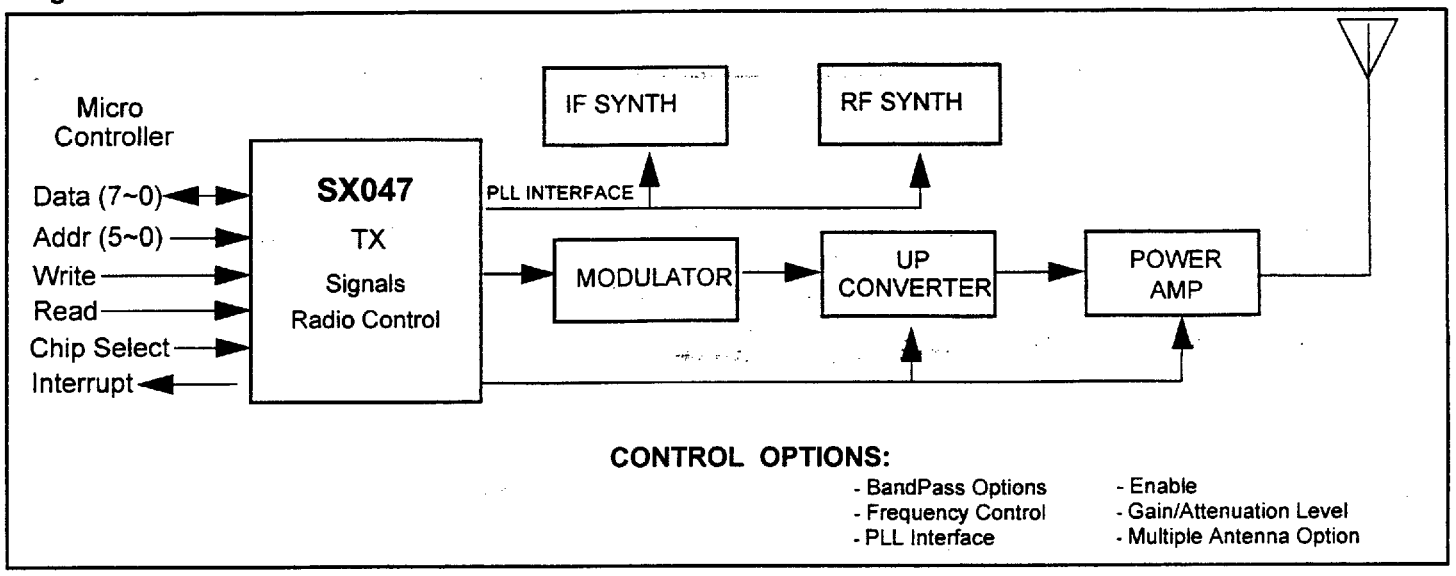
Figure 2. SYSTEM INTERFACE DIAGRAM



Functional Block Overview

The SX047 Block Diagram in Figure 1 details the major functional blocks of the device. The microcontroller manages the Transmit Message Processors independently through various control and flag registers on the IC.

The microcontroller can also use registers in the SX047 to control various radio functions. Figure 2 above represents the full radio implementation using the SX047.

MICROCONTROLLER INTERFACE: The device has a simple bus interface consisting of a bi-directional tri-state eight-bit data bus , a seven-bit address bus, read, write, and chip select inputs, and a general interrupt output. Target microcontrollers for this interface include the 68HC11, 68HC05, 6502, Z8, 8051, 16C5x, and 16C7x.

Power Manager: The user can select one of several power options to minimize power usage.

CONTROL AND FLAG REGISTERS: The SX047 has 19 registers available to the microcontroller. These registers allow programmable control over most characteristics of the transmit channel (See Control Options in Figures 3), as well as off-chip control of the radio portion of the design. (See Control Options in Figure 2)

The SX047 includes a programmable 8 to 96 bit serial RF synthesizer interface. This interface supports any of the three popular serial data transfer styles in RF synthesizers: pulsed transfer, active enable transfer, or clock and data only. It can also be set to a fourth 'user defined' mode. Extra control lines are also available for external circuits that require gain or attenuation level selection, pass band range selection, multiple antenna selection, etc..

CLOCK GENERATION: This is shown as part of the Transmit Message Processor in Figure 3. The clock generation circuit can be programmed to support crystals from 1MHz to 16MHz or can be driven by an external clock line. The 64MHz clock required for the maximum chipping rate and the 4MHz Tx_CLK signal are created in this block. Control options allow other programmable clocking levels and various 'divide by n' registers are provided.

Tx PN Code Generator: The SX047 provides two PN code registers (Code A and Code B), an offset register, and control registers for the creation of various usable maximal length codes and Gold codes. PN code lengths are "OFF", 3, 7, 11, 15, 31, 63, 127, 255, 511, 1027, and 2047. The 11-bit code is the Barker code (Wireless LAN specification IEEE P802.11). Outputs available are the Barker Code, Code A, Code B, or an A+B Gold Code. Disabling the PN code to create a narrowband transmission is also possible.

Tx FIFO: Byte-wide data from the microcontroller is placed in a 16-byte deep FIFO. The 'FIFO near-empty' detect level can be programmed at bytes 0, 2, 4, or 8.

The IC can also be programmed to either abort or end the message in an empty FIFO situation.

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Packet Generator: The Packet Generator controls whether or not the data is sent in packets, and what, if any, preamble and end protocols are added by the SX047. The user may choose to set the packet structure in the controller and then disable the on-chip packet capabilities.

In Packet Mode, the SX047 can generate a repeating preamble code, HDLC protocols, destination address and control commands, CRC-16 or CRC-32 error detection coding, and end codes as selected by the control registers. A packet mode frame format is shown below:

START FLAG	ADDRESS	CONTROL	INFORMATION	CRC	END FLAG
8 bits	8 bits	8 bits	8 * N bits (any length)	16/32 bits	8 bits

The packet mode uses the HDLC algorithm for automatically inserting a zero after any five ones in the address, control, information, and CRC fields of the message.

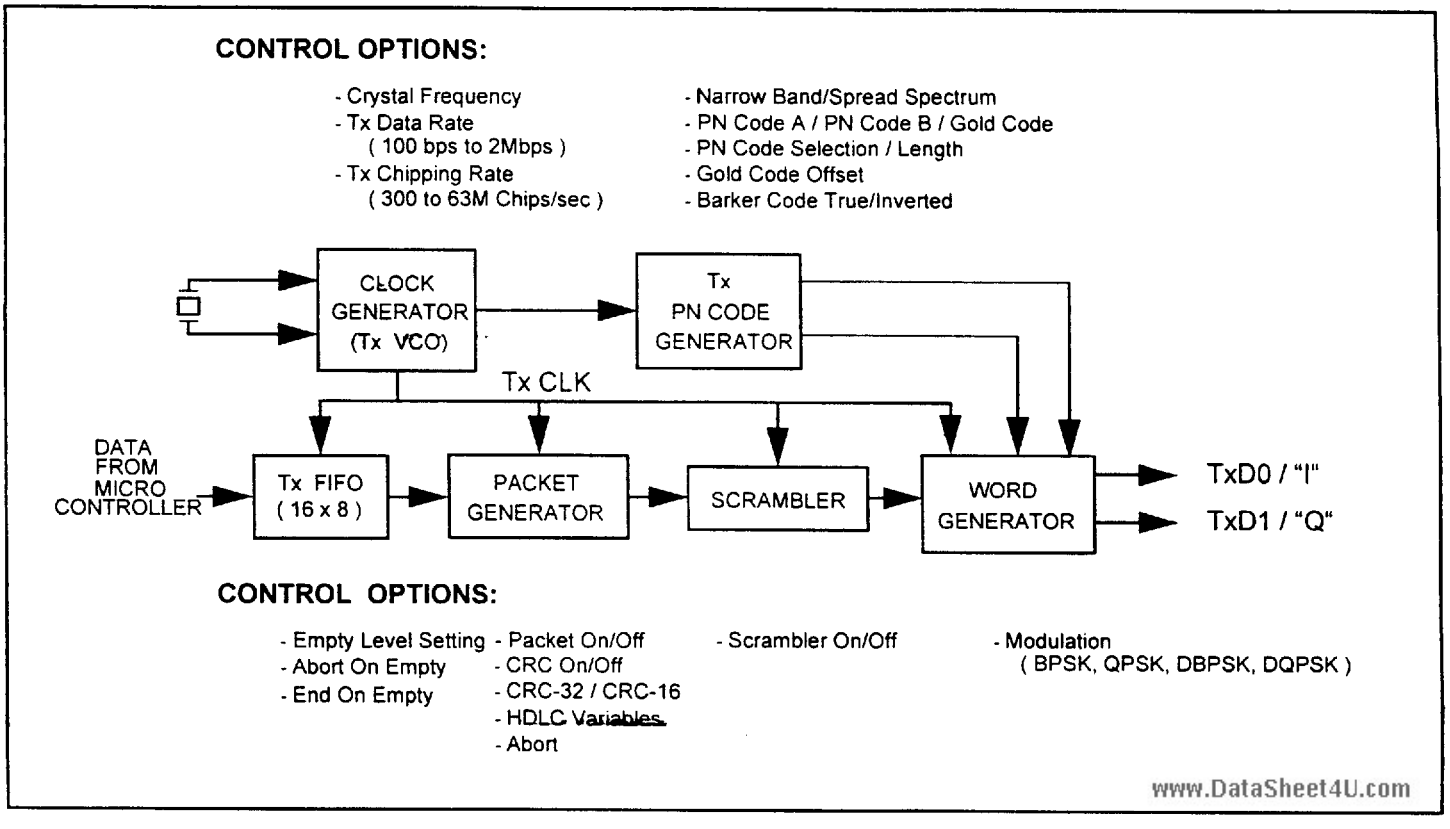
A data underrun (FIFO empty) usually signals that the message is complete, but can be programmed to interpret this condition as an ABORT.

Scrambler: The scrambler is a linear feedback shift register that randomizes the data over a length of 127 bits. The scrambler can be programmed on or off.

Word Generator: The word generator synchronizes the data with the start of the PN code (EPOCH clock) and mixes the PN code with the data transmission. The PN code is running at a much higher frequency than the transmitted data rate, and is sequenced completely once during each data bit period. It is then repeated for each subsequent data bit.

Data can be presented for BPSK, QPSK, Differential BPSK, or Differential QPSK modulation formats. Outputs TxD0 and TxD1, combined with the Tx PN signal, provide the required binary information for the external modulation circuit selected.

Figure 3. TRANSMIT MESSAGE PROCESSOR



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Data Rates

The SX047 can achieve data rates dependent on the PN code lengths used. These are shown below for each modulation scheme (nominal).

BPSK and DBPSK:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15	4M	4M
31	2M	2M
63	1M	1M
127	500K	500K
255	250K	250K
511	125K	125K
1023	62K	62K
2047	31K	31K

QPSK, DQPSK:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15	8M	4M
31	4M	2M
63	2M	1M
127	1M	500K
255	500K	250K
511	250K	125K
1023	125K	62K
2047	62K	31K

* The 11 bit Barker code (1,0,1,1,0,1,1,1,0,0,0).

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Pin Description

NAME:	TYPE:	FUNCTION:
AGND1	Analog ground	
GND1	ground	
VDD1	Vdd	
OSC1	input	Crystal Oscillator or external reference input. This input is divided by OSCDIV to generate the reference clock for the transmit PLL.
OSC2	padosc	Crystal Osc output.
PLL[0:3]	output	Off-Chip PLL programming; bit0, Enable1; bit1, Sclk; bit2, Enable0; bit3, Sdata.
TXD0	output	Transmit data "I" output.
TXD1	output	Transmit data "Q" output.
GND2	ground	
EXT[0:3]	output	External Control port (lower bits), User Defined Functions for radio control.
VDD2	Vdd	
INT	output	Active high. Initiates an interrupt to the microprocessor.
RESET	input	Active low. Sets all registers to default values and forces the SX047 into its standby state.
CS	input	Active low. Selects the chip for reading and writing via the uP interface
RD	input	Active low. Initiates a read operation via the uP interface.
WR	input	Active low. Initiates a write operation via the uP interface.
GND3	ground	
DATA[0:7]	BiDirection	uP Interface data bus.
ADDR[0:6]	input	uP Interface address bus.
VDD3	Vdd	
GND4	ground	
TEST	I/O	Test pin only.
AGND2	Analog ground	

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NAME:	TYPE:	FUNCTION:
AVDD2	Analog VDD	
RBIAS	Analog Input	Current reference for VCO DAC and analog buffers. Nominal resistor value of 30K ohm at 5 volt VDD.
VREF	Analog Input	Reference voltage for DAC. Value is mid-scale between VDD and GND
AGND3	Analog ground	
AVDD3	Analog VDD	
AVDD1	Analog VDD	
VCO1	Analog I/O	Transmit VCO voltage control input.

AMERICAN MICROSYSTEMS, INC.

WavePlex™ Wireless Products

SX047, SX048, SX049

High Data Rate Spread Spectrum Baseband Controllers

April, 1997

Datasheet

1.0 Electrical Specifications

1.1 Operational Ranges

Applies to all following specifications unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VDD/AVDD	Supply voltage	4.5	5	5.5	Volts
Ta	Operating temperature	-40		85	°C

1.2 DC Electrical Operating Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNITS
Vil	Input low voltage			0.25VDD	Volts
Vih	Input high voltage		0.7VDD		Volts
Vol	Output low voltage	Iol = 2mA		0.4	Volts
Voh	Output high voltage	Ioh = -1mA	2.4		Volts
Iil	Input leakage	Vin = 0 Volts to VDD/AVDD		±10	µA
Ioz	Output leakage	I/O = Hi impedance, Vout = 0 Volts to VDD/AVDD		±10	µA
OSCI VIL	Input low voltage			0.1LVDD	Volts
OSCI VIH	Input high voltage		0.9VDD		Volts

1.3 Analog Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DAC LSB	DAC current source, least significant bit		11.3		µA
DAC ZERO	DAC current with 0 input			100	nA
DAC FULL SCALE Source and Sink	DAC current source, with HEX F input	±100	±175	±250	µA
DAC DIFF LIN	DAC differential nonlinearity		±0.2		LSB
ADC STEP1[1,2]	ADC FIRST STEP		190		mV
ADC LSB[2]	ADC least significant bit		154		mV
ADC FULL SCALE[2]	ADC Full Scale		2.35		V
ADC DIFF LIN[2]	ADC differential nonlinearity		±0.50		LSB
VCO GAIN[2]	VCO Gain		45		MHz/Volt
RXDRES[2]	RXD0/1 resistance		60		Ohms
CVIL[2]	Comparator input low voltage			2.25	Volts
CVIH[2]	Comparator input high voltage	2.75			Volts

Specified typical values are from characterization at 25°C, 5.0V AVDD, VDD.

1.4 IDD Characteristics

All IDD tests are done at AVDD=VDD=5.0V, 1 MPBS BPSK, 64 MHz chipping, Internal transmit PN code mixing A & B Gold codes, 50 pF load using the indicated condition.

SYMBOL	CONDITION	MAX.	UNITS
ISLEEP	Sleep Mode	50	µA
ITXS	TX Standby	25	mA
IRXS[2]	RX Standby	45	mA
IALL[3]	Full Duplex	90	mA
IPN1[3]	Full Duplex with PN1 disabled	85	mA
ITXON1[4]	TX on, RX VCO off	65	mA
ITXON2[2]	TX on, RX VCO on	70	mA
IRXON[2]	RX on	70	mA

NOTES 1. ADC STEP1 includes offset. Successive steps defined by ADC/LSB value. 2. Applies to SX048 and SX049 only. 3. Applies to SX049 only. 4. Applies to SX047 and SX049 only.

2.0 Microcontroller Interface Read/Write Timing

2.1 Read Timing Characteristics

See Figure 2: Read Timing Diagram.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
Tcsd	Read chip select low to valid data out		45	nS
Trd	Read low to valid data out		45	nS
Tcsdz	Chip select high to data bus disable		15	nS
Trdz	Read high to data bus disable		15	nS
Tcsur	Read chip select setup	0		nS
Tchr	Read chip select hold	10		nS
Tadrsur	Read address setup	10		nS

2.2 Write Timing Characteristics

See Figure 1: Write Timing Diagram.

SYMBOL	PARAMETER	MAX.	UNITS
Tcsuw	Write chip select setup	0	nS
Tchw	Write chip select hold	10	nS
Tadrsuw	Write address setup	10	nS
Tadrh	Write address hold	10	nS
Tdsu	Write data setup time	10	nS
Tdh	Write data hold	10	nS

For additional information please contact your nearest AMI representative for a Spread Spectrum IC User's Manual.

Figure 2: Microcontroller Read Timing

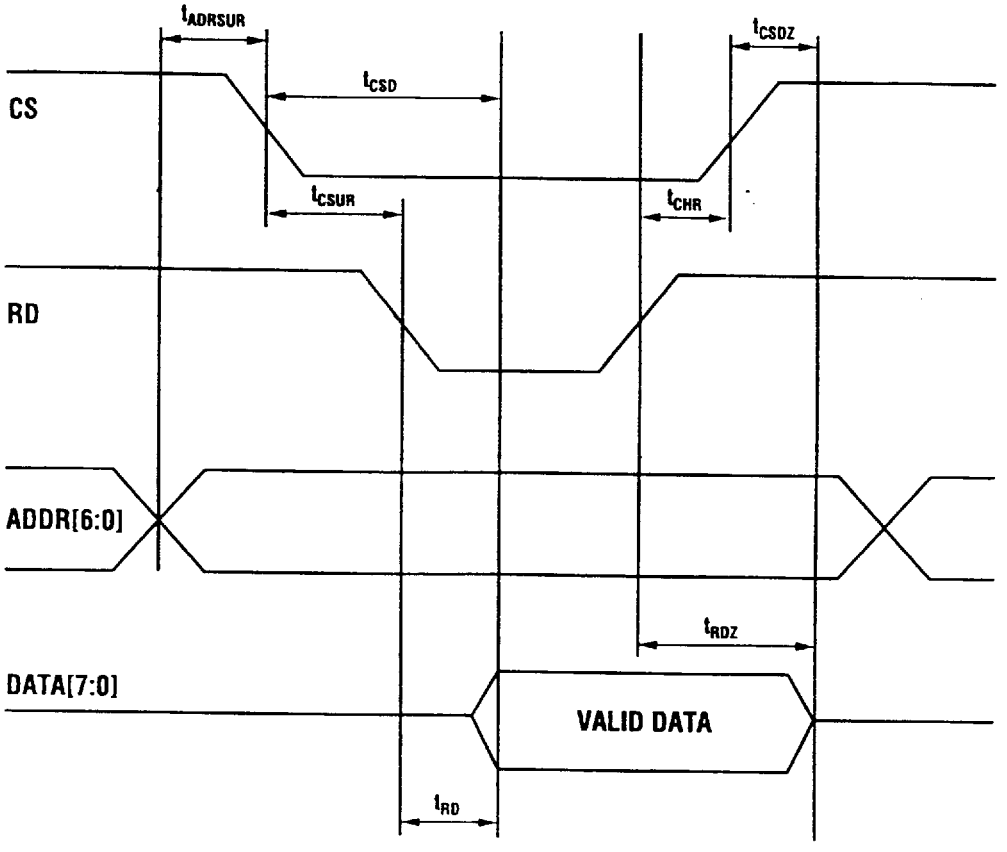


Figure 3: Input Test Waveforms and Measurment Levels

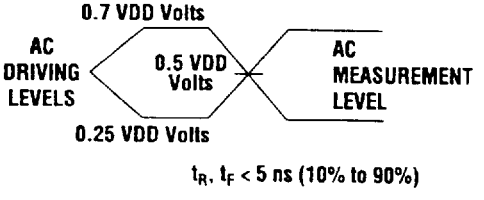


Figure 4: Output Test Load

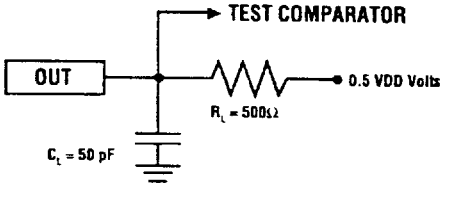
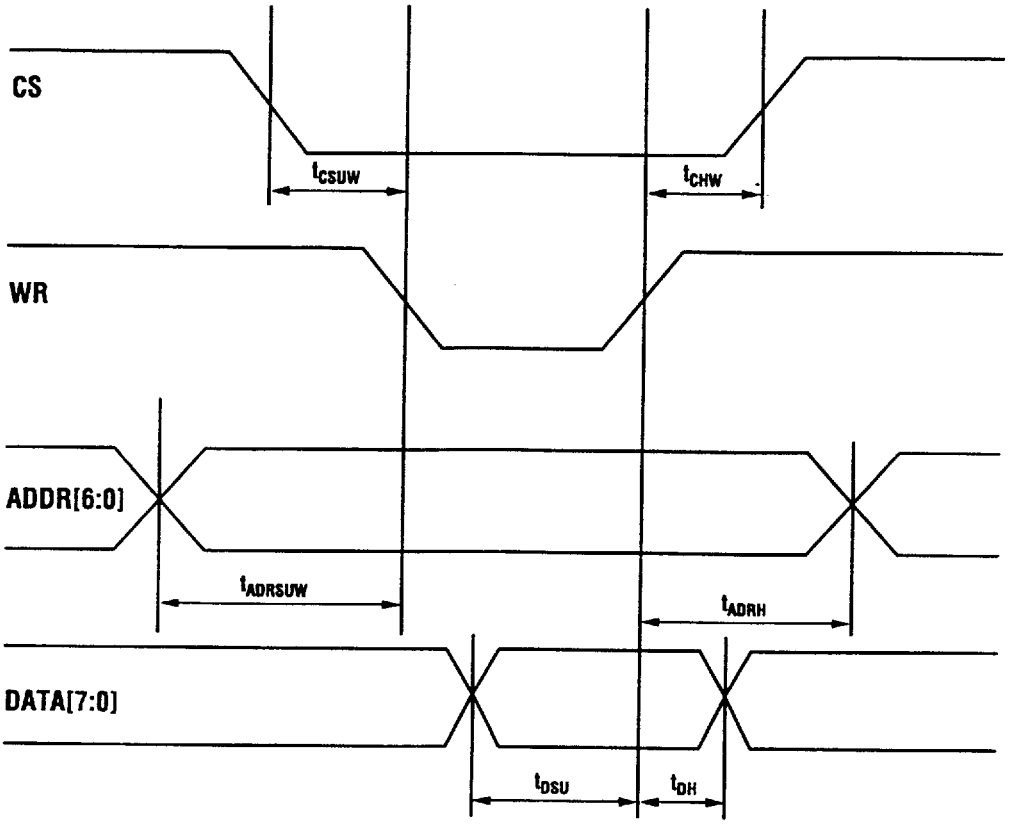


Figure 1: Microcontroller Write Timing



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General Description

The SX049 Spread Spectrum Transceiver is a highly programmable baseband CMOS integrated circuit that simplifies the design of direct sequence spread spectrum modems.

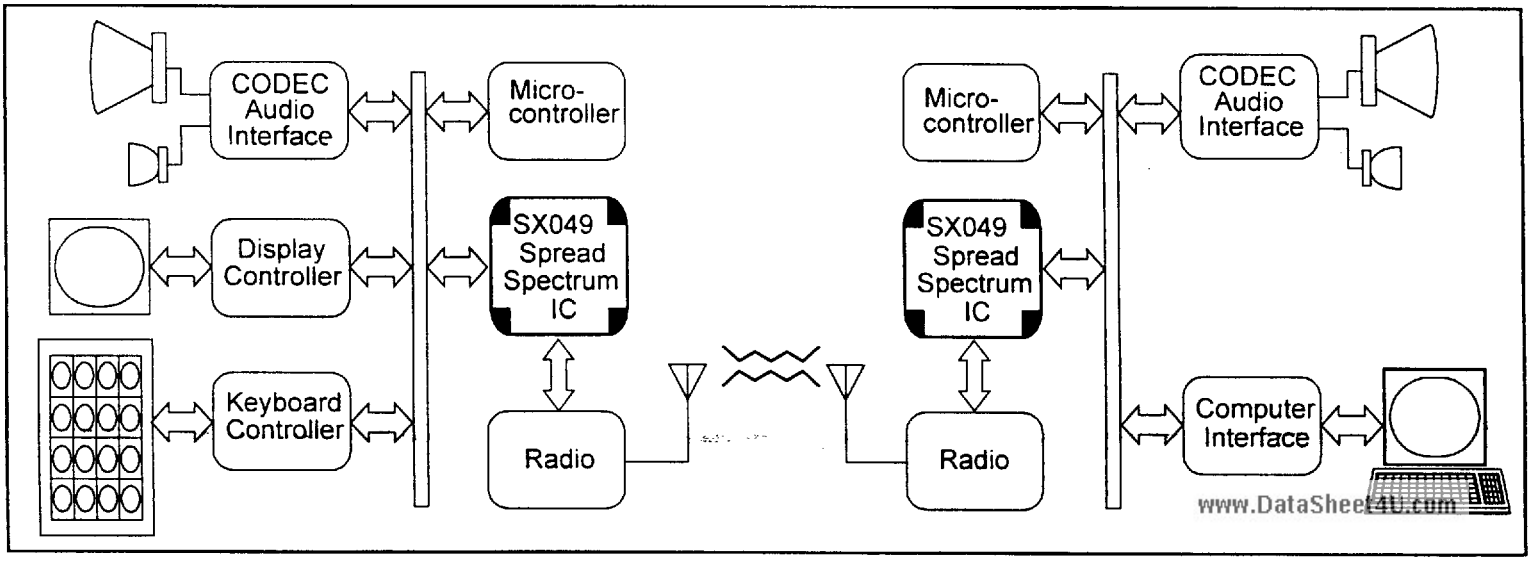
The SX049's internal functions include transmit and receive PN code generators; an acquire-and-track synchronization engine in the receiver; separate packet management units for transmit and receive; a complete 8-bit microcontroller interface with separate transmit and receive data FIFO's; and control logic and registers to allow active control of the IF and RF circuitry.

A user can program the SX049 at system power-up and then actively manage the IC to dynamically configure the radio for optimum spectral performance as both a transmitter and a receiver.

Features

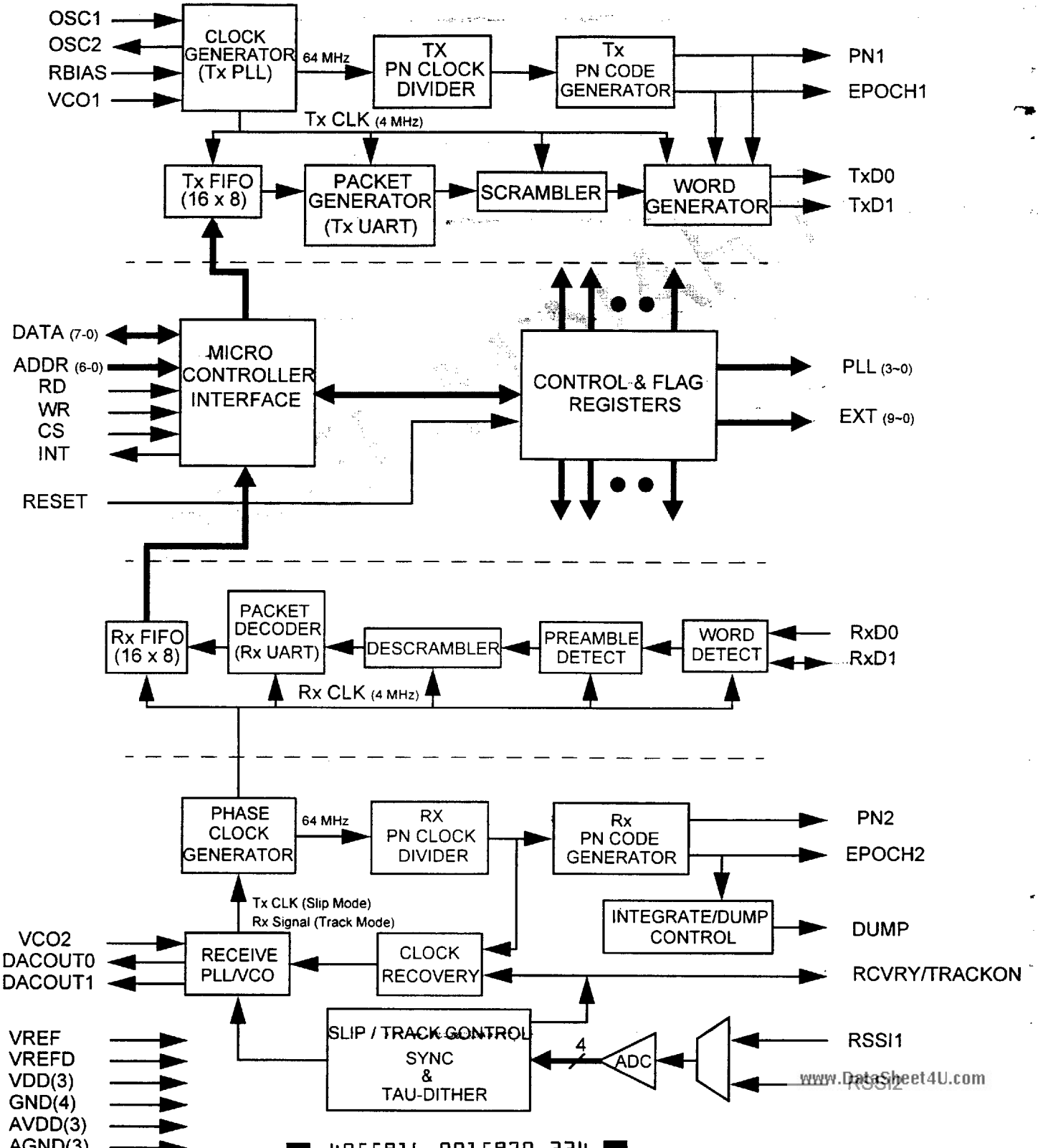
- Low cost CMOS implementation
- Low power (5 volt) with user controlled 'shutdown' modes
- Narrow band and Spread Spectrum operation
- Complete digital and analog baseband circuitry
- Supports RF transmission in any frequency band
- User programmable transmission protocol with 'pass through' or packetization formatting
- Standard microcontroller interface
- Full or Half duplex operation
- PN rates up to 64 Megachips per second
- Independent transmit and receive PN code generators, with Gold Code and 11-chip Barker Code options
- High process gain (up to 2047 chips/bit) and full range of PN code lengths from 'off' to 2047
- Data rates from 100 bps to 4 Mbps (BPSK) or 8 Mbps (QPSK) or 12 Mbps (QAM8) or 16 Mbps (QAM16).
- Programmable preamble lengths for faster acquisition when there has been recent transmission or reception
- 16 byte transmit and receive data FIFOs reduce interrupt overhead
- Support for BPSK, DBPSK, QPSK, DQPSK, QAM8, and QAM16 modulations
- Transmit and Receive codes can be independent
- Automatic cyclic redundancy check generation and detection (CRC-16 or CRC-32)
- Provides selectable code scrambling for spectral whitening code generation (127 bit data scrambler)
- Packetized synchronous protocol (HDLC) including abort sequence generation and checking, automatic zero insertion and deletion, and address field recognition

Figure 1: Example Target Application



This IC was designed in cooperation with Seattle Silicon Corporation. It licenses proprietary property of Seattle Silicon including:

Figure 2: SX049 BLOCK DIAGRAM



AMERICAN MICROSYSTEMS, INC.

WavePlex™ Wireless Products

January, 1997

SX049

High Data Rate

Spread Spectrum Transceiver

PRODUCT DESCRIPTION

Target Applications

The SX049 is intended for a wide range of remote data terminal applications that can benefit from FCC regulations concerning spread spectrum in any of the ISM bands.

Low data rate applications (from 100bps) may select the maximum length PN codes of 2047 to get processing gains to 32dB. Medium speed systems (250k to 1Mbps) may select PN code lengths from 63 to 255, and high-end systems at 1M to 16M bps can use the shorter maximal length sequences or the 11-bit barker code for optimum spreading.

Since SX049 features are actively programmable, sophisticated applications that monitor the spectrum and adapt the radio characteristics to minimize power and error rates are particularly good uses of the device.

Functional Overview

The SX049 Block Diagram is shown on Page 2. This drawing suggests the pin connections required for the part. Dashed lines are used to separate the four major function blocks of the device. From the top of the drawing these are: 1) the Transmit Message Processor; 2) the Microcontroller Interface and Control Registers; 3) the Receive Message Processor; and 4) the Analog Sync/Track engine.

Figure 3 below is a system block diagram of the SX049 and the required external IF and RF blocks. Notice that the modulation, despreading, and demodulation are functions external to the IC.

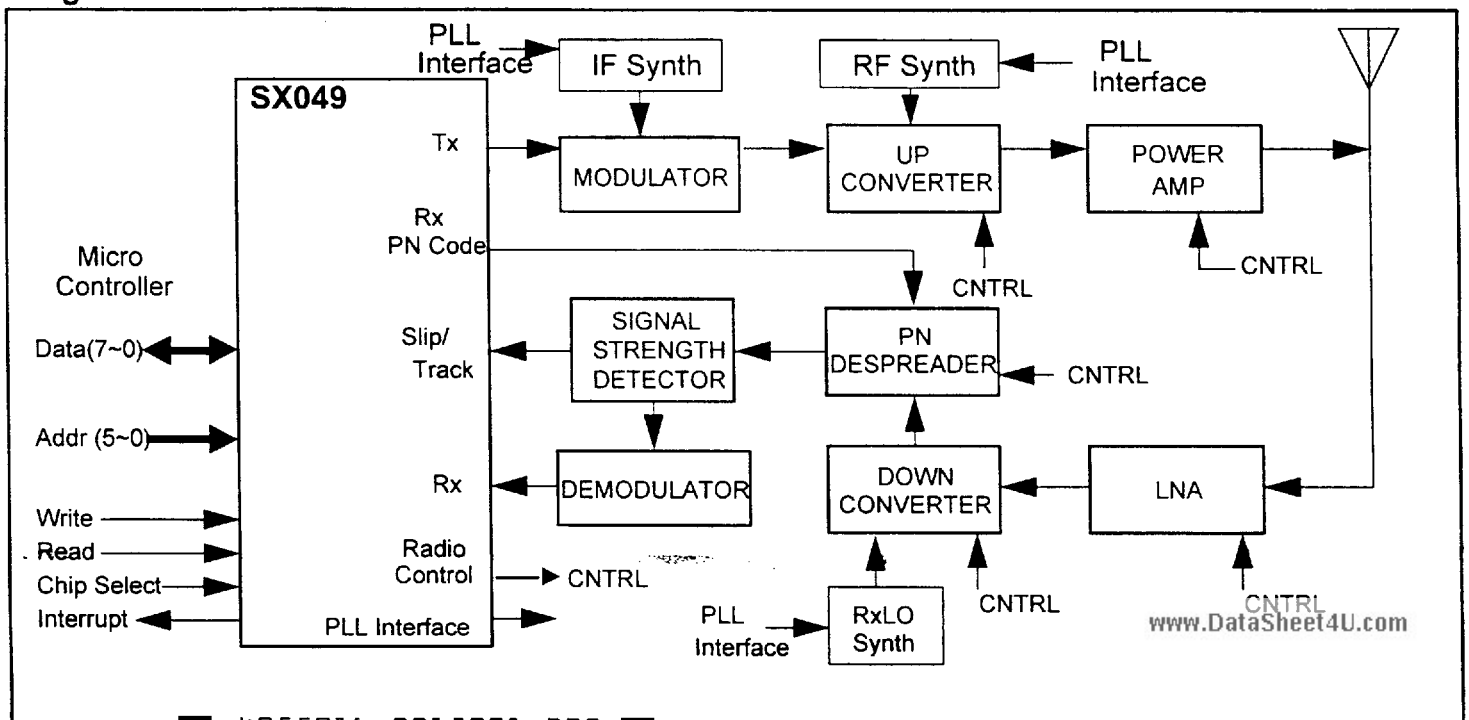
MICROCONTROLLER INTERFACE AND CONTROL REGISTERS: The device has a simple bus interface consisting of a bidirectional tri-state eight-bit data bus, a seven-bit address bus, read, write, and chip select inputs, and a general interrupt output. Target microcontrollers for this interface include the 68HC11, 68HC05, 6502, Z8, 8051, 16C5x, and 16C7x.

Power Manager: The IC has a 'sleep' mode that disables both Transmit and Receive VCO's and turns all active circuitry off. There are also separate 'Tx Standby' and 'Rx Standby' states that selectively power down the transmitter or receiver.

Control and Flag Registers: The SX049 has 45 registers available to the microcontroller. These registers allow programmable control over most characteristics of the Transmit and Receive channels as well as off-chip control of the radio portion of the design.

Depending on package type, ten (10) latchable EXT radio control output pins are available for uncommitted use. Typical applications include transmitter power levels, receiver gain levels, antenna selection, and channel filter selection.

Figure 3: SYSTEM INTERFACE DIAGRAM



Four (4) pins are available for serial stream programming of Tx and Rx RF PLL frequencies. Embedded programmable logic supports I²C, Pulsed Transfer, Active Enable Transfer, or direct user control. Serial data streams of 96 bits can be pre-written into the IC for PLL programming.

TRANSMIT MESSAGE PROCESSOR: The Transmit channel provides a complete Tx UART function for the environment.

Clock Generator (Tx PLL): The clock generation circuit can be programmed to operate with a crystal or system clock input of 1MHz to 16MHz. The 64MHz clock required for the maximum chipping rate and the 4MHz Tx_CLK signal are created in the PLL in this block.

Tx PN Clock Divider: The IC allows programmable PN chipping rates from 300 Hz to 64MHz. The PN chipping clock is programmed in this block.

Tx PN Code Generator: The SX049 provides two PN code registers (Code A and Code B), an offset register, and control registers for the creation of various usable maximal length and Gold codes. PN code lengths are "OFF", 3, 7, 11, 15, 31, 63, 127, 255, 511, 1027, and 2047. (The 11-bit code is the Barker code.) Outputs available for signal spreading are the Barker Code, Code A, Code B, or 'A + offset B' Gold codes. Disabling the PN code to create a narrowband transmission is also possible.

Tx FIFO: Byte-wide data from the microcontroller is placed in a 16-byte deep FIFO. The 'FIFO near-empty' detect level can be programmed at bytes 4, 8, 12, or 16. The IC can also be programmed to either abort or end the message in an empty FIFO situation.

Packet Generator: The Packet Generator builds the necessary preamble and preamble-end nibbles. The IC can be set in packet mode where it build a complete HDLC packet or in non-packet mode where FIFO bytes are appended to the preamble and shipped until the FIFO is empty.

Preamble Length: The SX049 uses a 'sliding correlator' synchronization approach to keep implementation costs and IC power low. The receive PN code is basically slipped one-half chip each data bit, and compared to the Tx PN code until the two codes synchronize. This requires a preamble bit length that increases with the length of the PN code used. The User Manual should be consulted for complete computational details.

A Short Preamble mode is supported in both full and half duplex to allow faster re-acquisitions in the event that there has been a recent transmission or reception to or from another transceiver.

Packet Generation: In Packet Mode, the SX049 generates the preamble code, HDLC protocols, including destination addresses, CRC-16 or CRC-32 error detection coding, and end codes as selected by the control registers.

A packet mode frame format is shown below:

START FLAG	ADDRESSES	INFORMATION	CRC	END FLAG
8 bits	16 bits	8 * N bits (any length)	16 / 32 bits	8 bits

Figure 4: TRANSMIT MESSAGE PROCESSOR

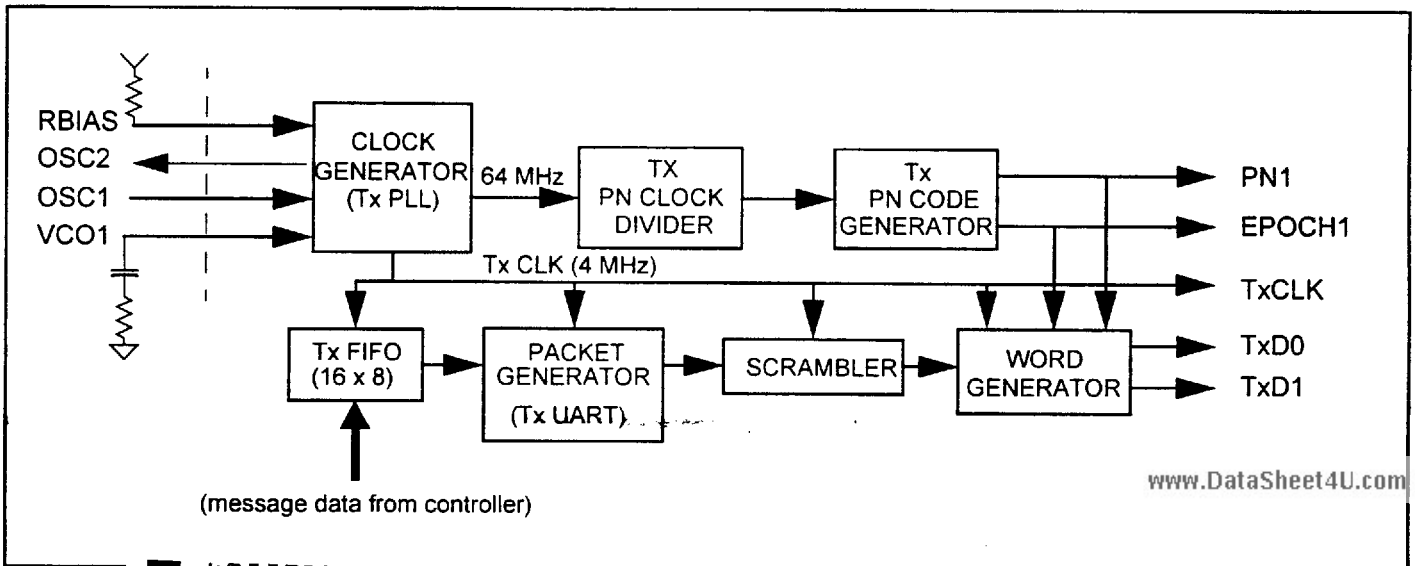
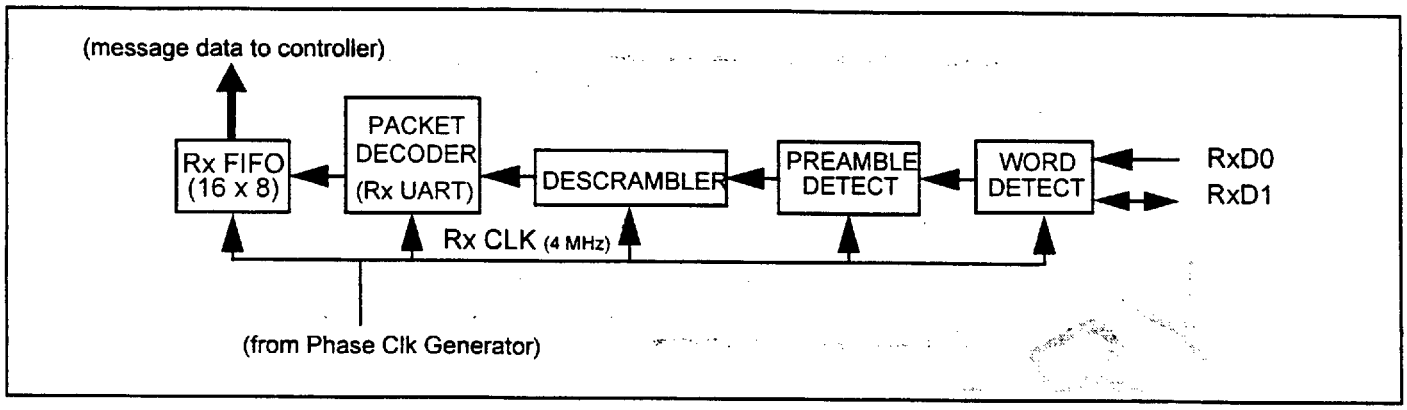


Figure 5: RECEIVE MESSAGE PROCESSOR



The packet mode uses the HDLC algorithm for automatically inserting a zero after any five ones in the address, information, and CRC fields of the message.

A data underrun (FIFO empty) usually signals that the message is complete, but can be programmed to interpret this condition as an ABORT.

Scrambler: The scrambler is a linear feedback shift register that randomizes the data over a length of 127 bits. The scrambler can be programmed on or off.

Word Generator: The word generator synchronizes the data with the start of the PN code (Epoch clock). The PN code is running at a much higher frequency than the transmitted data rate, and is sequenced completely once during each data bit period. It is then repeated for each subsequent data bit.

For BPSK, Differential BPSK, QPSK, and Differential QPSK the PN code can be programmed to be mixed with the data on the IC, or this mixing can be bypassed. In QAM8 and QAM16 modes the data is presented without PN mixing at the TxD0 output.

Output pins TxD0 and TxD1, combined with the PN1 and EPOCH1 signals provide the required signals. The use of the pins in each of the selectable modes is covered in detail in the Data Sheet and User's Manual.

RECEIVE MESSAGE PROCESSOR: The Receive channel (Figure 5 above) processes the receive message and delivers bytes of data to the microcontroller.

Word Detect: The Word Detect circuit reconstructs a single data stream from the incoming data streams processed by the external demodulator. BPSK, QPSK, DBPSK, DQPSK, QAM8, or QAM16 results from the demodulator are presented on the RxD0 and RxD1 pins to internal VREF comparators that set one/zero levels.

Preamble Detect: The Preamble Detect searches the incoming stream for the expected repeating preamble code followed by the end-of-preamble code. It determines bit phase and confirms that a valid message is being received.

Descrambler: The Descrambler recovers the data that was scrambled in the Transmit channel. The descrambler can be programmed on or off.

Packet Decoder: The Packet Decoder verifies the destination address and then recaptures the raw data for the microcontroller. The decoder alerts the controller of any receive (CRC) errors, abort codes, lost tracking, and end-of-message information via interrupts and status registers.

Rx FIFO: Byte-wide data for the microcontroller is placed in a 16-byte deep Rx FIFO. The 'FIFO near-full' detect level can be programmed at bytes 1, 5, 9, or 13. The FIFO relays status to the microcontroller by means of the interrupt pin and control registers.

ANALOG SYNC / TRACK ENGINE: The Sync / Track engine synchronizes the receiver PN code to the incoming signal and then maintains track on the signal until the end-of-message is received.

Receive PLL / VCO: In the 'slip', or acquire, mode this circuit locks on the 4MHz Tx Clk signal so that half chip slips can be made at the programmed PN clock rate until synchronization occurs and 'track' begins.

In 'track' mode this block becomes a VCO that is driven by slight voltage variations around the correlation peaks as measured on the RSSI1 input signal. This dithering of the frequency around the correlation peak allows the IC to maintain 'track'.

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Sync / Track Control: This state machine manages the synchronization function for the IC based on the control register settings and the action of the incoming message. The RSSI signals are analog level inputs that supply the "Receive Signal Strength" level of the incoming signal after despreading. Programmability and use of this state machine is covered in the User's Manual.

Rx PN Clock Divider: The IC allows programmable PN chipping rates from 300 Hz to 64MHz. The receive PN chipping clock is programmed in this block.

Rx PN Code Generator: The SX049 provides two Rx PN code registers (Code A and Code B), an offset register, and control registers for the creation of various usable maximal length and Gold codes. PN code lengths are "OFF", 3, 7, 11, 15, 31, 63, 127, 255, 511, 1027, and 2047. (The 11-bit code is the Barker code.) Outputs available for signal despreading are the Barker Code, Code A, or 'A + offset B' Gold codes. Disabling the PN code to receive a narrowband transmission is also possible.

PN2, EPOCH 2 (except in 64 pin version) and DUMP are output pins that manage the off-chip despreading and demodulation functions. The reader is referred to the SX049 Data Sheet for further detail on these and other block functions.

Data Rates

The SX049 can achieve data rates dependent on the PN code lengths used. These are shown below for BPSK and QPSK modulation schemes (nominal). QAM8 and QAM16 can produce data rates to 16M bps. Since they require external ADC's and DAC's and may have limited application, they are not shown here.

PN Code Length	Maximum Symbol Rate symbols/sec	BPSK, DBPSK Maximum Data Rate bits/sec	QPSK, DQPSK Maximum Data Rate bits/sec
3, 7, 11*, 15	4 M	4 M	8 M
31	2 M	2 M	4 M
63	1 M	1 M	2 M
127	500 K	500 K	1 M
255	250 K	250 K	500 K
511	125 K	125 K	250 K
1023	62 K	62 K	125 K
2047	31 K	31 K	62 K

* The 11 bit Barker code (1 0 1 1 0 1 1 1 0 0 0).

Packaging

The SX049 is available in the following surface mount packages:

68 pin Plastic Leaded Chip Carrier (PLCC)
64 pin Plastic Quad Flat Pack (PQFP)
64 pin Thin Plastic Quad Flat Pack (TPQFP)

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Pin Description

Name:	Type:	Function:
AGND1	Analog GND	
GND1	ground	
VDD1	Vdd	
OSC1	input	Crystal Oscillator or external reference input. This input is divided by OSCDIV to generate the reference clock for the transmit PLL.
OSC2	padosc	Xtal Osc output.
PLL[0:3]	output	Off-Chip PLL programming; bit0, Enable1; bit1, Sclk, bit2, Enable0, bit3, Sdata.
TXD0	output	Transmit data "I" output.
TXD1	output	Transmit data "Q" output, or QAM output clock.
* EPOCH1	output	Transmit PN Generator Epoch Signal.
PN1	output	Transmit PN Generator output, can be internally disabled (PMR bit 4).
GND2	ground	
EXT[0:3]	output	External Control port (lower bits), User Defined Functions for radio control.
VDD2	Vdd	
* EXT[4:9]	output	External Control port (upper bits), User Defined Functions for radio control.
INT	output	Active high. Initiates an interrupt to the microprocessor.
RESET	input	Active low. Sets all registers to default values and forces the SX049 in its standby state.
CS	input	Active low. Selects the chip for reading and writing via the uP interface.
RD	input	Active low. Initiates a read operation via the uP interface.
WR	input	Active low. Initiates a write operation via the uP interface.
GND3	ground	
DATA[0:7]	BiDirection	uP Interface data bus.
ADDR[0:6]	input	uP Interface address bus.
VDD3	Vdd	
GND4	ground	
DUMP	output	Integrate & Dump Control logic output.
* EPOCH2	output	Receive PN Generator Epoch Signal.
PN2	output	Receive PN Generator output.
RCVRY	BiDirection	Clock recovery input for Narrow Band Mode. Track-On (active high) output for Spread Spectrum Mode. Indicates to external circuitry that the SX049 is locked and tracking the received PN code.

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Name:	Type:	Function:
RXD0	Analog In	Receive data input 'I'.
RXD1	Analog I/O	Receive data input 'Q' or QAM mode output clock to external shift register.
VREFD	Analog In	Reference voltage for integrate and dump comparators and switches.
AGND2	Analog GND	
VCO2	Analog Input	Receive VCO control voltage input.
AVDD2	Analog VDD	
DACOUT0	Analog Output	Receive PLL DAC output during SLIP operation.
DACOUT1	Analog Output	Receive DAC output during TRACK operation. Note: DACOUT0 and DACOUT1 are provided in the event separate gain control is necessary for SLIP and TRACK operation.
RBIAS	Analog Input	Current reference for DACs and analog buffers. Nominal resistor value of 30K ohm for 5 volt VDD.
VREF	Analog Input	Reference voltage for ADC and DACs. Value is mid-scale between VDD and GND.
AGND3	Analog GND	
RSSI1	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC).
RSSI2	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC).This input is not usable in "Slip" mode.
AVDD3	Analog VDD	
AVDD1	Analog VDD	
VCO1	Analog I/O	Transmit VCO voltage control input.

* EPOCH 1, EPOCH2 and EXT pins 8:9 are not available in the 64 pin versions of the SX049.