XZ1001-BD

2.5-4.0 GHz GaAs MMIC
S-Band Core

Rev 01-Sep-10

M/A-COM Tech Asia

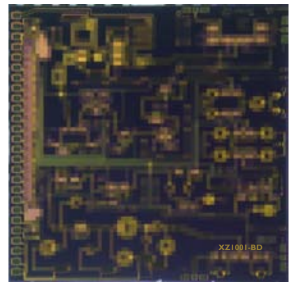
Features

- Highly Integrated Core Chip
- Transmit and Receive Modes of Operation
- Integrated T/R Switches, LNA and Driver Amplifier
- 6-Bit Phase Shifter and 6-Bit Attenuator
- 33.0 dB Small Signal RX Gain
- +20 dBm TX P1dB Compression Point
- Compensated On-Chip Gate Bias Circuit
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010

General Description

The XZ1001-BD is a highly integrated transmit/receive 4 port core chip. It is designed for applications operating within the 2.5 to 4 GHz range. The core consists of integrated transmit/receive switches, LNA, 6-bit phase shifter, 6-bit attenuator and driver amplifier. The digital control logic allows fast phase shifter and attenuator changes. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for phased array radar applications.

Chip Device Layout



Absolute Maximum Ratings

Supply Voltage (Vd)	8V
Gate Supply (Vs)	TBD
Logic Supply (Vl)	5V
Supply Current (Id)	676 mA
Input Power	TBD
Storage Temperature (Tstg)	-65 to +165 ºC
Operating Temperature (Ta)	-55 to MTTF
Channel Temperature	TBD

Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.

Electrical Characteristics (Ambient Temperature T=25 ºC)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	2.5		4
Input Return Loss RX/TX Mode (S11)	dB		-10	
Output Return Loss RX/TX Mode (S22)	dB		-15	
Receive/Transmit Small Signal Gain (S21)	dB		33	
Receive/Transmit Output Power for 1 dB Compression Point	dBm		20	
Receive Noise Figure (NF)	dB		2.5	
Receive Output Third Order Intercept (OIP3)	dBm		TBD	
Phase Shifter Range (6 Bit, 64 states, 5.625 deg step)	deg	0		354.375
Phase Shifter RMS Phase Error	deg		1.5	
Phase Shifter RMS Amplitude Error	dB		0.7	
Attenuator Range (6 Bit, 64 states, 0.45 dB step)	dB	0		28.35
Attenuator RMS Amplitude Error	dB		0.3	
Attenuator RMS Phase Error	deg		1.5	
Drain Bias Voltage (Vd1,2)	VDC	-	5	
Drain Bias Voltage (Vd3)	VDC	0.5	7	
Gate Bias Voltage (Vs1,2)	VDC		-10	-
Control Voltage High (I1A,2,3,4,5,56) & (I1P2,3,4,5,6)	VDC	+2.0	+3.3	+5.0
Control Voltage Low (I1A,2,3,4,5,56) & (I1P2,3,4,5,6)	VDC	0.0		+0.8
Supply Current (Id1) [Vs(1,2)=-10V, VD(1,2)=5V, VD3=7V]	mA		22	
Supply Current (Id2) [Vs(1,2)=-10V, VD(1,2)=5V, VD3=7V]	mA		60	
Supply Current (Id3) [Vs(1,2)=-10V, VD(1,2)=5V, VD3=7V]	mA		270	

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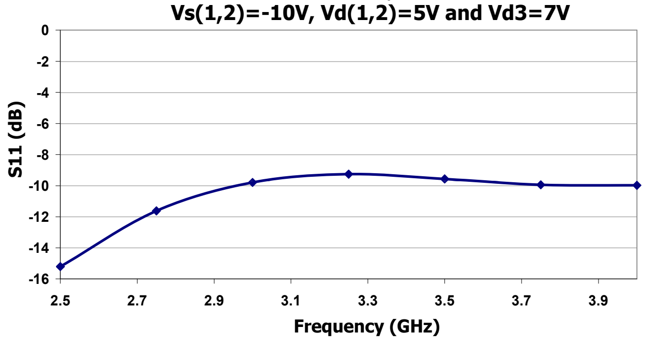
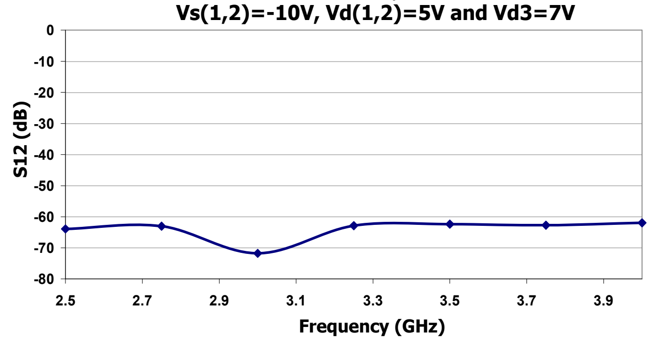
Typical Performance

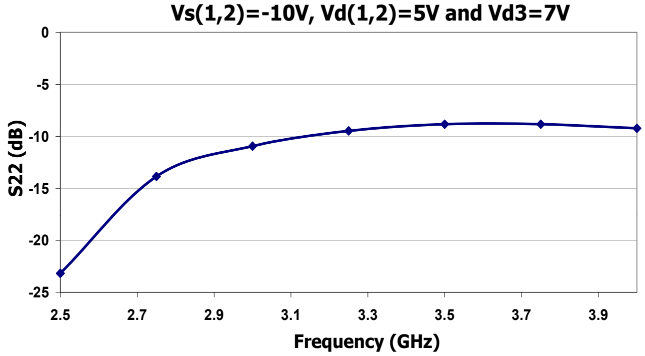
S11 in Transmit mode, reference state
Vs(1,2)=-10V, Vd(1,2)=5V and Vd3=7V



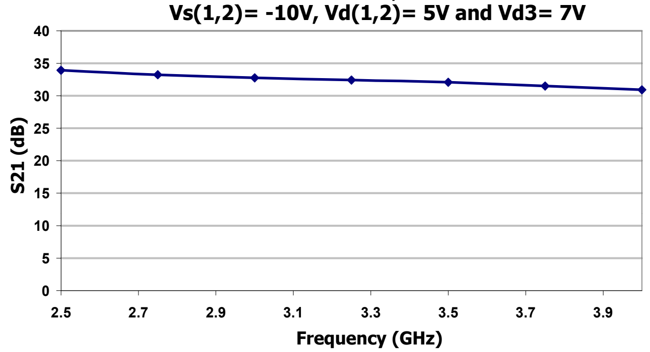
S12 in Transmit mode, reference state
Vs(1,2)=-10V, Vd(1,2)=5V and Vd3=7V



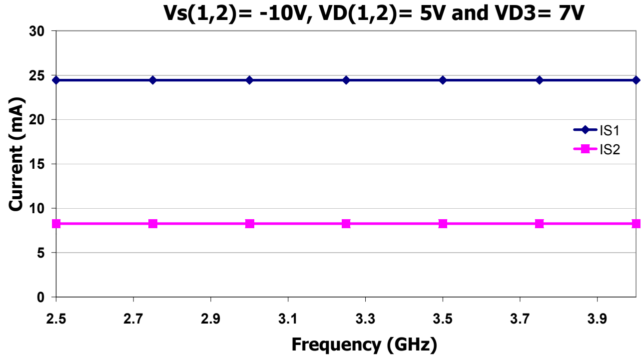
S22 in Transmit mode, reference state
Vs(1,2)=-10V, Vd(1,2)=5V and Vd3=7V



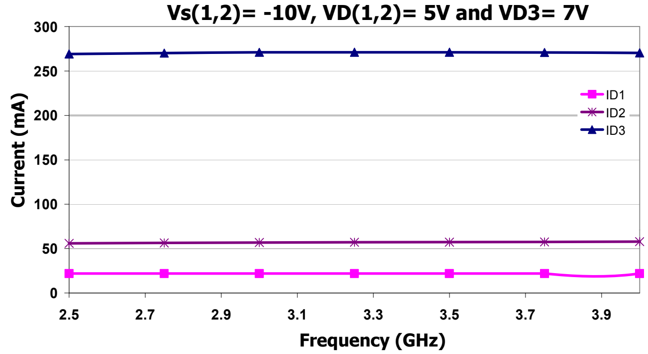
S21 in Transmit mode, reference state
Vs(1,2)= -10V, Vd(1,2)= 5V and Vd3= 7V



Gate Bias currents
Vs(1,2)= -10V, VD(1,2)= 5V and VD3= 7V



Drain Bias currents
Vs(1,2)= -10V, VD(1,2)= 5V and VD3= 7V



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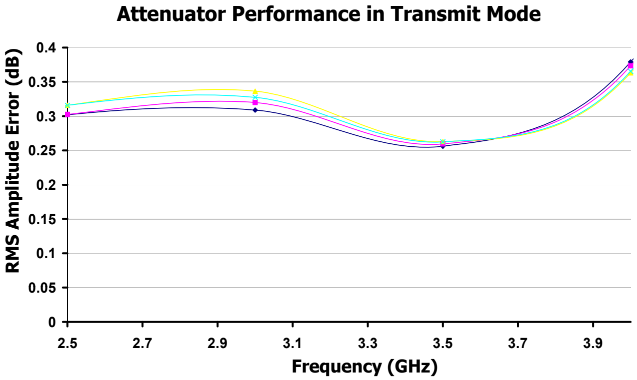
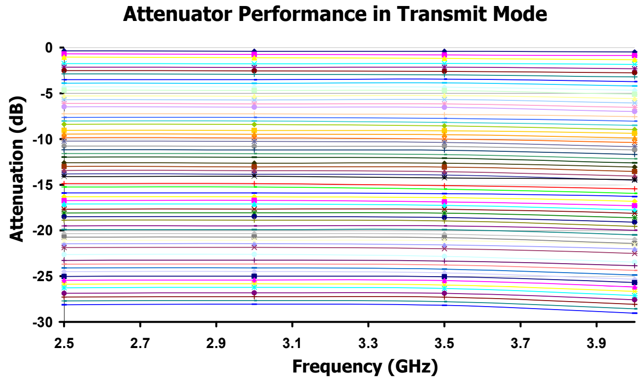
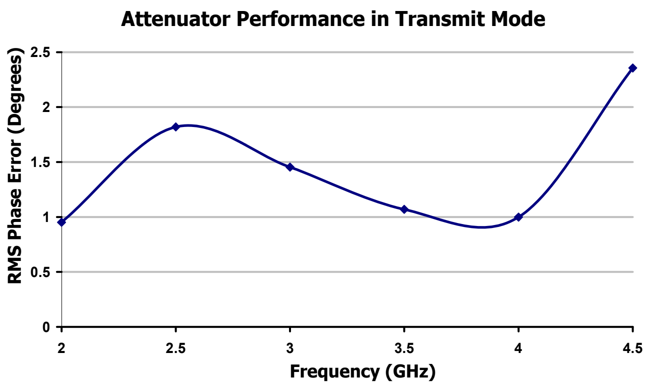
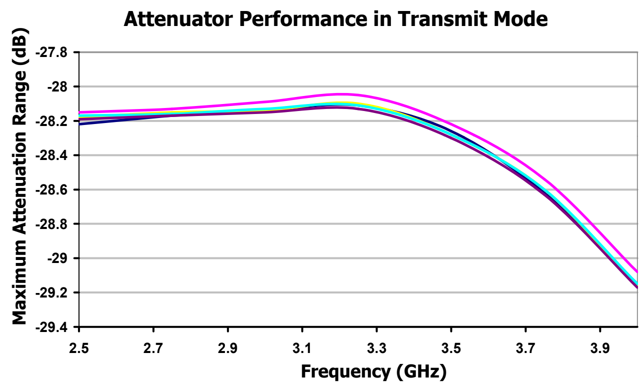
Attenuator Measurements

The following bias conditions were used to test the attenuator: Vs(1,2)= -10V, Vd(1,2)=5V and Vd3=7V.









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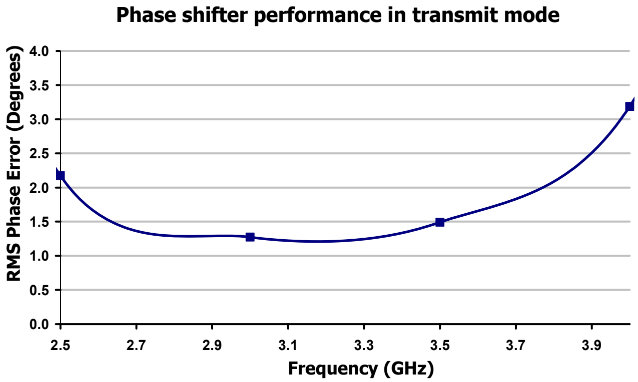
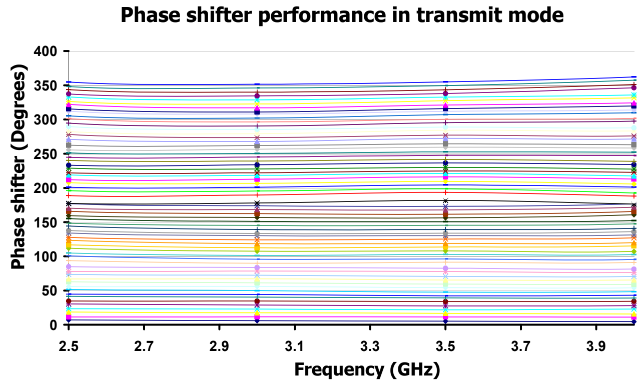
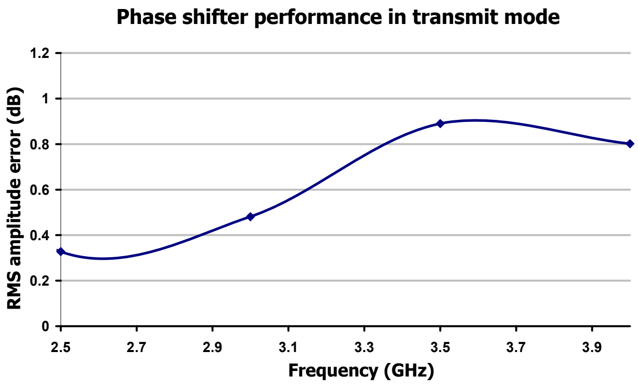
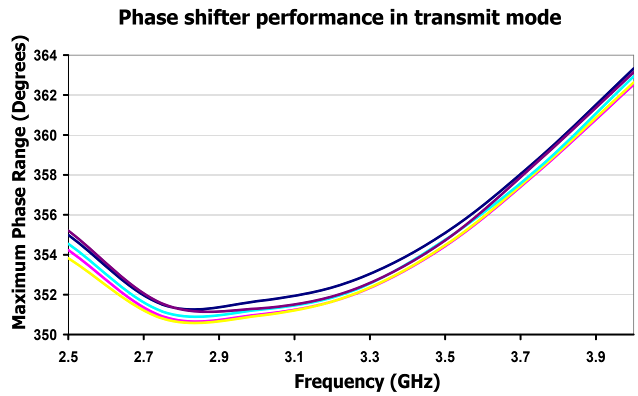
Phase Shifter Measurements

The following bias conditions were used to test the phase shifter: Vs(1,2)= -10V, Vd(1,2)=5V and Vd3=7V.









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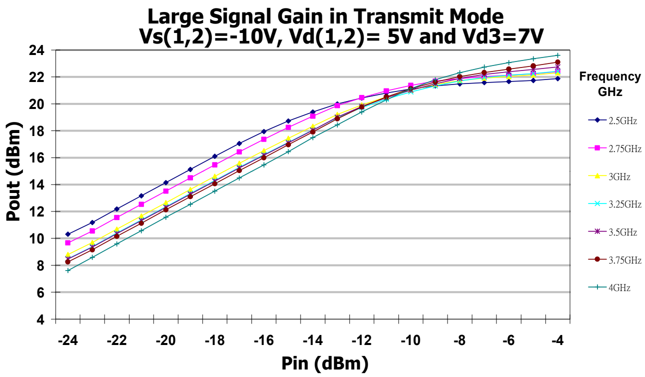
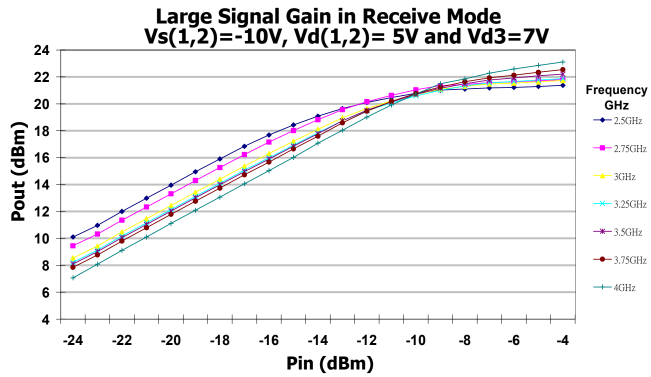
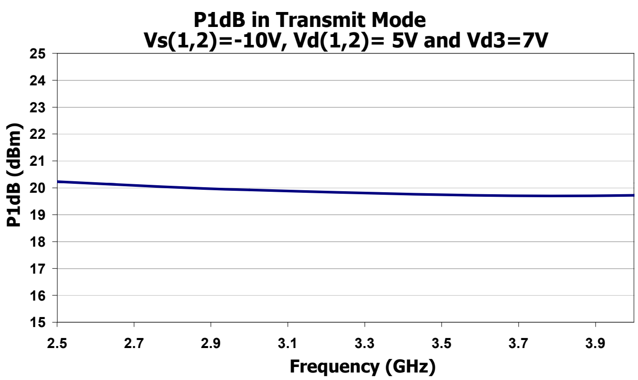
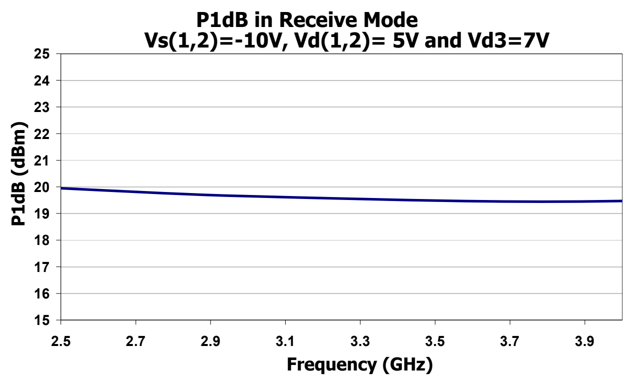
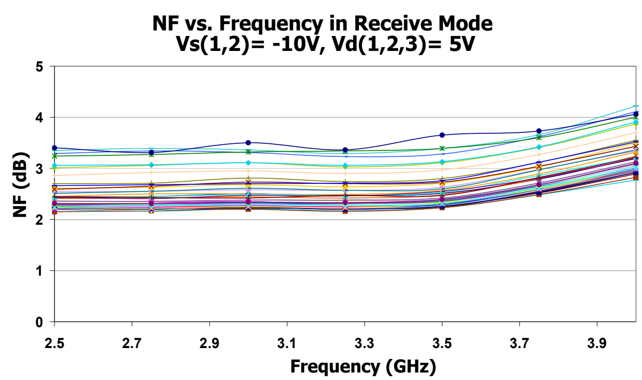
Power Measurements











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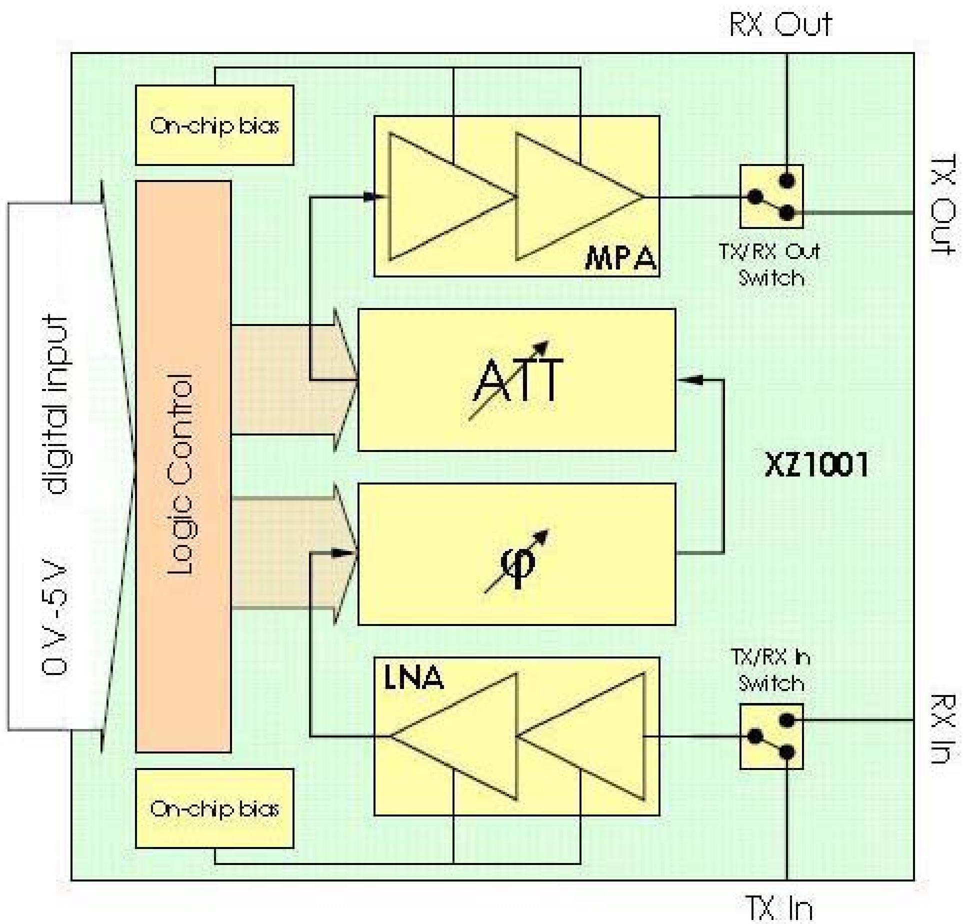
Core Chip Block Diagram



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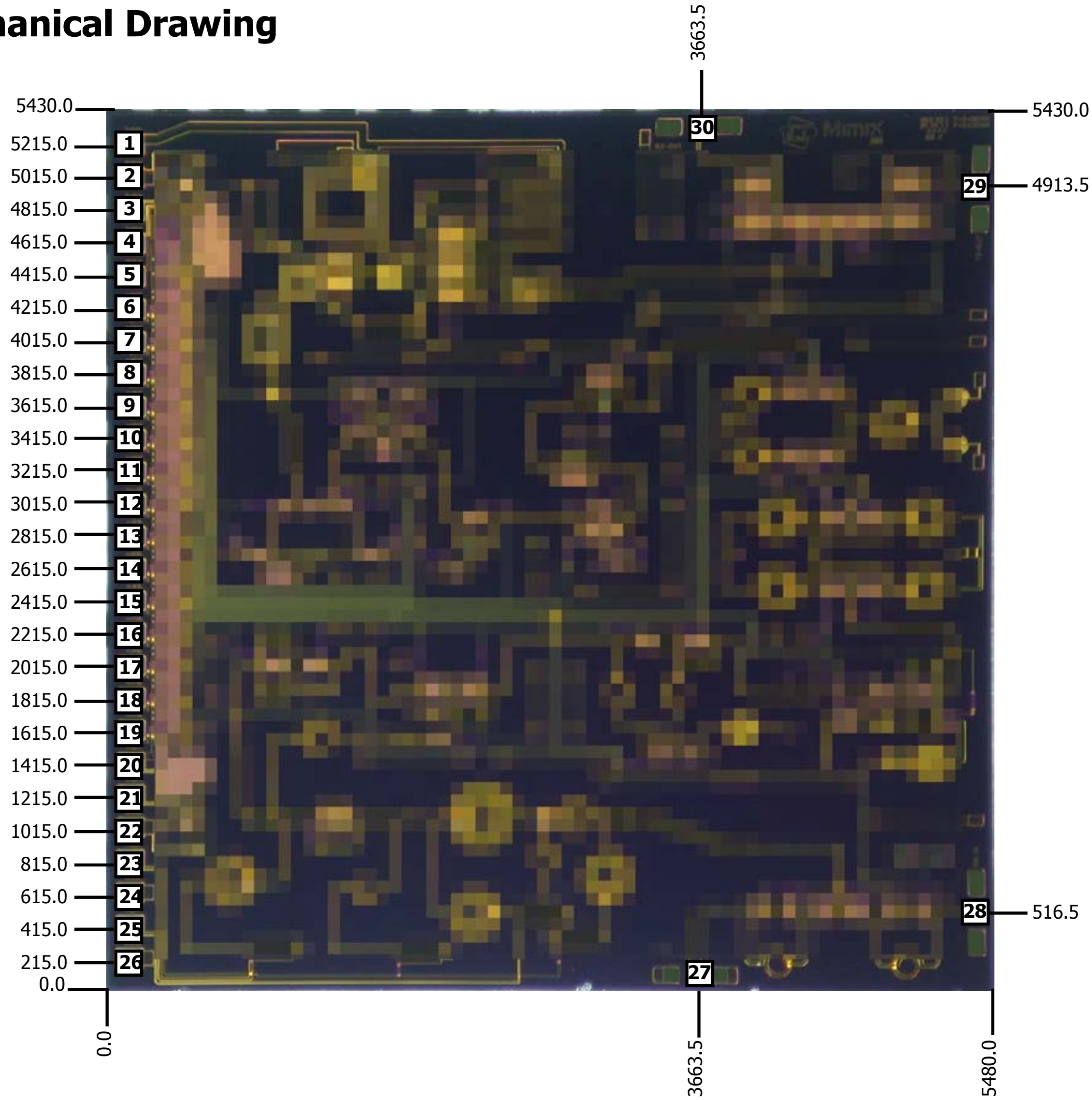
Mechanical Drawing



Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All Bond Pads are 0.100 x 0.100 (0.004 x 0.004).
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 12.4 mg.

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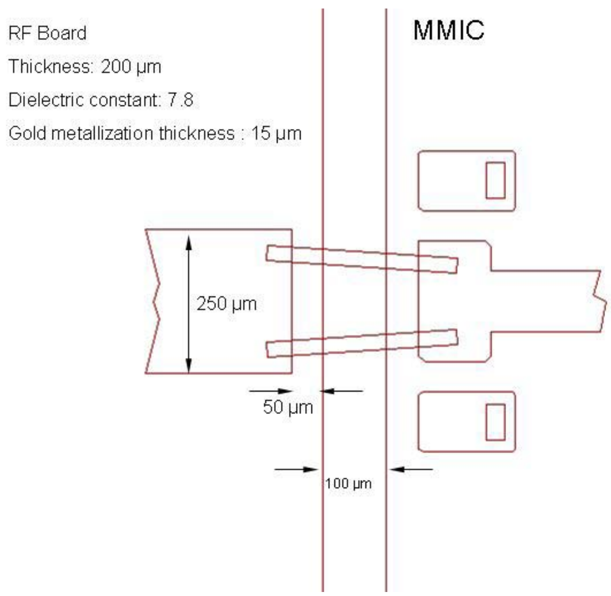
Bond Pad Designations

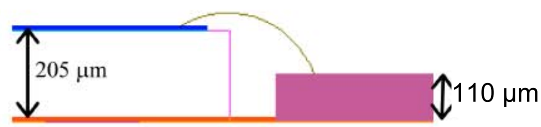
Pad #	Pad ID	Voltage [VDC]	Description
1	VD3	0.5 - 7V	Drain bias for MPA (stage 3) **see App note [5] for more details**
2	GND	-	Decoupling Ground
3	VG2		Monitor pad for stage 3 gate bias voltage
4	VS2	-10V	2nd Gate bias supply
5	GND	-	Decoupling Ground
6	I2S	0V - +3.3V	TX/RX Out switch
7	I6A	0 / +3.3	14.4 dB attenuation bit
8	I5A	0 / +3.3	7.2 dB attenuation bit
9	I4A	0 / +3.3	3.6 dB attenuation bit
10	I3A	0 / +3.3	1.8 dB attenuation bit
11	I2A	0 / +3.3	0.9 dB attenuation bit
12	I1A	0 / +3.3	0.45 dB attenuation bit
13	I6P	0 / +3.3	180º Phase bit
14	I5P	0 / +3.3	90º Phase bit
15	I4P	0 / +3.3	45º Phase bit

Pad #	Pad ID	Voltage [VDC]	Description
16	I3P	0 / +3.3	22.5º Phase bit
17	I2P	0 / +3.3	11.25º Phase bit
18	I1P	0 / +3.3	5.625º Phase bit
19	I1S	0V - +3.3V	TX/RX In switch
20	VS1	-10V	supply for LNA, 1st gate bias and digital
21	VG1		Monitor pad for stage 1 & 2 gate bias voltages
22	GND	-	Decoupling Ground
23	VD2	5V	Drain bias for LNA 2nd stage
24	GND	-	Decoupling Ground
25	VD1	5V	Drain bias for LNA 1st stage
26	GND	-	Decoupling Ground
27	TX-IN	RF	Transmit [TX] Input
28	RX-IN	RF	Receive [RX] Input
29	TX-OUT	RF	Transmit [TX] Output
30	RX-OUT	RF	Receive [RX] Output

App Note [1] Wire Bonding - Bond wires need to be as short as possible. The device is designed for a total bond wire inductance of 130 pH/RF bond pad. Different bond wire inductance will result in degraded performance See the diagram below for recommended bonding.

RF Transition Implementation





Loop height of RF bondings must be <200 um
Side-View

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App Note [2] Biasing - The core chip can be operated in either Transmit [TX] or Receive [RX] mode.

TX Mode - The TX mode is activated by setting the I1S and I2S switches, bond pads 6 and 19, to logic high (+3.3V).

RX Mode - To select the RX mode of operation the I1S and I2S switches, bond pads 6 and 19, are set to logic low (0V).

TX/RX Modes - For typical operation in either TX or RX mode, the gates (Vs 1,2) must be biased at -10V, the LNA/interstage amplifiers (Vd1,2) must be biased at 5V and the output power amplifier (MPA) must be set at +7V.

CAUTION! - Also, make sure to properly sequence the applied voltages to ensure negative gate bias (Vs 1,2) is available before applying the positive drain supply (Vd1,2,3).

App Note [3] Attenuator / Phase Shifter Control Bias - Logic buffering is integrated in the device to supply the necessary internal switching voltages. The reference state is enabled with logic "low" on all inputs, and the binary weighted phase (amplitude) states are switched by a logic "high" on the respective control input. Amplitude (phase) variation between phase (amplitude) states is minimized by optimization of internal matching and isolation between bits. Each bit is controlled using a '0' for the reference state and a '1' for the enabled state.

Atten Leve (dB)	I1A	I2A	I3A	I4A	I5A	I6A
0	0	0	0	0	0	0
0.45	1	0	0	0	0	0
0.9	0	1	0	0	0	0
1.8	0	0	1	0	0	0
3.6	0	0	0	1	0	0
7.2	0	0	0	0	1	0
14.4	0	0	0	0	0	1
-	-	-	-	-	-	-
28.35	1	1	1	1	1	1

Phase Shift (degrees)	I1P	I2P	I3P	I4P	I5P	I6P
0°	0	0	0	0	0	0
5.625°	1	0	0	0	0	0
11.25°	0	1	0	0	0	0
22.5°	0	0	1	0	0	0
45°	0	0	0	1	0	0
90°	0	0	0	0	1	0
180°	0	0	0	0	0	1
354.375°	1	1	1	1	1	1

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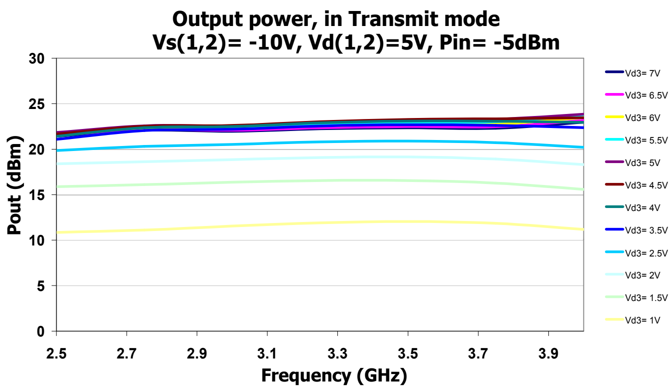
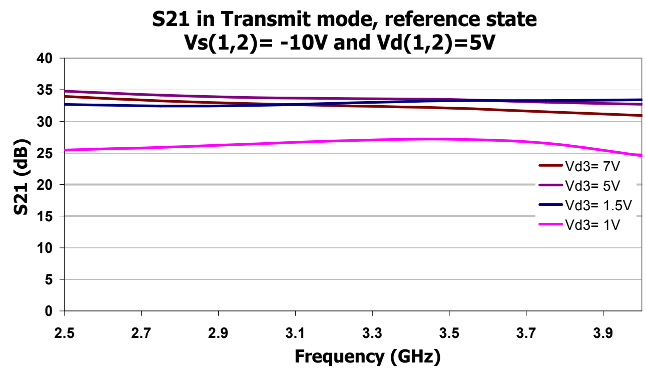
App Note [4] Bias Arrangement - Each DC Bias pad (Vd1,2,3) needs to have DC bypass capacitance (80-120 pF) as close to the device as possible. Additional DC bypass capacitance (10 nF) is also recommended.

App note [5] – The Pout and S21 of the XZ1001-BD can be adjusted depending on the biasing level of Vd3. The Pout of the XZ1001-BD is 22 dBm* and the S21 is 33 dB* when Vd3 is biased at 7V. The Pout and S21 can be reduced with lower biasing of Vd3 as illustrated in the plots below. This feature offers flexibility for the XZ1001-BD to suit applications with lower Pout and S21 specifications.

*There is a plan to increase the Pout to 30 dBm and S21 to 40 dB in a future release of the XZ1001-BD.





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Handling and Assembly Information

CAUTION! - M/A-COM Tech Asia MMIC Products contain gallium arsenide (GaAs) which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- Do not ingest.
- Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.
- Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.

Life Support Policy - M/A-COM Tech Asia's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President and General Counsel of M/A-COM Tech Asia. As used herein: (1) Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. (2) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ESD - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static containers, which should be opened in cleanroom conditions at an appropriately grounded antistatic workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

Die Attachment - GaAs Products from M/A-COM Tech Asia are 0.100 mm (0.004") thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the M/A-COM Tech Asia "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001^2 thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280º C (Note: Gold Germanium should be avoided). The work station temperature should be 310ºC +/- 10º C. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

Ordering Information

Part Number for Ordering	Description
XZ1001-BD-000V	RoHS compliant die packed in vacuum release gel paks
XZ1001-BD-EV1	XZ1001-BD Evaluation Module

Caution: ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling this device.

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