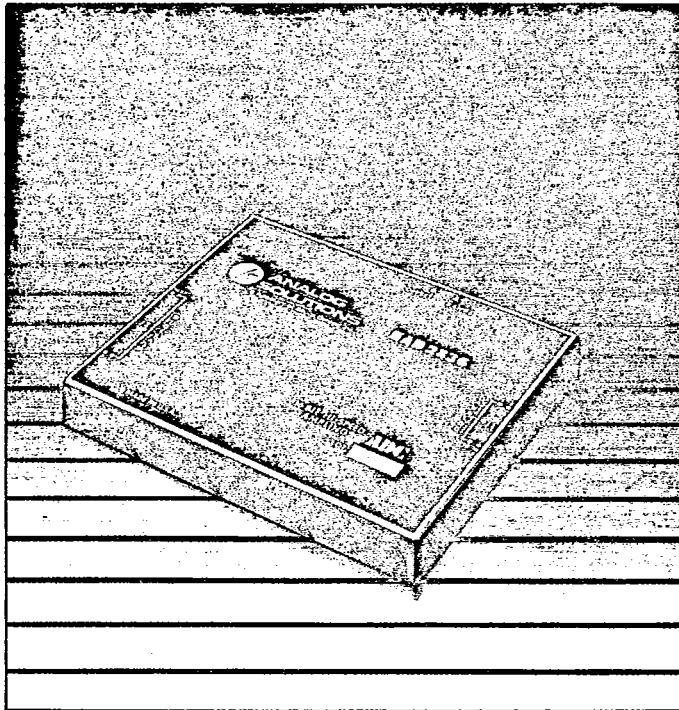




**ANALOG
SOLUTIONS™**
a subsidiary of Silicon General, Inc.

ZAD2836

16-Bit High-Speed Sampling
A/D Converter



Applications

- Medical Imaging Data Acquisition
- High-Speed Automatic Test
- Wide Dynamic Range Scientific Instrumentation
- Professional Audio
- Multiplexed Data Acquisition

Key Features

- 3.5 μ s A/D Conversion Time
- 200 kHz Total Throughput
- Superior Linearity Throughout Signal Range
- Built-In Ultra-Linear Sample/Hold
- Sample/Hold Dielectric Absorption < 0.001%
- Aperture Uncertainty < 50 ps.
- Dynamic Gain and Offset Correction Capabilities
- Tri-State Output Latches

Solutions for Data Conversion

Offering a five microsecond total throughput time and improved linearity and drift, the ZAD2836 sets the performance standard for 16-bit sampling A/D converters. Utilizing the latest IC technology and advanced Analog Solutions' proprietary circuit designs, the ZAD2836 provides significantly enhanced performance at a cost less than many older, slower designs.

The ZAD2836 is the solution to your high-speed 16-bit conversion needs.

General Description

The ZAD2836 is a high-performance, five microsecond, 16-bit sampling ADC which includes an ultra-linear Sample/Hold and high-speed A/D converter in one compact, fully tested module. The ZAD2836 has been optimized for performance in critical CT and MRI systems, where the dynamic range, accuracy around zero and repeatability are all critical.

Utilizing an advanced Digitally Corrected Sub-Ranging (DCSR) A/D converter approach and a novel Sample/Hold circuit, the ZAD2836 assures 16-bit total performance.

The ZAD2836's excellent long-term drift and temperature stability are accomplished by using specially selected and tested resistor networks in a proprietary DCSR circuit design that reduces the converter's sensitivity to individual component drift.

Description of Converter

The ZAD2836 utilizes a unique three-pass Digitally Corrected Sub-Ranging (DCSR) technique in conjunction with our proven "monobit" D/A converter architecture to provide premium converter performance.

The unit consists of an ultra-linear Sample/Hold, a 6-bit flash to ensure long-term accuracy, and our monobit DAC for reduced sensitivity to resistor drift.

The combination of the three-pass DCSR technique and monobit design DAC provides up to four times more allowance for component variation and drift than older two-pass sub-ranging converters.

This conservative design approach assures that the unit stays within specification over its full temperature range and that long-term drift is minimized.

PERFORMANCE SPECIFICATIONS

ZAD2836 LOW-DISTORTION 16-BIT SAMPLING A/D CONVERTER

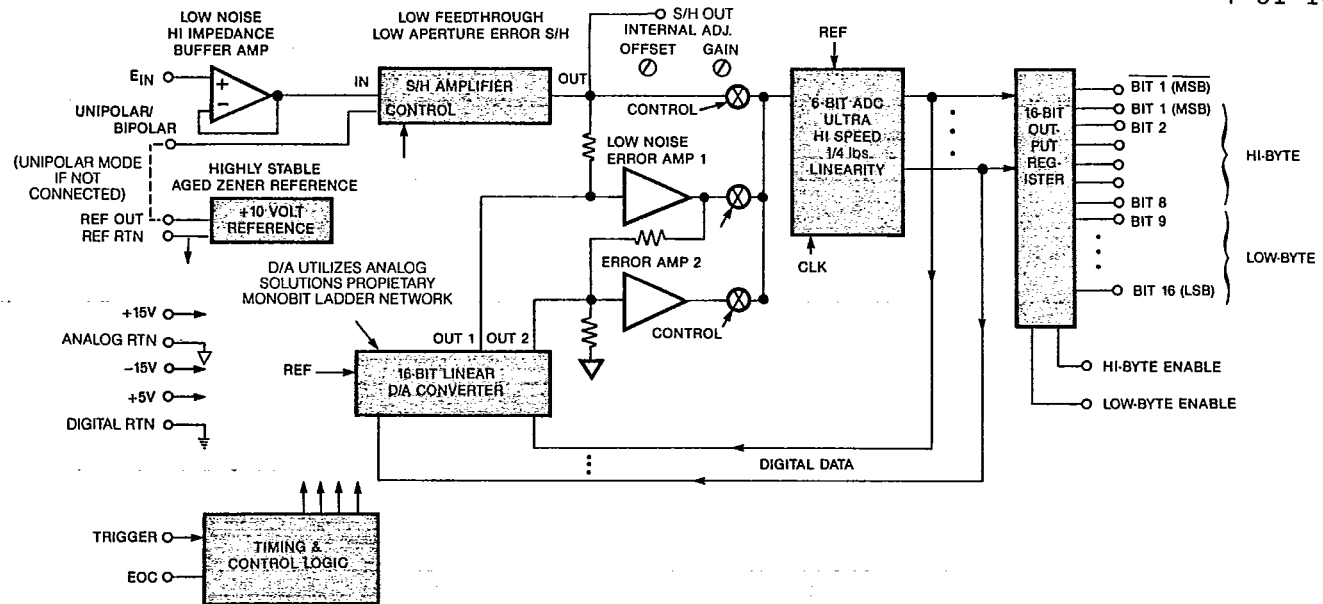
	UNIPOLAR	BIPOLAR		UNIPOLAR	BIPOLAR
ANALOG INPUT			HOLD MODE		
Voltage Range	0 to +10 V	±5 V	Droop Rate	5 $\mu\text{V}/\mu\text{s}$ max (typically doubles every 10°C)	*
Input Impedance	100 M Ω /5 pF typical	*	Dielectric Absorption	±0.001% of input signal voltage change, typical	*
Input Bias Current	±2 nA max (+10°C to +60°C)	*	S/H Feedthrough	-96 dB typical, -90 dB max	*
Initial Offset Voltage	±5mV max ³	*	SAMPLE MODE		
Stability of Offset Voltage	±100 $\mu\text{V}/72$ hrs typical	*	Slew Rate	20 V/ μs min	*
ACCURACY			Bandwidth	5 MHz typical, 2 MHz min	*
Resolution	16 bits	*	Acquisition Time	1.5 μs typical	*
Quantization Error	±0.5 LSB	*	DIGITAL INPUTS/OUTPUTS		
Relative Accuracy ¹	±0.003% FSR, max	*	Logic Levels	LSTTL/CMOS compatible	*
FSR Factory-Calibrated to	±0.01% ³	*	Data Outputs	16 bits data; Tri-state latch, 10 LS loads	*
Absolute Accuracy	±0.003% FSR max ²	*	Trigger Input	Negative edge; 1 μs pulse width min., 3 μs max. (see timing diagram)	*
Differential Non-Linearity	±0.5 LSB typical, ±0.75 LSB max	*	Trigger Load	1 LSTTL load ⁵	*
Reference Output	+10.000 V ±20 mV, load = 2 mA max	* ⁴	Tri-State Control	Logic 1 on HI BYTE EN or LO BYTE EN generates HI impedance state	*
Noise			End of Conversion (EOC)	Data valid on EOC high to low transition	*
Unipolar	40 μV RMS max	*	POWER REQUIREMENTS		
Bipolar	50 μV RMS max	*	+15 V ±0.25 V	65 mA typical	*
Missing Codes	No missing codes 10° to 50°C	*	-15 V ±0.25 V	85 mA typical	*
Harmonic Distortion (±5 V input, 10 kHz)		-90 dB, typical	+ 5 V ±0.25 V	100 mA typical	*
STABILITY			ENVIRONMENTAL & MECHANICAL		
Differential Non-Linearity Temperature Coefficient	±0.5 ppm/°C max	*	Operating Temperature Range	+10°C to +60°C	*
Offset Temperature Coefficient	±20 $\mu\text{V}/^\circ\text{C}$ typical, ±40 $\mu\text{V}/^\circ\text{C}$ max	*	Storage Temperature Range	-10°C to +75°C	*
Offset Versus Supply	100 $\mu\text{V}/1\%$ change in supply, max	*	Relative Humidity	0 to 85%, non-condensing up to 40°C	*
Gain Temperature Coefficient	±2 ppm/°C typical ±5 ppm/°C max	*	Shielding	RFI 6 sides, EMI 5 sides	*
Warm-up Time	15 minutes to specified accuracy	*	MATING CONNECTOR		
THROUGHPUT			J1: Amp 103183-7 or equiv. (analog, 16 pin)	*	
Throughput Time (ADC and S/H)	5.0 μs max (200 kHz throughput)	*	J2: Amp 1-103183-2 or equiv. (digital, 28 pin)	*	
A/D Conversion Time	3.5 μsec , typical	*	PACKAGE SIZE*		
SAMPLE-TO-HOLD SWITCHING			3.8 in. (96.5mm) × 4.5 in. (114.3mm) × 0.562 in. (14.3mm) max. pkg. height		
Aperture Delay	15 ns typical	*			
Aperture Uncertainty	±50 ps typical ±100 ps max	*			

(Specifications apply @ 25°C unless otherwise noted)

* Same as Unipolar

NOTE:

1. Worst case summation of S/H and A/D non-linearity errors. Best fit straight-line.
2. After OFFSET/GAIN adjustment.
3. Internal (or external customer installed) pots allow field calibration.
4. Shaded areas denotes enhanced performance.
5. External 10 k Ω pull-up required.
6. Consult factory for mounting dimensions.
7. ZAD2846 is recommended for ultra low distortion applications.



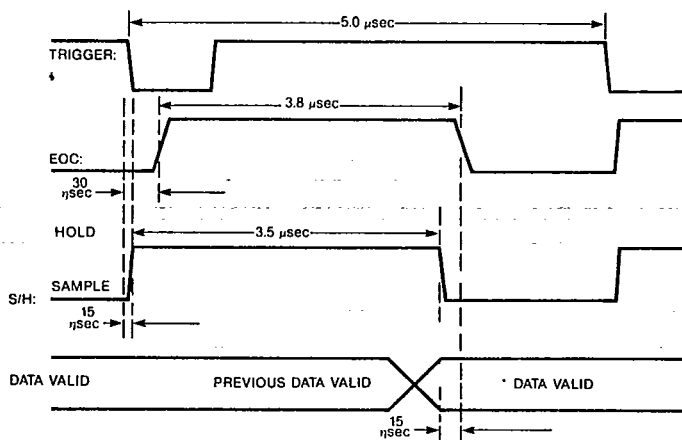
ZAD2836 Three-Pass Digitally Corrected Sub-Ranging (DCSR) Architecture

Sample/Hold Characteristics:

The Sample/Hold is one of the most critical and difficult portions of any data acquisition system.

Through careful design, utilizing unique circuitry, the Sample/Hold section of the ZAD2836 provides true 16-bit linearity, dielectric absorption of 0.001% (< 1 LSB) necessary for accurately acquiring wide dynamic range inputs, and 1.5 microseconds total acquisition and settling time.

The ZAD2836's Sample/Hold is truly leading the state-of-the-art.

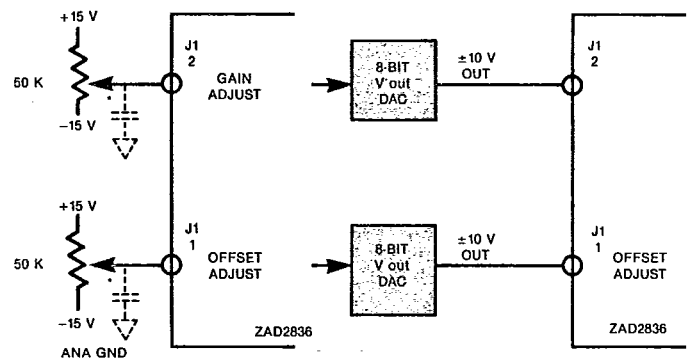


Timing Diagram

Dynamic Adjustment of Gain and Offset:

In addition to internal gain and offset adjustment, provision has been made for the addition of external adjustments. By utilizing these pins and external voltage output D/A's, the gain and offset of the A/D can be dynamically adjusted by the host computer or micro-computer. The available adjustment range for the

ZAD2836 has been increased beyond that normally required to enable this dynamic adjustment to handle typical system gain and offset errors.



CONVENTIONAL ADJUSTMENT * OPTIONAL .01 μ F CERAMIC IF POT IS MORE THAN 2" FROM PIN. DYNAMIC ADJUSTMENT GAIN ADJ RANGE: ± 300 ppm of FSR. OFFSET ADJ RANGE: ± 5 mV.

External Offset and Gain Adjustment

This provides the system designer with the capability to dynamically correct system errors, which results in increased accuracy, system stability and reduced long-term drift.

PC Board Layout

The analog input lead lengths should be as short as possible, preferably surrounded on both sides by an analog ground plane. The module has been carefully laid out internally to separate the analog input from the digital output. This practice should be extended to the PC board as much as possible. All digital control signals should also be kept away from the analog input.

Separate ground planes for analog and digital circuits associated with the ZAD2836 are extremely important. Of equal importance is the use of completely

separate analog and digital ground returns to their respective power supplies. No interconnection of these two returns should occur anywhere in the system except for that which is located within the ZAD2836. In addition, the use of the ANALOG RETURN PIN as an analog ground mecca is recommended. All of these precautions are suggested in order to minimize the effects of ground loops and to eliminate the possibility of digital noise coupling into the analog circuitry.

Power Supplies

In order to take advantage of the full 16-bit accuracy of the ZAD2836, it is recommended that well-regulated linear power supplies be used for the ±15V required by the ZAD2836.

Output Coding

Unipolar Binary	Offset Binary	MSB	LSB
+ 9.99985 V	+ 4.99985 V	11.....11	
+ 5.00000 V	+ 0.00000 V	10.....00	
+ 0.00000 V	- 5.00000 V	00.....00	

Note: For 2's complement coding use the MSB in place of the MSB output.

Input range selection:

Range	Connect
0 to +10 Volts	signal input is PIN 15, GND PIN 9
± 5 Volts	PIN 10 to PIN 9, signal input is PIN 15

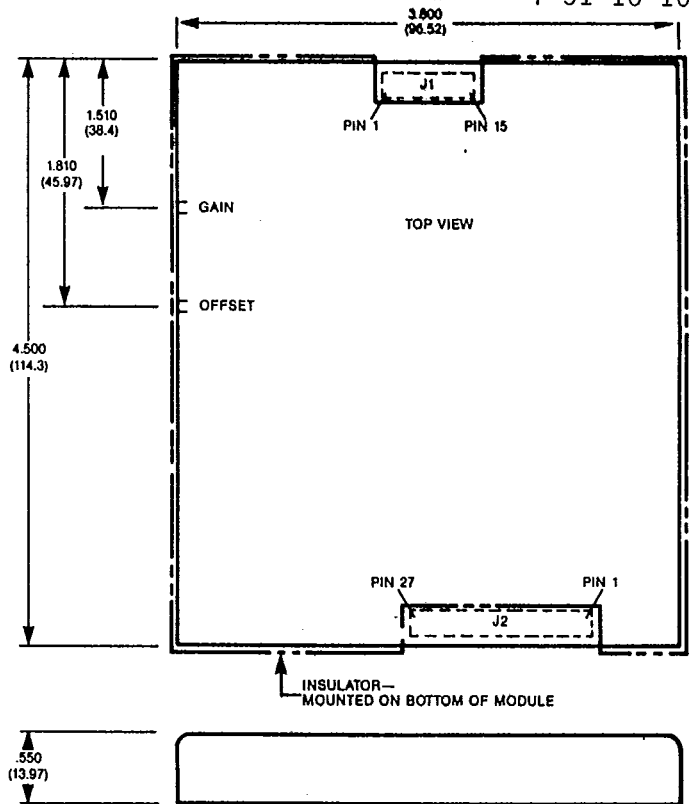
Additional Products from Analog Solutions

- Precision A/D and D/A Converters
- Precision 16-bit and 18-bit D/A Converters
- High-Performance Sample/Hold Amplifiers
- Logarithmic, Isolation and Special-Purpose Amplifiers
- High-Speed Telecommunications A/D and D/A Systems
- Precision Load Cell and Strain-Gage Sub-Systems
- High Speed Industrial Control Interfaces

Custom Products

We invite customers to take full advantage of our custom design capability to provide the optimum product solution. Please contact our sales department for further information.

Ordering Guide
 To Order Specify:
 ZAD2836 16-Bit High-Speed Sampling A/D Converter
 To place your order, contact Analog Solutions at (408) 433-1900



NUMBERS IN PARENTHESIS ARE IN MM

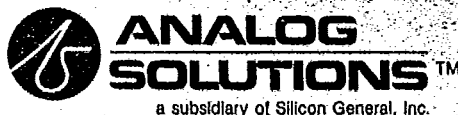
Physical Outline

J1 Pin Assignments

- | | |
|---------------|--------------|
| 1. OFFSET ADJ | 9. BIPOLAR |
| 2. GAIN ADJ. | 10. REF. OUT |
| 3. -15 V | 11. S/H OUT |
| 4. -15V | 12. REF. RTN |
| 5. ANALOG RTN | 13. SIG. RTN |
| 6. ANALOG RTN | 14. SIG. RTN |
| 7. +15 V | 15. SIG. IN |
| 8. +15 V | 16. SIG. RTN |

J2 Pin Assignments

- | | |
|-----------------|---------------------|
| 1. TRIGGER | 19. LO BYTE ENABLE* |
| 2. EOC | 20. HI BYTE ENABLE* |
| 3. N/C | 21. BIT 7 |
| 4. N/C | 22. BIT 8 |
| 5. +5 V | 23. BIT 5 |
| 6. +5 V | 24. BIT 6 |
| 7. DIGITAL RTN | 25. BIT 3 |
| 8. DIGITAL RTN | 26. BIT 4 |
| 9. BIT 1 | 27. BIT 1 MSB |
| 10. DIGITAL RTN | 28. BIT 2 |
| 11. BIT 15 | |
| 12. BIT 16 LSB | |
| 13. BIT 13 | |
| 14. BIT 14 | |
| 15. BIT 11 | |
| 16. BIT 12 | |
| 17. BIT 9 | |
| 18. BIT 10 | |
- N/C: Do Not Connect.
 SIG RTN, Analog RTN and Digital RTN Internally Connected
 * Open = Enabled



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