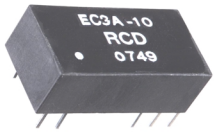
PROGRAMMABLE ECL DELAY LINES

RESISTORS•CAPACITORS•COILS•DELAY LINES

EC3A 3 BIT 10K ECL LOGIC
EC3H 3 BIT 10KH ECL LOGIC

Term.W is RoHS compliant

- ❒ Incremental delays of 0.5nS to 10nS
- ❒ Choice of 16-pin DIP or SM package

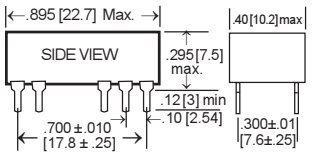


10K ECL RCD P/N	10KH ECL RCD P/N	Incremental Delay per Step (nS)	Error (Ref to "000")	Referenced to "000" - Delay in nS per Program Setting (P3*P2*P1)							
				000	001	010	011	100	101	110	111
EC3A-0.5	EC3H-0.5	0.5 ± .25	± .30	0*	0.5	1.0	1.5	2.0	2.5	3.0	3.5
EC3A-0.75	EC3H-0.75	0.75 ± .3	± .50	0*	0.75	1.5	2.25	3.0	3.75	4.5	5.25
EC3A-1	EC3H-1	1.0 ± .4	± .50	0*	1.0	2.0	3.0	4.0	5.0	6.0	7.0
EC3A-1.25	EC3H-1.25	1.25 ± .5	± .70	0*	1.25	2.5	3.75	5.0	6.25	7.5	8.75
EC3A-1.5	EC3H-1.5	1.5 ± .5	± .70	0*	1.5	3.0	4.5	6.0	7.5	9.0	10.5
EC3A-2	EC3H-12	2.0 ± .7	± .80	0*	2.0	4.0	6.0	8.0	10	12	14
EC3A-2.5	EC3H-2.5	2.5 ± .7	± .90	0*	2.5	5.0	7.5	10	12.5	15	17.5
EC3A-3	EC3H-3	3.0 ± .7	± 1.0	0*	3.0	6.0	9.0	12	15	18	21
EC3A-5	EC3H-5	5.0 ± 1	± 1.5	0*	5.0	10	15	20	25	30	35
EC3A-10	EC3H-10	10 ± 1.5	±3.0	0*	10	20	30	40	50	60	70

* Inherent delay of EC3A 10K ECL is 3 ± 0.5nS and inherent delay of EC3H 10KH ECL is 1.5 ± 0.5nS. The initial delay and cumulative tolerances is referenced to setting "000." For example, the setting "111" delay of EC3A-1 is 7.0 ± 0.5 nS ref. to "000," and 10.0 ± 1.0 ns referenced to the input. The setting "111" delay of EC3H-1 is 7.0 ± 0.5 nS ref. to "000," and 8.5 ± 1.0 ns referenced to the input.

EC3A 10K ECL OPERATING SPECIFICATIONS

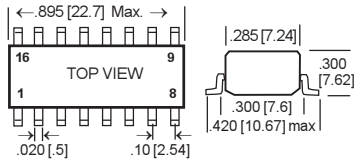
V_{EE} Supply Voltage: -5.20 ± 0.25VDC
I_{EE} Supply Current: 60 mA typical
Logic "1" Input: V_{IH}= -.98V min., I_{IH}= 265µA max, I_{IH} (pin 6*)= -11mA typ.
Logic "0" Input: V_{IL}= -1.63V max, I_{IL}= 0.5µA min., I_{IL} (Pin 6*)= -2mA typ.
V_{OH} Logic "1" Voltage Out: -.96V min.
V_{OL} Logic "0" Voltage Out: -1.65V max.
Input Pulse Width: 40% of max. delay min.
Operating Temp. Range: -30 to +85°C
Storage Temperature Range: -65 to +150°C



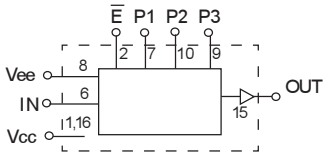
Type EC3A & EC3H (16-pin DIP)

EC3H 10KH ECL OPERATING SPECIFICATIONS

V_{EE} Supply Voltage: -5.20 ± 0.25VDC
I_{EE} Supply Current: 75 mA typical
Logic "1" Input: V_{IH}= -.98V min., I_{IH}= 320µA max, I_{IH} (pin 6*)= -11mA typ.
Logic "0" Input: V_{IL}= -1.63V max, I_{IL}= 0.7µA min., I_{IL} (Pin 6*)= -2mA typ.
V_{OH} Logic "1" Voltage Out: -.96V min.
V_{OL} Logic "0" Voltage Out: -1.65V max.
Input Pulse Width: 40% of max. delay min.
Operating Temp. Range: -30 to +85°C
Storage Temperature Range: -65 to +150°C



Type EC3AG & EC3HG (16-pin SMD *)
* Info on SM package is preliminary



CIRCUIT SCHEMATIC: ENABLE input E (pin #2) is active low. Output is disabled (low) when pin #2 is logic high.

*** INPUT LOADING AT PIN #6**: internally connected to eight ECL gate inputs terminated by Thevenin equivalent of 100 Ohms to -2V.

P/N DESIGNATION: EC3A AG ☐ - 10 - B W

RCD Type: EC3A, EC3H
Surface Mount Option: G (leave blank if standard thru-hole DIP)
Options: assigned by RCD (leave blank if std.)
Delay Time (incremental delay per step)
Packaging: B=Bulk (magazine tube std)
Termination: W=Lead-free, Q=Tin/Lead (leave blank if either is acceptable)

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