

BIPOLAR ANALOG INTEGRATED CIRCUIT

μ PC1853

MATRIX SURROUND IC WITH I²C BUS

The μ PC1853 is a phase shift matrix surround IC. Only 2 speakers on the front side implement wide sound expansion, and by adding rear speakers, rich three-dimensional sound can be obtained.

The μ PC1853 can perform all controls (mode switching, volume control and so on) through the I²C bus.

FEATURES

- Any control is possible through the I²C bus.
- Surround effect can be realized by only 2 speakers on the front side.
- On-chip tone (bass and treble) control circuit.
- Level-adjustable output pin for heavy bass sound.
- Level-adjustable output pin for AV amplifier.
- μ PC1853-01 : On-chip low boost circuit.
On-chip volume and balance control circuits.
- μ PC1853-02 : On-chip L-channel volume and R-channel volume control circuits.

APPLICATION

- TV, audio

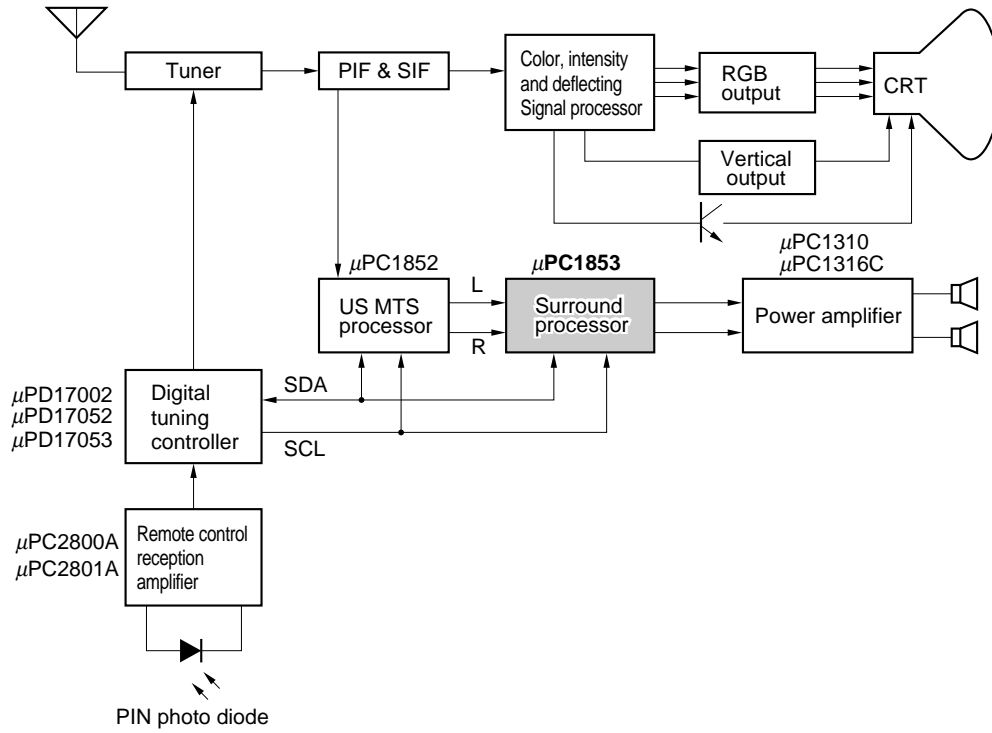
ORDERING INFORMATION

Part Number	Package
μ PC1853CT-01	30-pin plastic shrink DIP (400 mil)
μ PC1853CT-02	"

The information in this document is subject to change without notice.

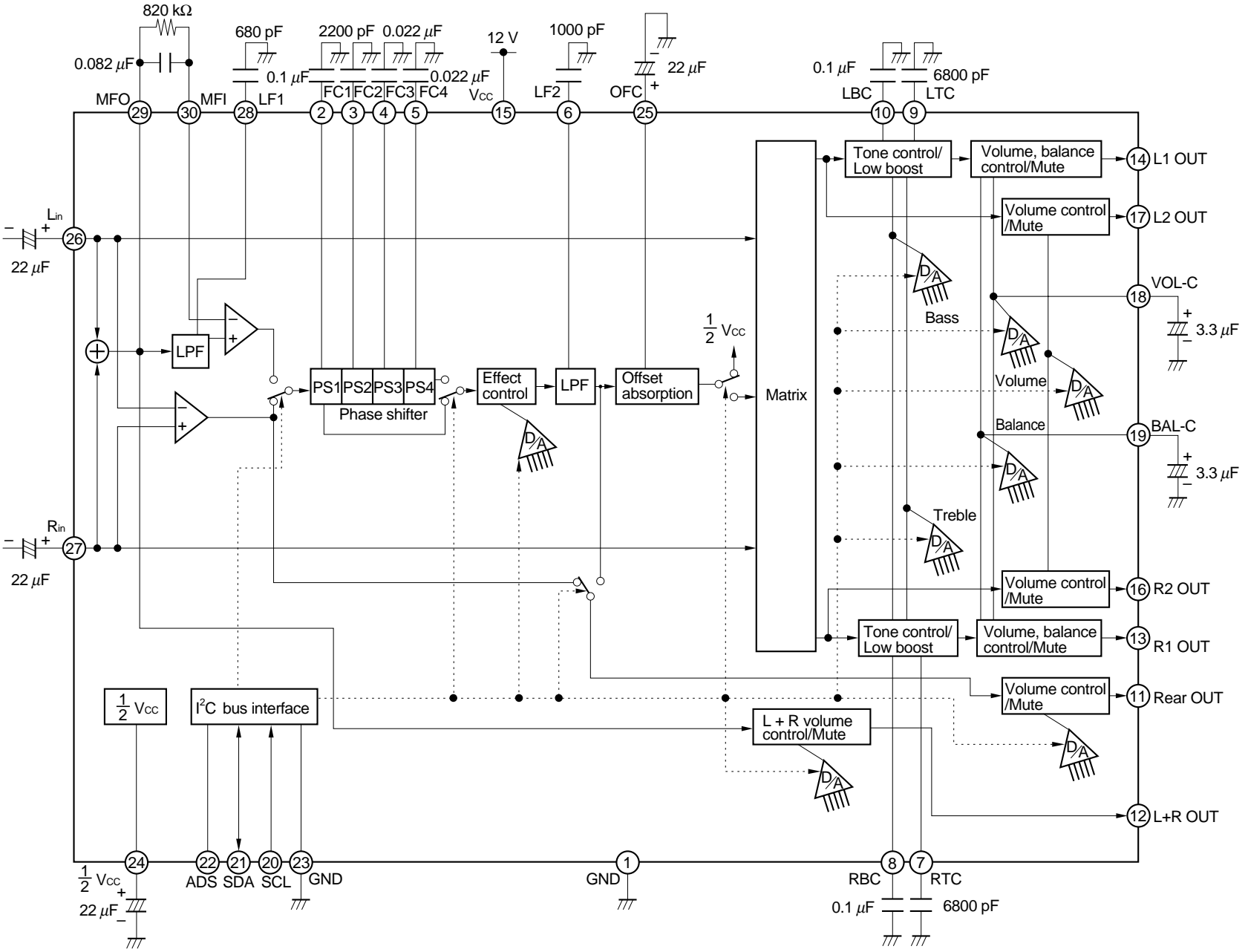
SYSTEM BLOCK DIAGRAM

- TV

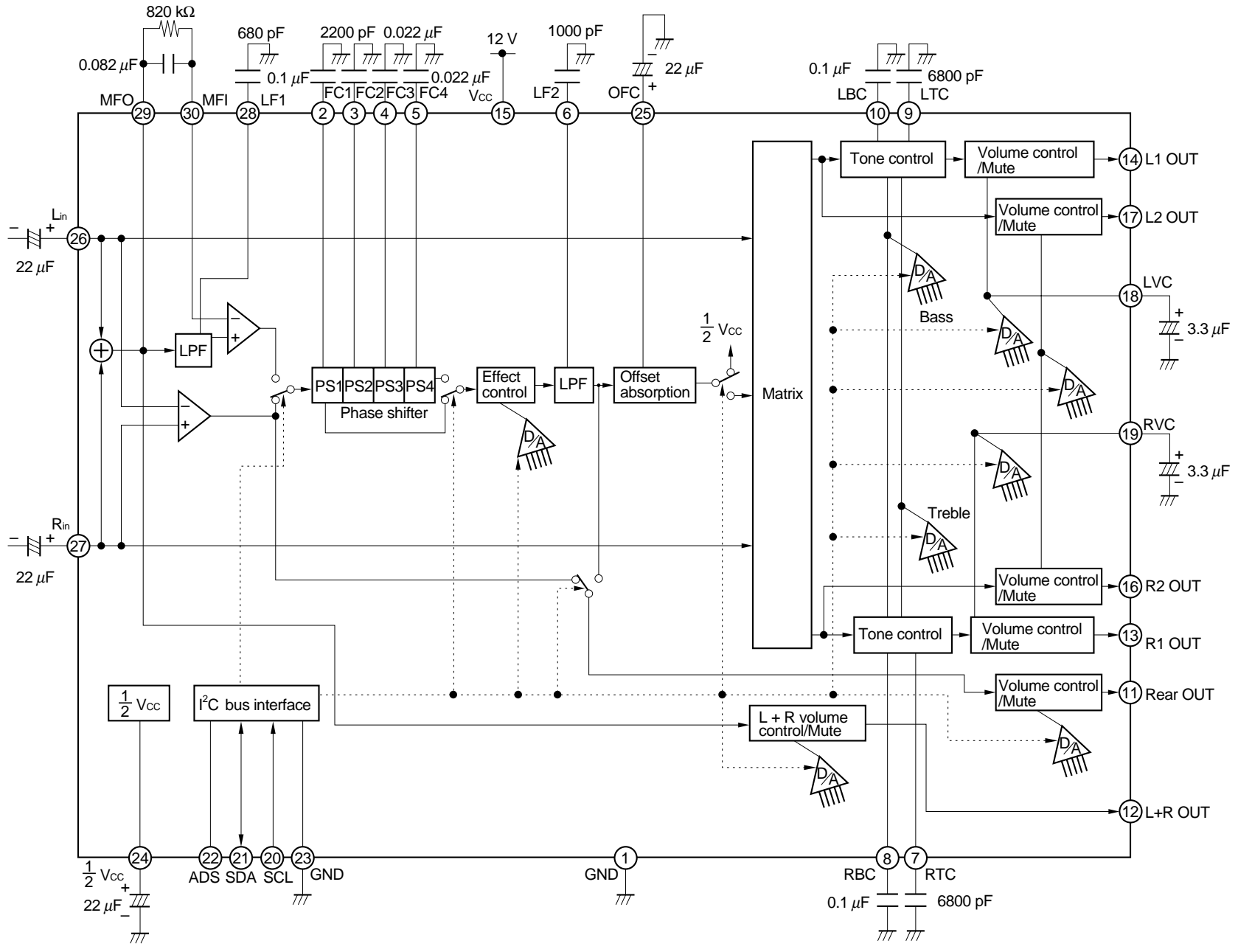


BLOCK DIAGRAM

(1) μPC1853-01

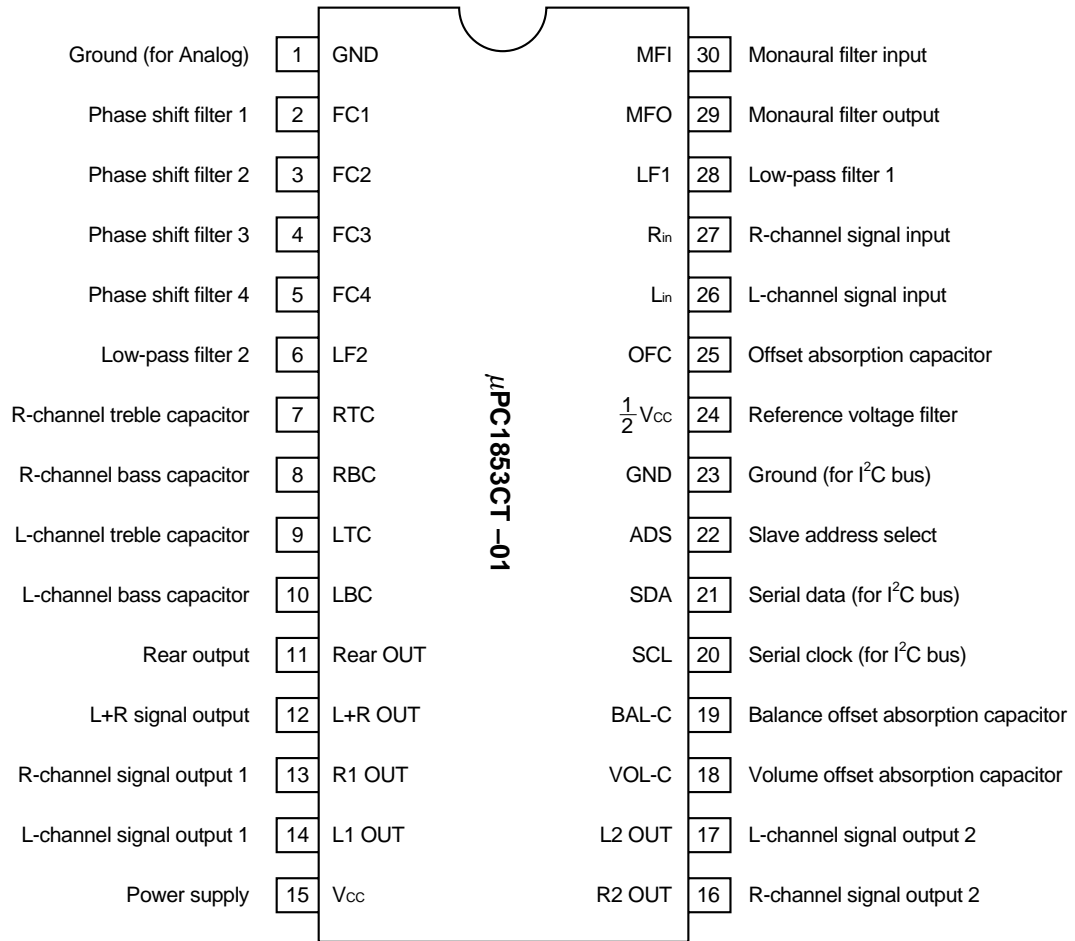


(2) μPC1853-02

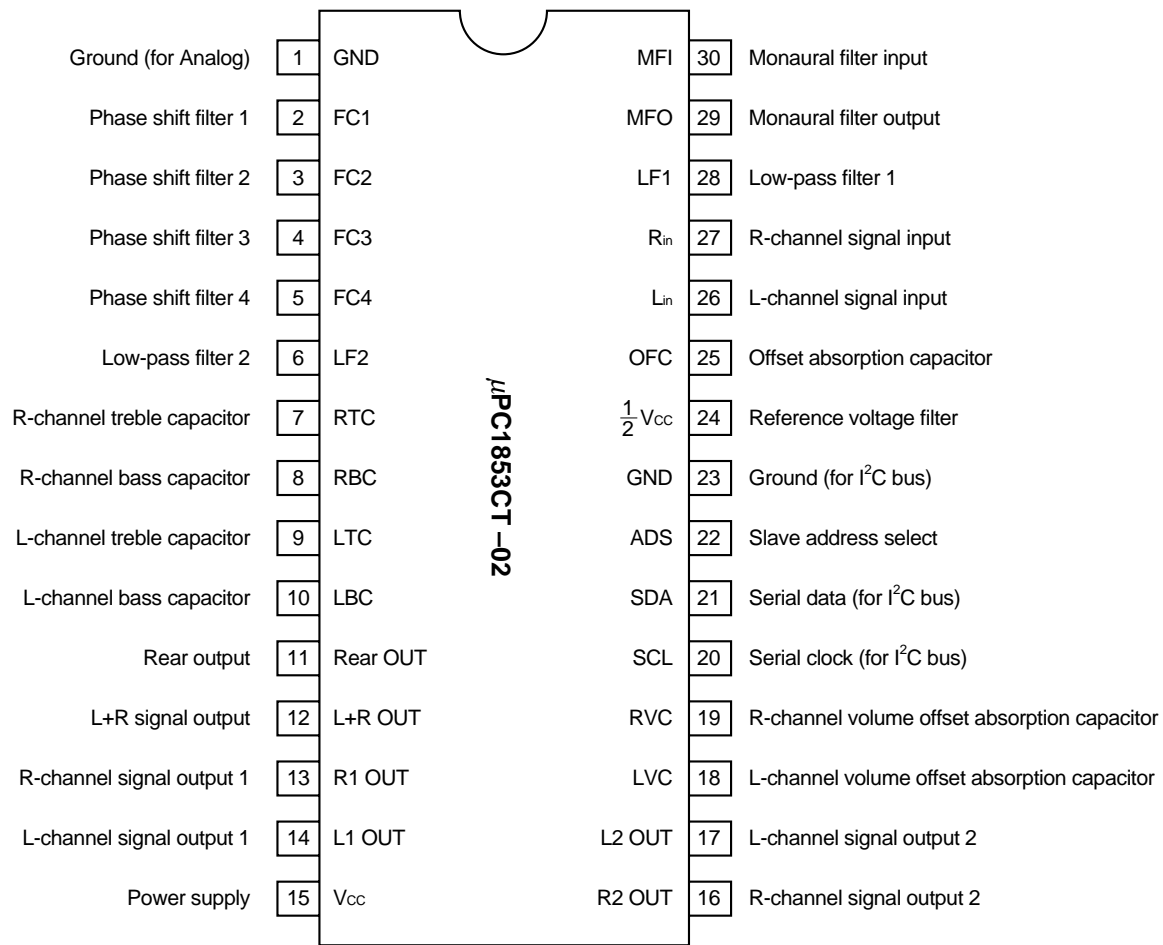


PIN CONFIGURATION (Top View)

(1) μPC1853-01



(2) μPC1853-02



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1. EXPLANATION OF PINS

Table 1-1 Explanation of Pins (1/8)

Pin Number	Pin Name	Equivalent Circuit	Description
1	GND		<p>Ground for analog signal. Pin voltage: approx. 0.0 V</p>
2	FC1		<p>Capacitor connection pin which determines time constant of phase shifter. Pin voltage: approx. 6.0 V</p>
3	FC2		
4	FC3		

Table 1-1 Explanation of Pins (2/8)

Pin Number	Pin Name	Equivalent Circuit	Description
5	FC4		<p>Capacitor connection pin which determines time constant of phase shifter.</p> <p>Pin voltage: approx. 6.0 V</p>
6	LF2		<p>Low-pass filter.</p> <p>Pin voltage: approx. 6.0 V</p>
7	RTC		<p>Capacitor connection pin for treble boost/cut frequency characteristic of R-channel signal.</p> <p>Pin voltage: approx. 6.0 V</p>
8	RBC		<p>Capacitor connection pin for bass boost/cut frequency characteristic of R-channel signal.</p> <p>Pin voltage: approx. 6.0 V</p>

Table 1-1 Explanation of Pins (3/8)

Pin Number	Pin Name	Equivalent Circuit	Description
9	LTC		<p>Capacitor connection pin for treble boost/cut frequency characteristic of L-channel signal.</p> <p>Pin voltage: approx. 6.0 V</p>
10	LBC		<p>Capacitor connection pin for bass boost/cut frequency characteristic of L-channel signal.</p> <p>Pin voltage: approx. 6.0 V</p>
11	Rear OUT		<p>L-R signal output pin. Select the output signal (ϕ(L-R) signal or (L-R) signal) (see 4.4.1(4) or 4.4.2(2) Rear output selection).</p> <ul style="list-style-type: none"> ϕ(L-R): Phase-shifted. (L-R) : Not phase-shifted. <p>Pin voltage: approx. 6.0 V</p>
12	L+R OUT		<p>L+R signal output pin.</p> <p>Pin voltage: approx. 6.0 V</p>

Table 1-1 Explanation of Pins (4/8)

Pin Number	Pin Name	Equivalent Circuit	Description
13	R1 OUT		<p>R-channel signal output pin (for main output). Pin voltage: approx. 6.0 V</p>
14	L1 OUT		<p>L-channel signal output pin (for main output). Pin voltage: approx. 6.0 V</p>
15	Vcc		<p>Supply voltage. Pin voltage: approx. 12.0 V</p>
16	R2 OUT		<p>R-channel signal output pin for external audio processor and so on. Pin voltage: approx. 6.0 V</p>

Table 1-1 Explanation of Pins (5/8)

Pin Number	Pin Name	Equivalent Circuit	Description
17	L2 OUT		<p>L-channel signal output pin for external audio processor and so on. Pin voltage: approx. 6.0 V</p>
18	VOL-C (μPC1853-01)		<p>Capacitor connection pin which absorbs shock noise of D/A converter for volume control. Pin voltage: approx. 6.0 V</p>
	LVC (μPC1853-02)		<p>Capacitor connection pin which absorbs shock noise of D/A converter for L-channel volume control. Pin voltage: approx. 6.0 V</p>
19	BAL-C (μPC1853-01)		<p>Capacitor connection pin which absorbs shock noise of D/A converter for balance control. Pin voltage: approx. 4.8 V</p>
	RVC (μPC1853-02)		<p>Capacitor connection pin which absorbs shock noise of D/A converter for R-channel volume control. Pin voltage: approx. 4.8 V</p>
20	SCL		<p>Serial clock line pin (clock input for I²C bus). Pin voltage: approx. 0.0 V</p>

Table 1-1 Explanation of Pins (6/8)

Pin Number	Pin Name	Equivalent Circuit	Description
21	SDA		<p>Serial data line pin (data input for I²C bus).</p> <p>Pin voltage: approx. 0.0 V</p>
22	ADS		<p>Slave address selection pin.</p> <p>Pin voltage: approx. 0.0 V</p>
23	DGND		<p>Ground for I²C bus signal.</p> <p>Pin voltage: approx. 0.0 V</p>
24	$\frac{1}{2} V_{cc}$		<p>Filter pin for middle point of supply voltage.</p> <p>Pin voltage: approx. 6.0 V</p>

Table 1-1 Explanation of Pins (7/8)

Pin Number	Pin Name	Equivalent Circuit	Description
25	OFC		<p>Capacitor connection pin which absorbs offset voltage generated by phase shifter.</p> <p>Pin voltage: approx. 6.0 V</p>
26	Lin	<p>L-channel signal input</p>	<p>L-channel signal input pin.</p> <p>Input impedance: 60 kΩ</p> <p>Pin voltage: approx. 6.0 V</p>
27	Rin	<p>R-channel signal input</p>	<p>R-channel signal input pin.</p> <p>Input impedance: 60 kΩ</p> <p>Pin voltage: approx. 6.0 V</p>
28	LF1		<p>Low-pass filter.</p> <p>Pin voltage: approx. 6.0 V</p>

Table 1-1 Explanation of Pins (8/8)

Pin Number	Pin Name	Equivalent Circuit	Description
29	MFO		High-pass filter output pin for surround function (Simulated mode) (see 4.3 Surround Function). Pin voltage: approx. 6.0 V
30	MFI		High-pass filter input pin for surround function (Simulated mode) (see 4.3 Surround Function). Pin voltage: approx. 6.0 V

2. ATTENTIONS

<1> Attention on Pop Noise Reduction

When changing the surround mode and switching power, use the mute function (approx. 200 ms) for pop noise reduction (see **4.4.1(2) Mute** for the μ PC1853-01 or **4.4.2(1) Mute** for the μ PC1853-02).

<2> Attention on Supply Voltage

Drive data on the I²C bus after supply voltage of total application system becomes stable.

3. I²C BUS INTERFACE

The μPC1853 has serial bus function. This serial bus (I²C bus) is a double wired bus developed by Philips. It is composed of 2 wires: serial clock line (SCL) and serial data line (SDA).

The μPC1853 has built-in I²C bus interface circuit, 9 rewritable registers (8 bits).

SCL (Serial Clock Line)

The master CPU outputs serial clock to synchronize with the data. According to this clock, the μPC1853 takes in the serial data.

Input level is compatible with CMOS.

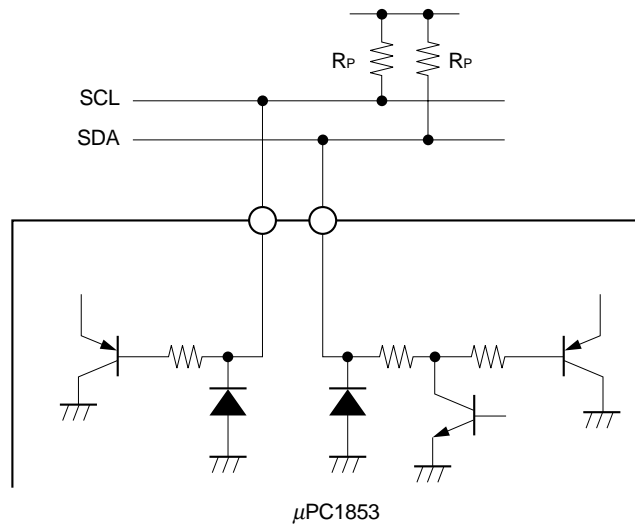
Clock frequency is 0 to 100 kHz.

SDA (Serial Data Line)

The master CPU outputs the data which is synchronized with serial clock. The μPC1853 takes in this data according to the clock.

Input level is compatible with CMOS.

Fig. 3-1 Internal Equivalent Circuits of Interface Pin



3.1 Data Transfer

3.1.1 Start condition

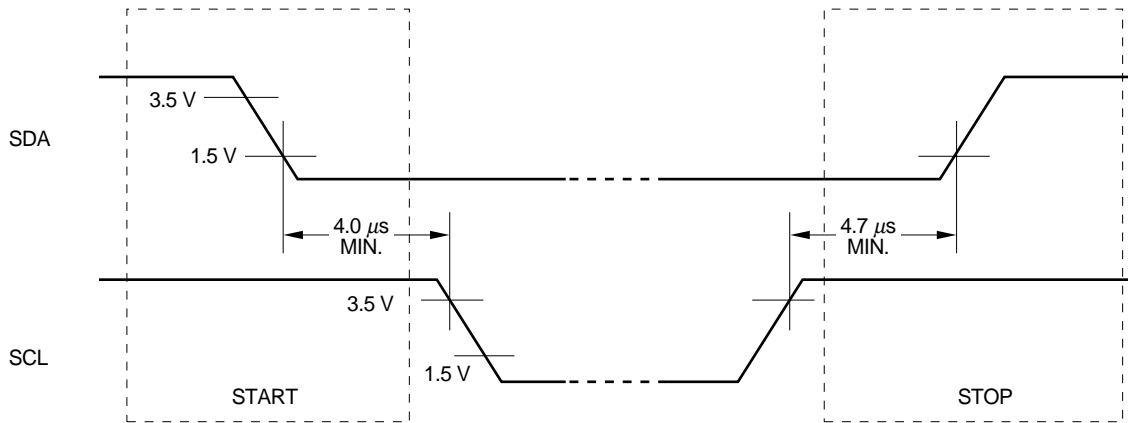
Start condition is made by falling of SDA from “High” to “Low” during SCL is “High” as shown in Fig. 3-2.

When this start condition is received, the μPC1853 takes in the data synchronizing with the clock after that.

3.1.2 Stop condition

Stop condition is made by rising of SDA from “Low” to “High” during SCL is “High” as shown in Fig. 3-2. When this stop condition is received, the μPC1853 stops to take in or output the data.

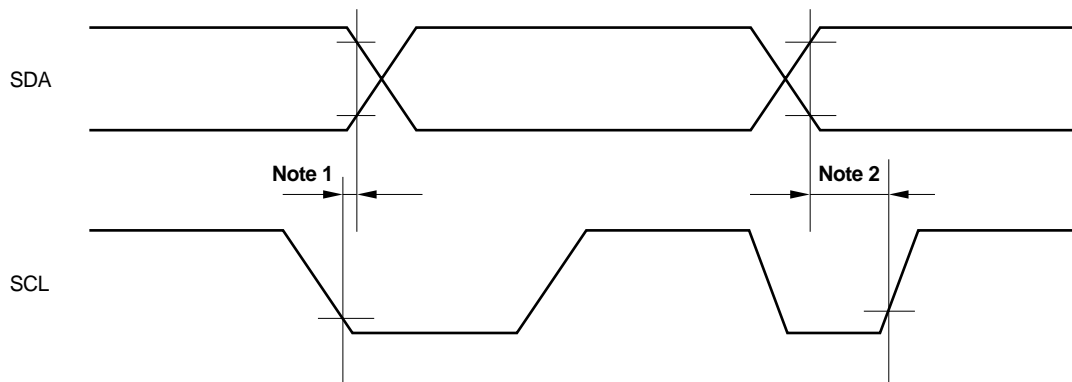
Fig. 3-2 Start/Stop Condition of Data Transfer



3.1.3 Data transfer

In the case of data transfer, data changing should be executed while SCL is “Low” like Fig. 3-3. When SCL is “High”, be sure not to change the data.

Fig. 3-3 Data Transfer



Note 1. Data hold time for I²C device: 300 ns MIN., Data hold time for CPU: 5 μs MIN.

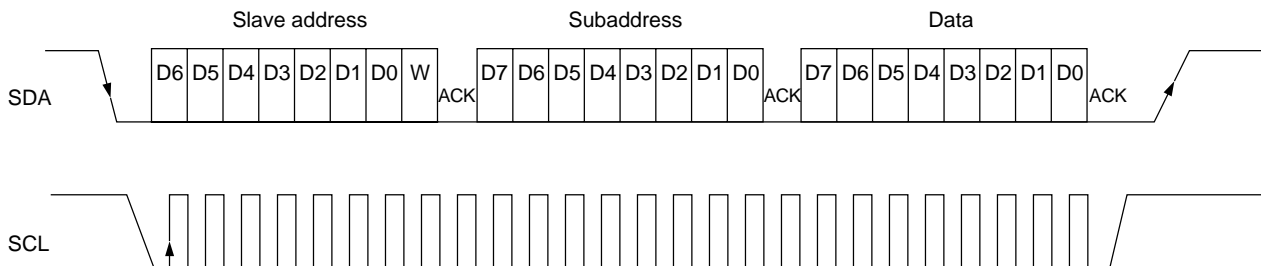
2. Data set-up time: 250 ns MIN.

Remark Clock frequency: 0 to 100 kHz

3.2 Data Transfer Format

Fig. 3-4 is an example of data transfer in write mode.

Fig. 3-4 Example of Data Transfer in Write Mode



Remark W: Write mode, ACK: Acknowledge bit

Data is composed of 8 bits. Acknowledge bit is always added after this 8 bits data. Data should be transferred from MSB first.

The 1 byte immediately after start condition specifies the slave address (chip address). This slave address is composed of 7 bits.

Table 3-1 is the slave address of the μPC1853. This slave address is registered by Phillips.

Table 3-1 Slave Address of μPC1853

Bias Voltage of ADS (Pin 22)	Slave address						
	D6	D5	D4	D3	D2	D1	D0
5V	1	0	0	0	1	1	0
GND	1	0	0	0	1	0	0

User can set bit D1 freely.

- 0: Bias voltage of ADS (pin 22) is GND.
- 1: Bias voltage of ADS (pin 22) is 5 V.

The remaining 1 bit is the read/write bit which specifies the direction of the data transferred after that. Set “0” because the μPC1853 has write mode only.

The byte following the slave address is subaddress byte of the μPC1853.

The μPC1853 has 9 subaddresses from SA₀ to SA₈, and each of them is composed of 8 bits. The data to be set to the subaddress follows this subaddress byte.

The μPC1853 has automatic increment function. This function increments subaddress automatically in write mode.

By using automatic increment function, once slave address and subaddress are set, data can be transferred continuously to the next subaddress. Use this function for initializing and so on. In the case of changing the data continuously of one subaddress (adjustment and so on), set the automatic increment function OFF (see **4.4.1(8) Automatic increment function**).

3.2.1 1 byte data transfer

The following is the format in the case of transferring 1 byte data.

S T A	SLAVE ADDRESS	W	A C K	SUB ADDRESS	A C K	DATA	A C K	S T P
-------------	------------------	---	-------------	----------------	-------------	------	-------------	-------------

Remark STA: Start, W: Write mode, ACK: Acknowledge bit, STP: Stop

3.2.2 Serial data transfer

The following is the format in the case of transferring 8 bytes data at one time by using automatic increment function (the data of subaddress 01H to 08H, bit D6 is "1").

S T A	SLAVE ADDRESS	W	A C K	SUB ADDRESS	A C K	DATA1	A C K	DATA2	A C K	---	DATA9	A C K	S T P
-------------	------------------	---	-------------	----------------	-------------	-------	-------------	-------	-------------	-----	-------	-------------	-------------

Remark STA: Start, W: Write mode, ACK: Acknowledge, STP: Stop

The master CPU transfers "00H" as subaddress SA₀ after start and slave address like above figure. It transfers the data of SA₀ after subaddress, and then transfers the data of SA₁, SA₂..., SA₈ continuously without transferring stop condition. Finally, it transfers stop condition and terminates.

The increments of the subaddress of the μPC1853 stops automatically when the subaddress comes to "08H" inside of it.

3.2.3 Acknowledge

On I²C bus, acknowledge bit is added to the 9th bit after the data in order to judge whether data transfer has been succeeded or not. The master CPU judges it from "High" and "Low" of acknowledge condition.

When this acknowledge period is "Low", it means success. And when the condition is "High", it means failure of transfer or forced release of bus as NAK state.

The condition of being NAK state is when wrong slave address is transferred to slave IC or data transfer from slave side is finished in read state.

4. EXPLANATION OF EACH COMMAND

4.1 Subaddress List

(1) μPC1853-01

Bit Sub-address	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	Rear output selection 0: φ(L-R) 1: L-R	Low boost 0: OFF 1: ON	Low boost gain 0: 6 dB 1: 3 dB	Rear output mute 0: OFF 1: ON	L+R signal output mute 0: OFF 1: ON	Audio output mute 0: OFF 1: ON	Main output mute 0: OFF 1: ON	Audio output control link 0: OFF 1: ON
01H	0	Automatic increment 0: OFF 1: ON	Main output volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
02H	0	Automatic increment 0: OFF 1: ON	Balance control L-channel attenuation volume : Low to Flat to Flat R-channel attenuation volume : Flat to Flat to Low Data : 111111 to 100000 to 000000					
03H	0	Automatic increment 0: OFF 1: ON	Bass control Gain : Boost to 0 dB to Cut Data : 111111 to 100000 to 000000					
04H	0	Automatic increment 0: OFF 1: ON	Treble control Gain : Boost to 0 dB to Cut Data : 111111 to 100000 to 000000					
05H	0	Automatic increment 0: OFF 1: ON	L+R signal output volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
06H	0	Automatic increment 0: OFF 1: ON	Audio output volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
07H	0	Automatic increment 0: OFF 1: ON	Rear output volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
08H	Surround ON/OFF 0: OFF 1: ON	Automatic increment 0: OFF 1: ON	Units of phase shifters 0: 4 units 1: 1 unit	Monaural/Stereo selection 0: Stereo 1: Monaural	Effect control Effect : Large to Normal to Small Data : 1111 to 1000 to 0000			

Caution Be sure to write data "0" in the subaddress 01H to 07H, bit D7.

(2) μ PC1853-02

Sub-address \ Bit	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	Rear output selection 0: ϕ (L-R) 1: L-R	0	0	Rear output mute 0: OFF 1: ON	L+R signal output mute 0: OFF 1: ON	Audio output mute 0: OFF 1: ON	0	0
01H	0	Automatic increment 0: OFF 1: ON	R-channel signal output (R1 OUT pin) volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
02H	0	Automatic increment 0: OFF 1: ON	L-channel signal output (L1 OUT pin) volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
03H	0	Automatic increment 0: OFF 1: ON	Bass control Gain : Boost to 0 dB to Cut Data : 111111 to 100000 to 000000					
04H	0	Automatic increment 0: OFF 1: ON	Treble control Gain : Boost to 0 dB to Cut Data : 111111 to 100000 to 000000					
05H	0	Automatic increment 0: OFF 1: ON	L+R signal output volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
06H	0	Automatic increment 0: OFF 1: ON	Audio output volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
07H	0	Automatic increment 0: OFF 1: ON	Rear output volume control Attenuation volume : Flat to Low Data : 111111 to 000000					
08H	Surround ON/OFF 0: OFF 1: ON	Automatic increment 0: OFF 1: ON	Units of phase shifters 0: 4 units 1: 1 unit	Monaural/Stereo selection 0: Stereo 1: Monaural	Effect control Effect : Large to Normal to Small Data : 1111 to 1000 to 0000			

Caution Be sure to fix data of the subaddress 00H, bit D6, D5, D1, D0 and subaddress 01H to 07H, bit D7 to "0".

4.2 Initialization

After power-on, be sure to initialize the subaddress data to table below.

Table 4-1 Initial Data of μ PC1853-01

Subaddress \ Bit	Bit							
	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	1	0	0	0	0	0	0	0
01H	0	1	1	1	1	1	1	1
02H	0	1	1	0	0	0	0	0
03H	0	1	1	0	0	0	0	0
04H	0	1	1	0	0	0	0	0
05H	0	1	1	1	1	1	1	1
06H	0	1	1	1	1	1	1	1
07H	0	1	1	1	1	1	1	1
08H	0	1	0	0	1	0	0	0

Table 4-2 Initial Data of μ PC1853-02

Subaddress \ Bit	Bit							
	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	1	0	0	0	0	0	0	0
01H	0	1	1	1	1	1	1	1
02H	0	1	1	1	1	1	1	1
03H	0	1	1	0	0	0	0	0
04H	0	1	1	0	0	0	0	0
05H	0	1	1	1	1	1	1	1
06H	0	1	1	1	1	1	1	1
07H	0	1	1	1	1	1	1	1
08H	0	1	0	0	1	0	0	0

Caution Until initializing completely, mute by the external units.

4.3 Surround Function

About the setting of surround mode, see table below.

Table 4-3 Setting of Surround Mode

Setting Surround mode	Subaddress: 08H			Description		
	D7	D5	D4	Surround ON/OFF	Units of phase shifter	Monaural/Stereo selection
OFF	0	–	–	OFF	–	–
Movie	1	0	0	ON	4 units	Stereo
Music	1	1	0		1 unit	
Simulated	1	0	1		4 units	Monaural

–: Don't care.

Caution When changing the surround mode, use the mute function (approx. 200 ms) for pop noise reduction (see 4.4.1(2) Mute for the μPC1853-01 or 4.4.2(1) Mute for the μPC1853-02).

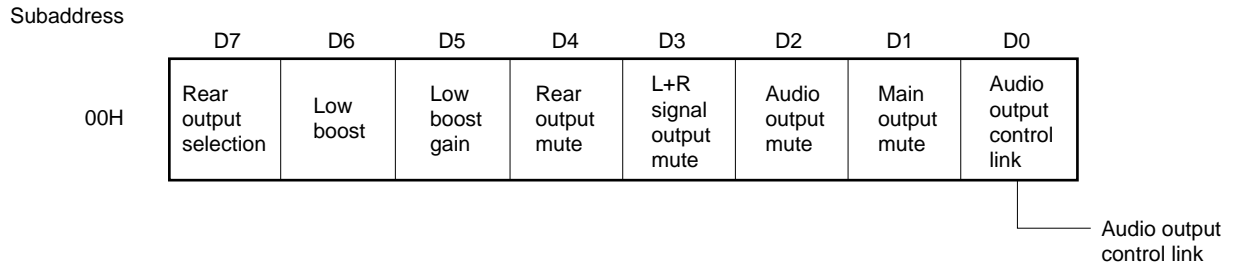
4.4 Explanation of Each Command

4.4.1 μPC1853-01

(1) Audio Output Control Link

By the data of subaddress 00H, bit D0, audio output volume link can be controlled (linked with main output control or not).

Fig. 4-1 Audio Output Control Link



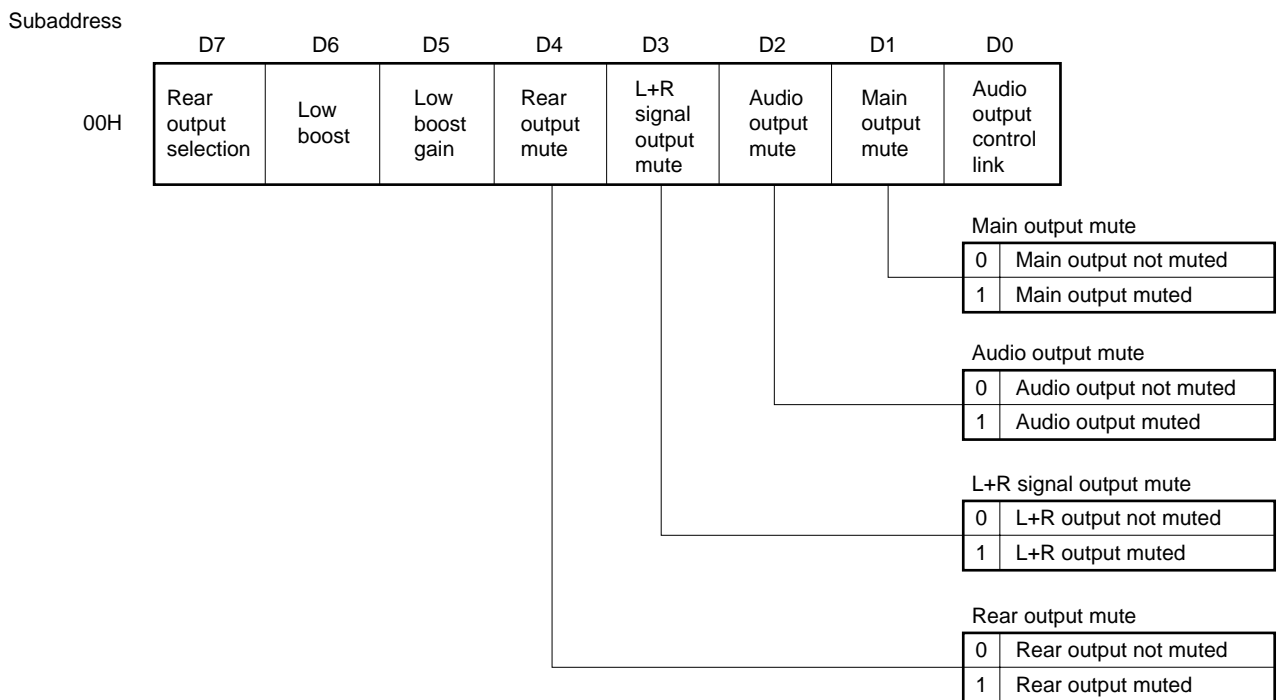
Audio output control link

0	Audio output volume controlled independently.
	Main output volume control (Subaddress: 01H, Bit: D5 to D0) Audio output volume control (Subaddress: 06H, Bit: D5 to D0)
1	Audio output volume control can be linked with main output volume control.
	Main output volume and audio output volume control (Subaddress: 01H, Bit: D5 to D0)

(2) Mute

By the data of subaddress 00H, bit D1 to D4, ON/OFF of mute function can be controlled.

Fig. 4-2 Mute (μPC1853-01)

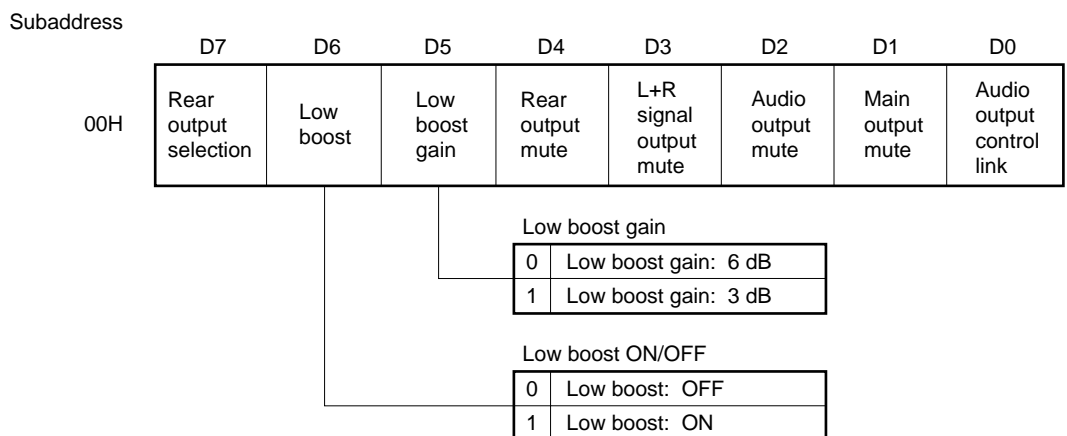


Caution Use the mute function (approx. 200 ms) for pop noise reduction when changing the surround mode and switching power.

(3) Low boost function

By the data of subaddress 00H, bit D5, the low boost gain can be selected (3 dB or 6 dB). And, by the data of subaddress 00H, bit D6 ON/OFF of the low boost can be controlled.

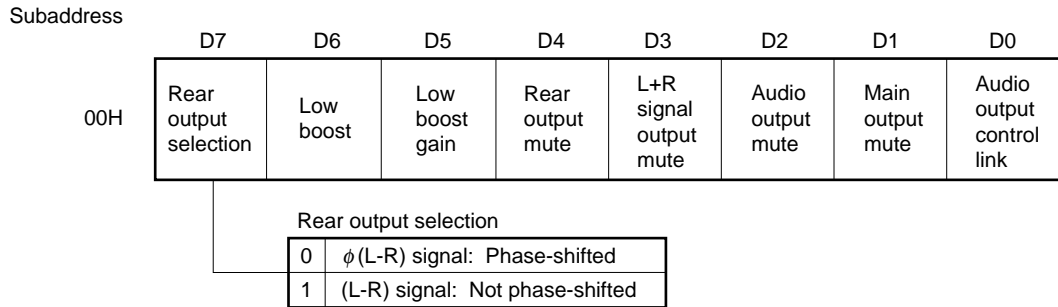
Fig. 4-3 Low Boost Function



(4) Rear output selection

By the data of subaddress 00H, bit D7, output signal of the rear output pin can be selected (ϕ (L-R) signal or (L-R) signal).

Fig. 4-4 Rear Output Selection (μPC1853-01)

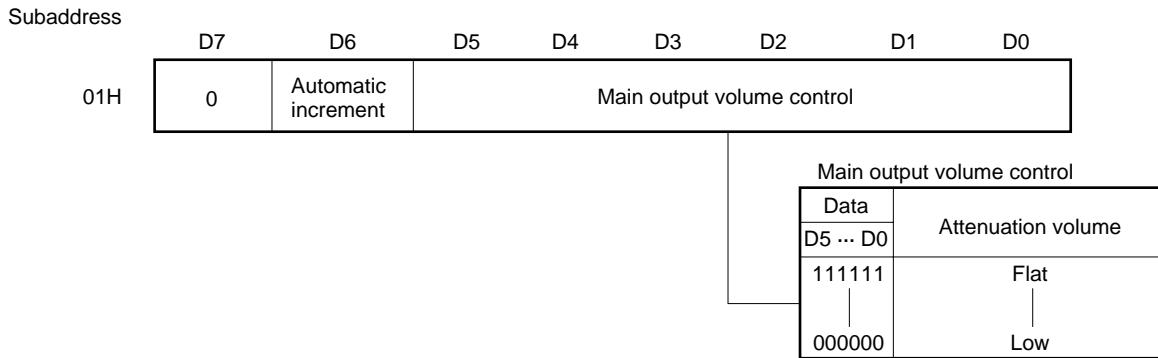


(5) Volume control

By the data of subaddress 01H, 05H, 06H and 07H, bit D5 to D0, the volume control can be adjusted in 64 levels.

Fig. 4-5 Volume Control (μPC1853-01) (1/2)

• **Main output volume control**



• **L+R signal output volume control**

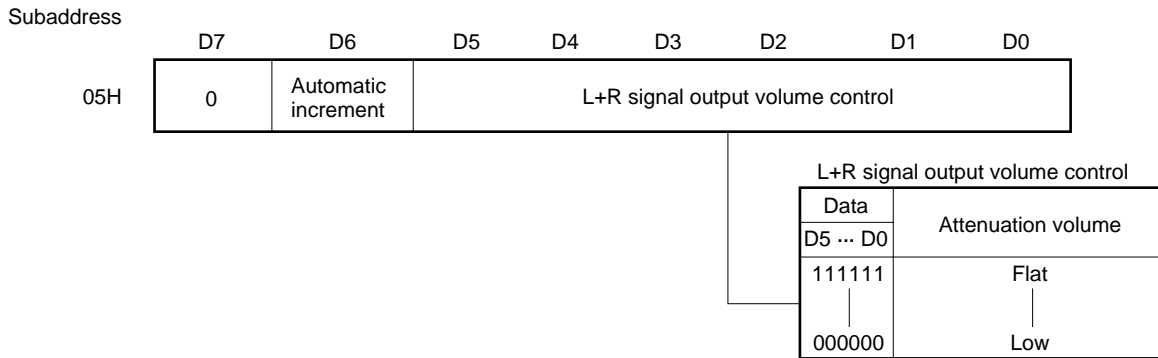
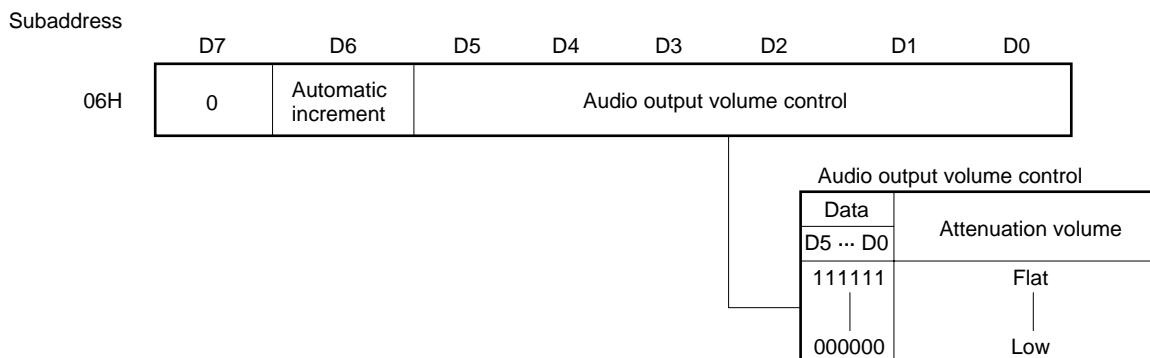


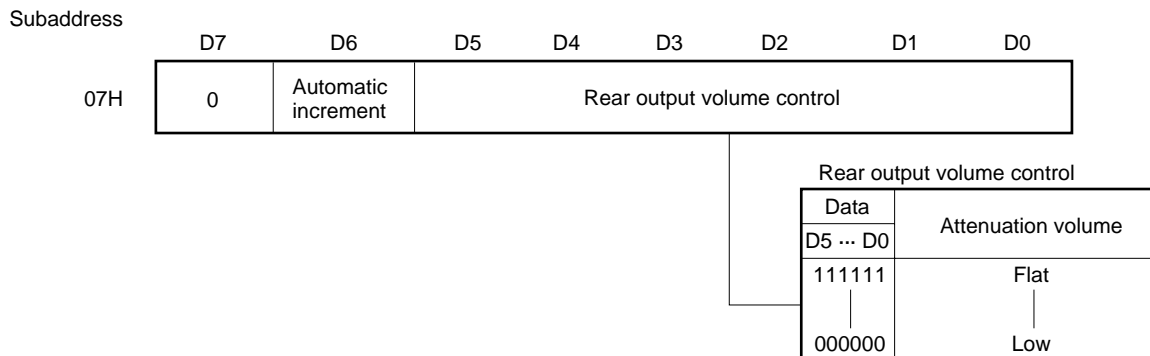
Fig. 4-5 Volume Control (μPC1853-01) (2/2)

• Audio output volume control^{Note}



Note When selecting the mode linking main output volume control to audio output volume control, the audio output volume can be controlled by the data of main output volume control (see **(1) Audio Output Control Link**). In that case, fix the audio output volume control data to “111111”.

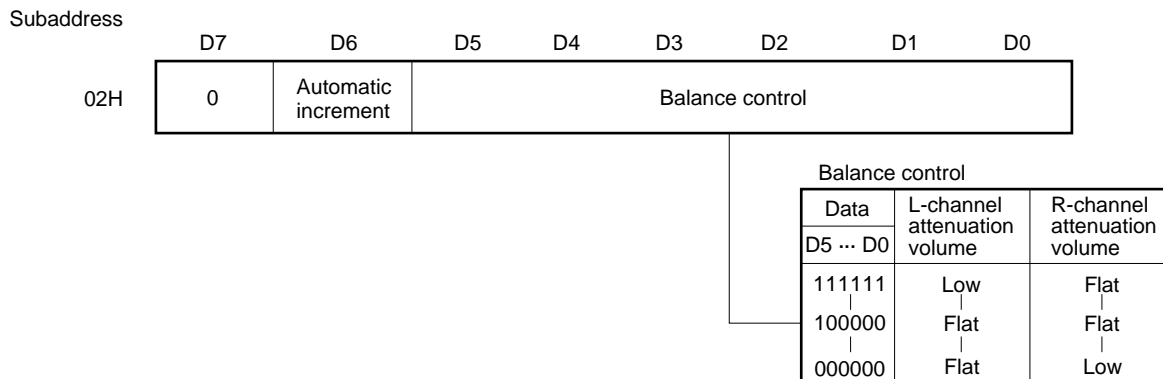
• Rear output volume control



(6) Balance control

By the data of subaddress 02H, bit D5 to D0, the balance level of L1 OUT and R1 OUT pin can be adjusted in 64 levels.

Fig. 4-6 Balance Control

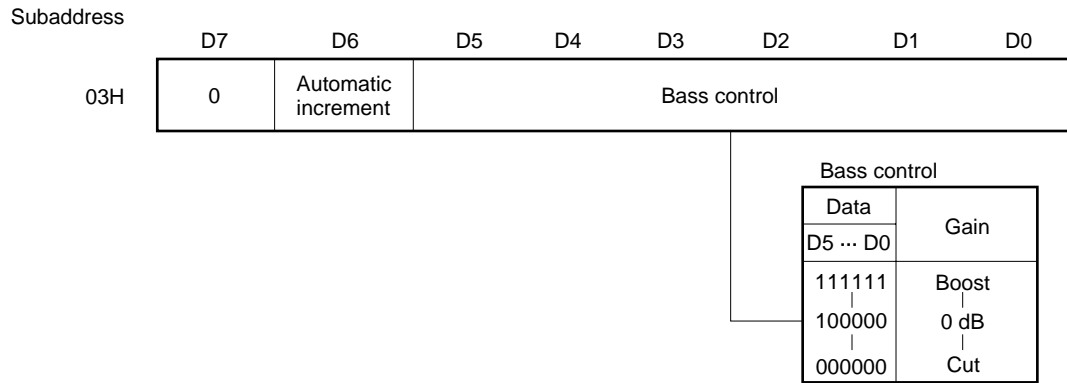


(7) Bass and treble control

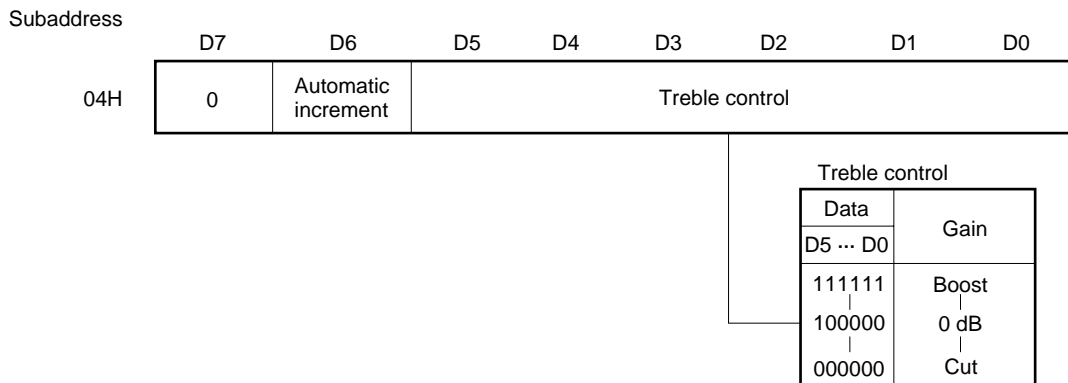
By the data of subaddress 03H and 04H, bit D5 to D0, the bass and treble tone for main output (L1 OUT and R1 OUT pin) can be adjusted in 64 levels.

Fig. 4-7 Bass and Treble Control

• **Bass control**



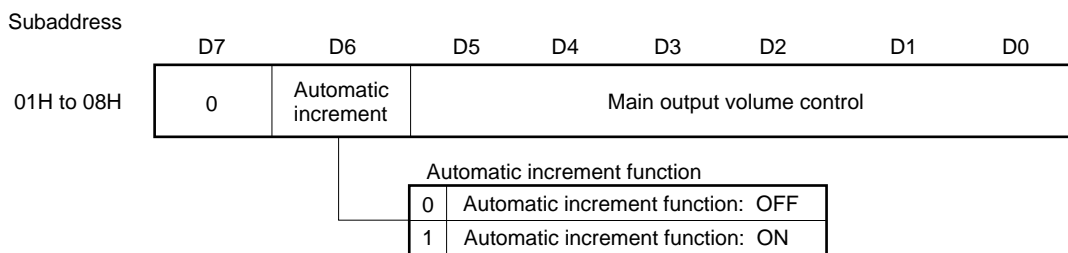
• **Treble control**



(8) Automatic increment function

By the data of subaddress 01H to 08H, bit D6, ON/OFF of the automatic increment function can be controlled.

Fig. 4-8 Automatic Increment Function



Caution After power-on, be sure to initialize the subaddress data (see 4.2 Initialization).

The automatic increment function increments subaddress automatically.

Automatic increment function is ON : Subaddress is incremented automatically.
 If once slave address and subaddress are set, without setting the next subaddress, data of the next subaddress can be transferred.

Automatic increment function is OFF: Subaddress is fixed.
 Data of the fixed subaddress can be set repeatedly.

The automatic increment ON/OFF bit is in the subaddress 01H to 08H. The increment of subaddress is controlled individually by each automatic increment ON/OFF bit. As for 00H, subaddress is not incremented automatically (see 4.1 Subaddress List).

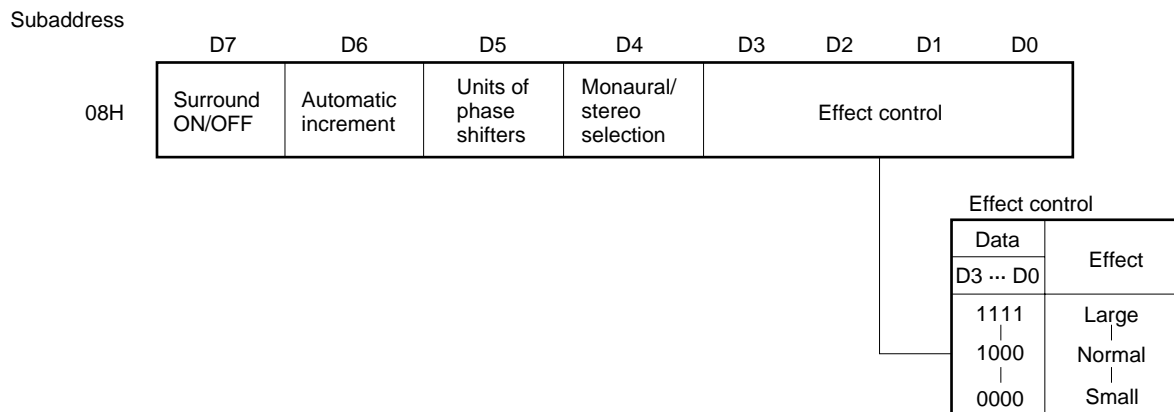
For example, when the automatic increment function of subaddress 01H is ON and that of 02H is OFF, subaddress is incremented from 01H to 02H automatically and is fixed on 02H.

In case of the automatic increment function of 08H is ON, subaddress is not incremented. If next data is transferred after setting data of 08H (acknowledge bit: L), the acknowledge condition is changed into NAK state (acknowledge bit: H). And the data transfer from the master CPU is stopped.

(9) Effect control

By the data of subaddress 08H, bit D3 to D0, the level of indirect sound signal (surround signal) added to the original signal can be adjusted in 16 levels.

Fig. 4-9 Effect Control



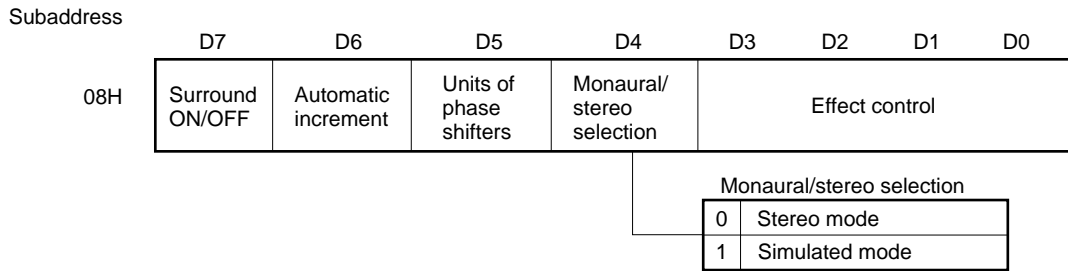
(10) Monaural/Stereo selection

By the data of subaddress 08H, bit D4, the surround mode can be selected (stereo mode or simulated mode).

Stereo mode : Surround signal processing for stereo source.
 The phase of the difference between L-channel and R-channel signals is shifted and added to the original signal.

Simulated mode : Stereo sound simulation for monaural source.
 The phase of the difference between the signal through HPF and the signal through LPF is shifted, and the signals are added to the original signal. When the output frequency characteristics of L-channel and R-channel signals become the form of comb, stereo sound simulation can be realized.

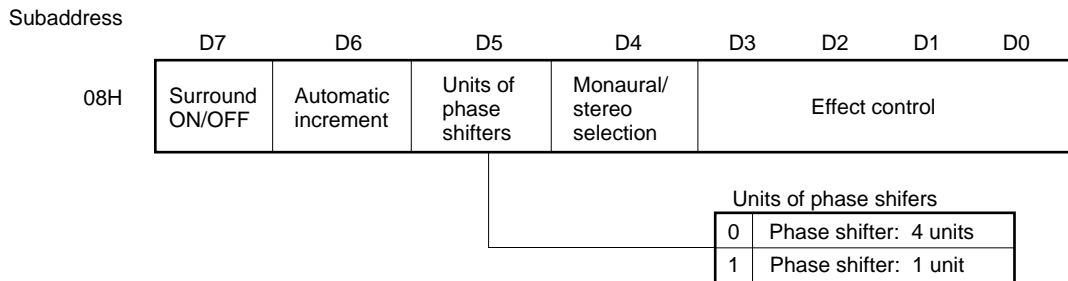
Fig. 4-10 Monaural/Stereo Selection



(11) Units of phase shifters

By the data of subaddress 08H, bit D5, the number of phase shifter's units (1 or 4 units) can be selected for the indirect sound signal (surround signal).

Fig. 4-11 Units of Phase Shifters



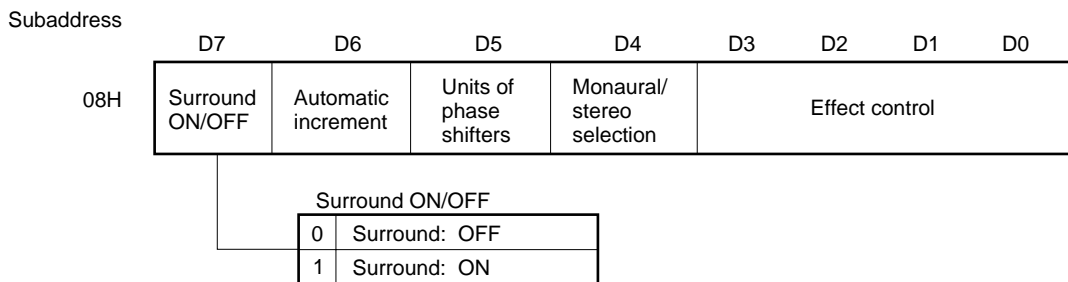
(12) Surround ON/OFF

By the data of subaddress 08H, bit D7, ON/OFF of surround (indirect sound) mode can be selected.

Surround OFF: Original signal is taken out directly (OFF mode).

Surround ON : The signal passed through the phase shifter (indirect sound) is added to the original signal (Movie, Music and Simulated mode).

Fig. 4-12 Surround ON/OFF

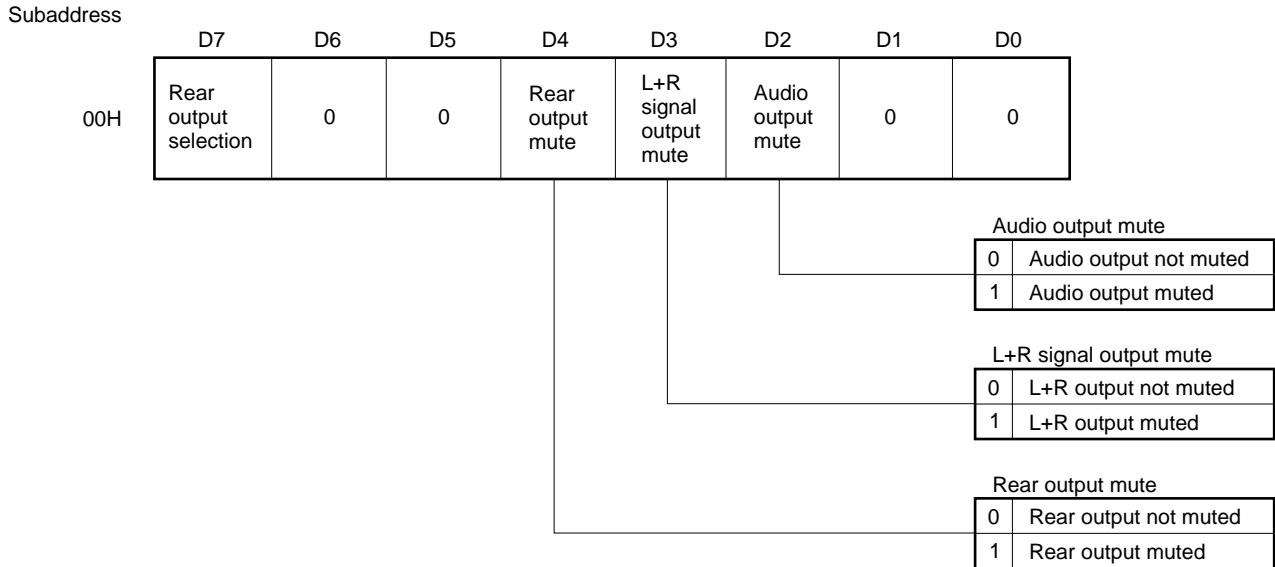


4.4.2 μPC1853-02

(1) Mute

By the data of subaddress 00H, bit D2 to D4, ON/OFF of mute function can be controlled.

Fig. 4-13 Mute (μPC1853-02)

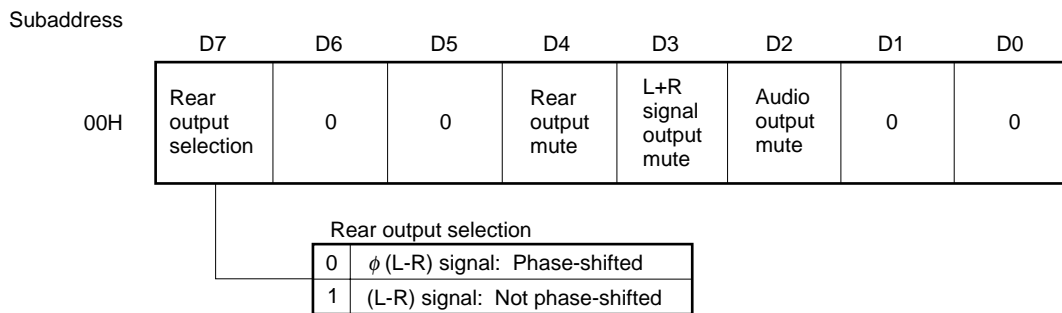


Caution Use the mute function (approx. 200 ms) for pop noise reduction when changing the surround mode and switching power.

(2) Rear output selection

By the data of subaddress 00H, bit D7, output signal of the rear output pin can be selected (ϕ (L-R) signal or (L-R) signal).

Fig. 4-14 Rear Output Selection (μPC1853-02)

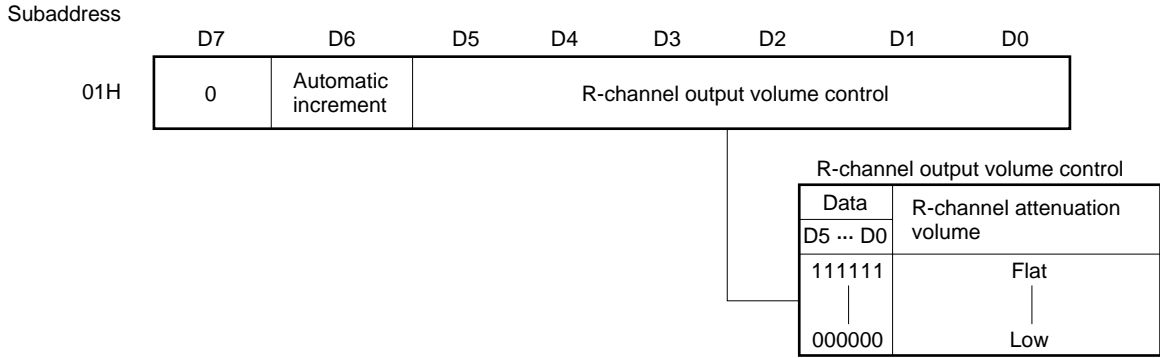


(3) Volume control

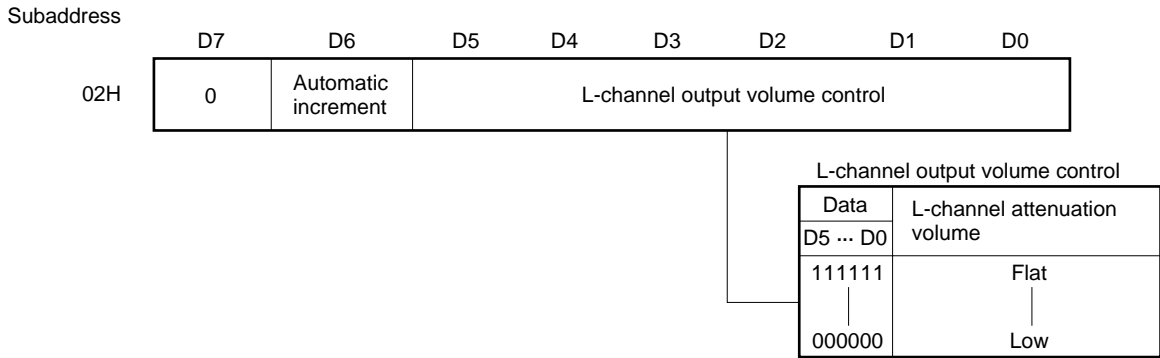
By the data of subaddress 01H, 02H, 05H, 06H and 07H, bit D5 to D0, the volume control can be adjusted in 64 levels.

Fig. 4-15 Volume Control (μPC1853-02) (1/2)

• **R-channel output volume control**



• **L-channel output volume control**



• **L+R signal output volume control**

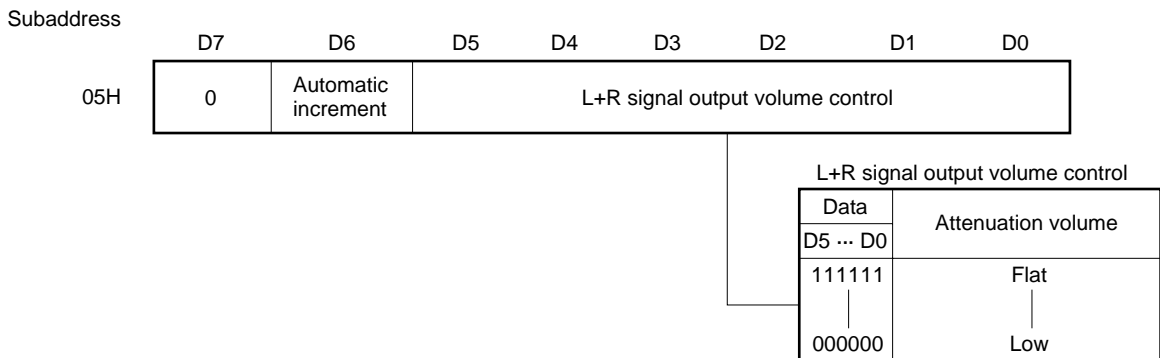
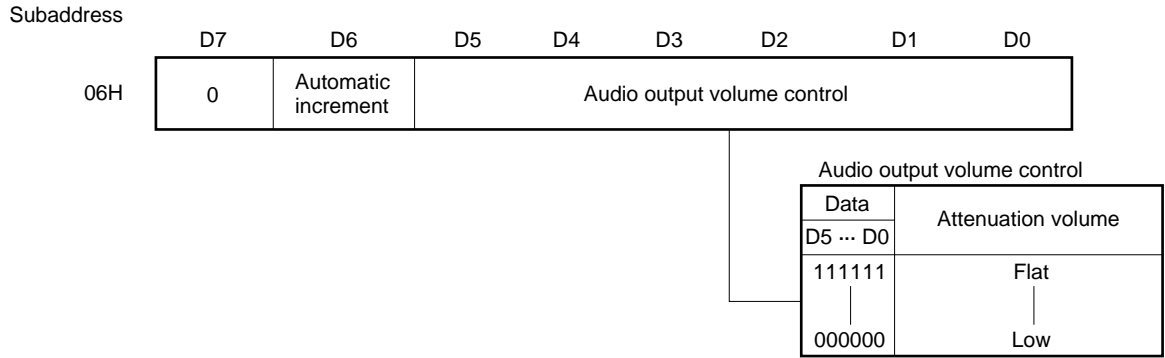
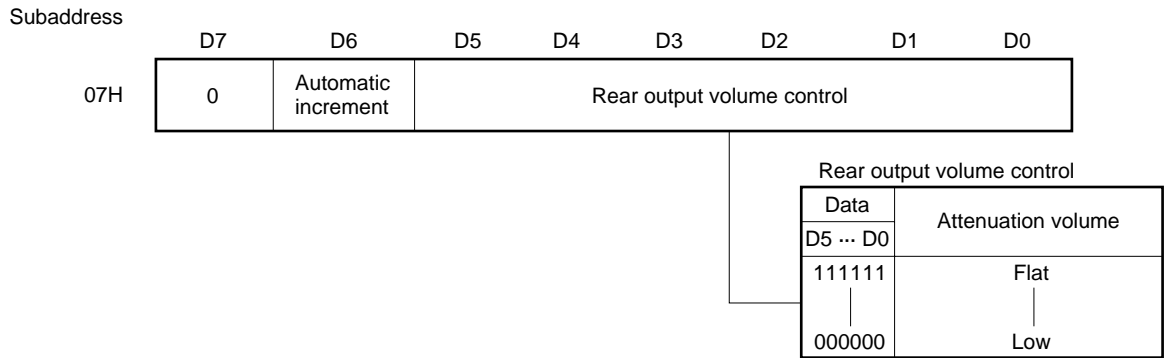


Fig. 4-15 Volume Control (μPC1853-02) (2/2)

• Audio output volume control



• Rear output volume control



- (4) **Bass and treble control**
See 4.4.1 (7) Bass and treble control.
- (5) **Automatic increment function**
See 4.4.1 (8) Automatic increment function.
- (6) **Effect control**
See 4.4.1 (9) Effect control.
- (7) **Monaural/Stereo selection**
See 4.4.1 (10) Monaural/Stereo selection.
- (8) **Units of phase shifters**
See 4.4.1 (11) Units of phase shifters.
- (9) **Surround ON/OFF**
See 4.4.1 (12) Surround ON/OFF.

5. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Unless otherwise specified, $T_A = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Test conditions	Ratings	Unit
Supply voltage	V_{CC}	No signal	14.0	V
Input signal voltage	V_{IN}		V_{CC}	V
I ² C bus input pin voltage	V_{cont}		$V_{CC} + 0.2$	V
Power dissipation	P_D	$T_A = 75\text{ }^\circ\text{C}$	500	mW
Operating temperature	T_A	$V_{CC} = 12\text{ V}$	-20 to +75	°C
Storage temperature	T_{stg}		-40 to +125	°C

Recommended Operating Conditions (Unless otherwise specified, $T_A = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		10.8	12.0	13.2	V
Input signal voltage	V_{IN}	$V_{CC} = 12\text{ V}$, Gain of input-output: 0 dB	0.0	1.4	7.9	V_{p-p}
I ² C bus input pin voltage (H)	V_{contH}	Pins SDA and SCL	3.5	5.0	6.0	V
I ² C bus input pin voltage (L)	V_{contL}		0.0	0.0	1.5	V

Electrical Characteristics

($V_{CC} = 12\text{ V}$, $T_A = 25\text{ °C}$, $RH \leq 70\%$, $f = 1\text{ kHz}$, $V_{IN} = 0.5\text{ V}_{rms}$, No load impedance, unless otherwise specified)

General (1/1)

Parameter	Symbol	Test conditions	Switch mode ^{Note}			Subaddress data								MIN.	TYP.	MAX.	Unit	
			S1	S2	S3	00	01	02	03	04	05	06	07					08
Supply current	I_{CC}	No signal	b	b	–	80	7F	60	60	60	7F	7F	7F	48	16	24	32	mA
Maximum input voltage 1	V_{OM1}	L_{in} , $R_{in} \geq 2.8\text{ V}_{rms}$, THD = 1 %, L1 OUT, R1 OUT, L2 OUT, R2 OUT, L+R OUT	a	a	–	80	7F	60	60	60	7F	7F	7F	48	7.9	8.8	9.3	V_{p-p}
Maximum input voltage 2	V_{OM2}	$L_{in} \geq 2.8\text{ V}_{rms}$, $R_{in} = \text{GND}$, THD = 1 %, Rear OUT	a	b	–	80	7F	60	60	60	7F	7F	7F	48	2.5	2.8	3.3	V_{p-p}
Distortion rate (L-ch)	THD _L	$f = 1\text{ kHz}$, $L_{in} = 0.5\text{ V}_{rms}$, $R_{in} = \text{GND}$, L1 OUT, L2 OUT	a	b	–	80	7F	60	60	60	7F	7F	7F	48	–	0.1	0.5	%
Distortion rate (R-ch)	THD _R	$f = 1\text{ kHz}$, $L_{in} = \text{GND}$, $R_{in} = 0.5\text{ V}_{rms}$, R1 OUT, R2 OUT	b	a	–	80	7F	60	60	60	7F	7F	7F	48	–	0.1	0.5	%

–: Don't care.

Note See 7. MEASURING CIRCUIT.

Remark The values are common to both the $\mu\text{PC1853CT-01}$ and $\mu\text{PC1853CT-02}$.

(1) μPC1853CT-01 Volume control, tone control block (1/3)

Parameter	Symbol	Test conditions	Switch mode ^{Note}			Subaddress data								MIN.	TYP.	MAX.	Unit	
			S1	S2	S3	00	01	02	03	04	05	06	07					08
Volume attenuation 1 (1)	ATT _{VL11}	Lin = 0.5 V _{rms} , Rin = GND,	a	b	-	80	7F	60	60	60	7F	7F	7F	48	-1.5	0.0	+1.5	dB
Volume attenuation 1 (2)	ATT _{VL12}	L1 OUT					60							-25.0	-19.0	-13.0	dB	
Volume attenuation 1 (3)	ATT _{VL13}						40							-80.0	-	-	dB	
Volume attenuation 2 (1)	ATT _{VL21}	Lin = 0.5 V _{rms} , Rin = GND,	a	b	-	80	7F	60	60	60	7F	7F	7F	48	-1.5	0.0	+1.5	dB
Volume attenuation 2 (2)	ATT _{VL22}	L2 OUT										60		-25.0	-19.0	-13.0	dB	
Volume attenuation 2 (3)	ATT _{VL23}											40		-80.0	-	-	dB	
L+R volume attenuation 1	ATT _{VLR1}	Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} ,	a	a	-	80	7F	60	60	60	7F	7F	7F	48	-1.5	0.0	+1.5	dB
L+R volume attenuation 2	ATT _{VLR2}	L+R OUT										60		-25.0	-19.0	-13.0	dB	
L+R volume attenuation 3	ATT _{VLR3}											40		-80.0	-	-	dB	
Rear volume attenuation 1	ATT _{VRE1}	Lin = 0.5 V _{rms} , Rin = GND,	a	b	-	80	7F	60	60	60	7F	7F	7F	48	8.5	10.0	11.5	dB
Rear volume attenuation 2	ATT _{VRE2}	Rear OUT											60	-15.0	-9.0	-3.0	dB	
Balance attenuation (L-ch) 1 (1)	ATT _{BL11}	Lin = 0.5 V _{rms} , Rin = GND,	a	b	-	80	7F	41	60	60	7F	7F	7F	48	-1.5	0.0	+1.5	dB
Balance attenuation (L-ch) 1 (2)	ATT _{BL12}	L1 OUT						60						-1.5	0.0	+1.5	dB	
Balance attenuation (L-ch) 1 (3)	ATT _{BL13}							7F						-80.0	-	-	dB	
Balance attenuation (R-ch) 1 (1)	ATT _{BR11}	Lin = GND, Rin = 0.5 V _{rms} ,	b	a	-	80	7F	41	60	60	7F	7F	7F	48	-80.0	-	-	dB
Balance attenuation (R-ch) 1 (2)	ATT _{BR12}	R1 OUT						60						-1.5	0.0	+1.5	dB	
Balance attenuation (R-ch) 1 (3)	ATT _{BR13}							7F						-1.5	0.0	+1.5	dB	
Low-band boost control	V _{BB}	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	b	-	80	7F	60	7F	60	7F	7F	7F	48	7.0	10.0	13.0	dB
Low-band flat control	V _{BF}	Rin = GND, L1 OUT							60					-3.0	0.0	+3.0	dB	
Low-band cut control	V _{BC}								41					-13.0	-10.0	-7.0	dB	
Low-band boost control (6 dB) 1	V _{B6dB1}	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	b	-	80	7F	60	60	60	7F	7F	7F	48	2.0	3.0	4.0	dB
Low-band boost control (6 dB) 2	V _{B6dB2}	Rin = GND, L1 OUT					↓	60						3.0	4.0	5.0	dB	
Low-band boost control (6 dB) 3	V _{B6dB3}					C0	50							4.0	6.0	8.0	dB	

-: Don't care.

Note See 7. MEASURING CIRCUIT.

(1) μ PC1853CT-01 Volume control, tone control block (2/3)

Parameter	Symbol	Test conditions	Switch mode ^{Note}			Subaddress data								MIN.	TYP.	MAX.	Unit	
			S1	S2	S3	00	01	02	03	04	05	06	07					08
Low-band boost control (3 dB) 1	V _{B3dB1}	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	b	–	A0	7F	60	60	60	7F	7F	7F	48	0.5	1.5	2.5	dB
Low-band boost control (3 dB) 2	V _{B3dB2}	Rin = GND, L1 OUT				↓	60							1.0	2.0	3.0		
Low-band boost control (3 dB) 3	V _{B3dB3}					E0	50							2.0	3.0	4.0		
High-band boost control	V _{TB}	f = 10 kHz, Lin = 0.5 V _{rms} ,	a	b	–	80	7F	60	60	7F	7F	7F	48	7.0	10.0	13.0	dB	
High-band flat control	V _{TF}	Rin = GND, L1 OUT					60							–3.0	0.0	+3.0		
High-band cut control	V _{TC}						41							–13.0	–10.0	–7.0		
L, R in-phase gain difference 1 (1)	DG ₁₁	Lin = GND, Rin = 0.5 V _{rms} ,	b	a	–	80	7F	60	60	60	7F	7F	48	–1.0	0.0	+1.0	dB	
L, R in-phase gain difference 1 (2)	DG ₁₂	L1 OUT, R1 OUT					60							–1.0	0.0	+1.0		
L, R in-phase gain difference 2 (1)	DG ₂₁	Lin = GND, Rin = 0.5 V _{rms} ,	b	a	–	80	7F	60	60	60	7F	7F	48	–1.0	0.0	+1.0	dB	
L, R in-phase gain difference 2 (2)	DG ₂₂	L2 OUT, R2 OUT									60			–1.0	0.0	+1.0		
L, R in-phase gain difference 3 (1)	DG ₃₁	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	a	–	80	7F	60	7F	60	7F	7F	48	–1.0	0.0	+1.0	dB	
L, R in-phase gain difference 3 (2)	DG ₃₂	Rin = 0.5 V _{rms} ,							60					–1.0	0.0	+1.0		
L, R in-phase gain difference 3 (3)	DG ₃₃	L1 OUT, R1 OUT							41					–1.0	0.0	+1.0		
L, R in-phase gain difference 4 (1)	DG ₄₁	f = 10 kHz, Lin = 0.5 V _{rms} ,	a	a	–	80	7F	60	60	7F	7F	7F	48	–1.0	0.0	+1.0	dB	
L, R in-phase gain difference 4 (2)	DG ₄₂	Rin = 0.5 V _{rms} ,							60					–1.0	0.0	+1.0		
L, R in-phase gain difference 4 (3)	DG ₄₃	L1 OUT, R1 OUT							41					–1.0	0.0	+1.0		
L, R in-phase gain difference 5 (1)	DG ₅₁	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	a	–	80	7F	60	60	60	7F	7F	48	–1.0	0.0	+1.0	dB	
L, R in-phase gain difference 5 (2)	DG ₅₂	Rin = 0.5 V _{rms} ,				↓	60							–1.0	0.0	+1.0		
L, R in-phase gain difference 5 (3)	DG ₅₃	L1 OUT, R1 OUT				C0	48							–1.0	0.0	+1.0		
L, R in-phase gain difference 6 (1)	DG ₆₁	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	a	–	A0	7F	60	60	60	7F	7F	48	–1.0	0.0	+1.0	dB	
L, R in-phase gain difference 6 (2)	DG ₆₂	Rin = 0.5 V _{rms} ,				↓	60							–1.0	0.0	+1.0		
L, R in-phase gain difference 6 (3)	DG ₆₃	L1 OUT, R1 OUT				E0	48							–1.0	0.0	+1.0		

–: Don't care.

Note See 7. MEASURING CIRCUIT.

(1) μ PC1853CT-01 Volume control, tone control block (3/3)

Parameter	Symbol	Test conditions	Switch mode ^{Note}			Subaddress data								MIN.	TYP.	MAX.	Unit		
			S1	S2	S3	00	01	02	03	04	05	06	07					08	
Muting attenuation 1	Mute 1	Lin = 0.5 V _{rms} , Rin = GND, L1 OUT	a	b	–	82	7F	60	60	60	7F	7F	7F	48	–80.0	–	–	dB	
Muting attenuation 2	Mute 2	Lin = GND, Rin = 0.5 V _{rms} , R1 OUT	b	a	–									–80.0	–	–	dB		
Muting attenuation 3	Mute 3	Lin = 0.5 V _{rms} , Rin = GND, L2 OUT	a	b	–	84								–80.0	–	–	dB		
Muting attenuation 4	Mute 4	Lin = GND, Rin = 0.5 V _{rms} , R2 OUT	b	a	–									–80.0	–	–	dB		
Muting attenuation 5	Mute 5	Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , L+R OUT	a	a	–	88								–80.0	–	–	dB		
Muting attenuation 6	Mute 6 (Rear)	Lin = 0.5 V _{rms} , Rin = GND, Rear OUT	a	b	–	90								–70.0	–	–	dB		
DC offset at muting mode (L1 OUT, R1 OUT)	V _{OS1}	No signal	b	b	–	80	7F	60	60	60	7F	7F	7F	48	–50	0	+50	mV	
DC offset at muting mode (L2 OUT, R2 OUT)	V _{OS2}					82									–50				
DC offset at muting mode (L+R OUT)	V _{OS3}					84									–50				
DC offset at muting mode (Rear OUT)	V _{OS4}					88									–50				
						90													

–: Don't care.

Note See 7. MEASURING CIRCUIT.

(2) μ PC1853CT-02 Volume control, tone control block (1/2)

Parameter	Symbol	Test conditions	Switch mode ^{Note}			Subaddress data								MIN.	TYP.	MAX.	Unit	
			S1	S2	S3	00	01	02	03	04	05	06	07					08
Volume attenuation 1 (1) L-ch	ATT _{VL11}	Lin = 0.5 V _{rms} ,	a	b	–	80	7F	7F	60	60	7F	7F	7F	48	–1.5	0.0	+1.5	dB
Volume attenuation 1 (2) L-ch	ATT _{VL12}	Rin = GND,						60							–25.0	–19.0	–13.0	dB
Volume attenuation 1 (3) L-ch	ATT _{VL13}	L1 OUT						40							–80.0	–	–	dB
Volume attenuation 1 (4) R-ch	ATT _{VR14}	Lin = GND,	a	b	–	80	7F	7F	60	60	7F	7F	7F	48	–1.5	0.0	+1.5	dB
Volume attenuation 1 (5) R-ch	ATT _{VR15}	Rin = 0.5 V _{rms} , R1 OUT						60							–25.0	–19.0	–13.0	dB
Volume attenuation 1 (6) R-ch	ATT _{VR16}							40							–80.0	–	–	dB
Volume attenuation 2 (1)	ATT _{VL21}	Lin = 0.5 V _{rms} , Rin = GND,	a	b	–	80	7F	7F	60	60	7F	7F	7F	48	–1.5	0.0	+1.5	dB
Volume attenuation 2 (2)	ATT _{VL22}	L2 OUT										60			–25.0	–19.0	–13.0	dB
Volume attenuation 2 (3)	ATT _{VL23}											40			–80.0	–	–	dB
L+R volume attenuation 1	ATT _{VLR1}	Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} ,	a	a	–	80	7F	7F	60	60	7F	7F	7F	48	–1.5	0.0	+1.5	dB
L+R volume attenuation 2	ATT _{VLR2}	L+R OUT										60			–25.0	–19.5	–13.0	dB
L+R volume attenuation 3	ATT _{VLR3}											40			–80.0	–	–	dB
Rear volume attenuation 1	ATT _{VRE1}	Lin = 0.5 V _{rms} , Rin = GND,	a	b	–	80	7F	7F	60	60	7F	7F	7F	48	8.5	10.0	11.5	dB
Rear volume attenuation 2	ATT _{VRE2}	Rear OUT										60			–15.0	–9.0	–3.0	dB
Low-band boost control	V _{BB}	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	b	–	80	7F	7F	7F	60	7F	7F	7F	48	7.0	10.0	13.0	dB
Low-band flat control	V _{BF}	Rin = GND, L1 OUT										60			–3.0	0.0	+3.0	dB
Low-band cut control	V _{BC}											41			–13.0	–10.0	–7.0	dB
High-band boost control	V _{TB}	f = 100 kHz, Lin = 0.5 V _{rms} ,	a	b	–	80	7F	7F	60	7F	7F	7F	7F	48	7.0	10.0	13.0	dB
High-band flat control	V _{TF}	Rin = GND, L1 OUT										60			–3.0	0.0	+3.0	dB
High-band cut control	V _{TC}											41			–13.0	–10.0	–7.0	dB
L, R in-phase gain difference 1 (1)	DG ₁₁	Lin = GND, Rin = 0.5 V _{rms} ,	b	a	–	80	7F	7F	60	60	7F	7F	7F	48	–1.0	0.0	+1.0	dB
L, R in-phase gain difference 1 (2)	DG ₁₂	L1 OUT, R1 OUT						60	60						–1.5	0.0	+1.5	dB
L, R in-phase gain difference 2 (1)	DG ₂₁	Lin = GND, Rin = 0.5 V _{rms} ,	b	a	–	80	7F	7F	60	60	7F	7F	7F	48	–1.0	0.0	+1.0	dB
L, R in-phase gain difference 2 (2)	DG ₂₂	L2 OUT, R2 OUT										60			–1.0	0.0	+1.0	dB

–: Don't care.

Note See 7. MEASURING CIRCUIT.

(2) μPC1853CT-02 Volume control, tone control block (2/2)

Parameter	Symbol	Test conditions	Switch mode ^{Note}			Subaddress data								MIN.	TYP.	MAX.	Unit	
			S1	S2	S3	00	01	02	03	04	05	06	07					08
L, R in-phase gain difference 3 (1)	DG ₃₁	f = 100 Hz, Lin = 0.5 V _{rms} ,	a	a	-	80	7F	7F	7F	60	7F	7F	7F	48	-1.0	0.0	+1.0	dB
L, R in-phase gain difference 3 (2)	DG ₃₂	Rin = 0.5 V _{rms} ,							60					-1.0	0.0	+1.0	dB	
L, R in-phase gain difference 3 (3)	DG ₃₃	L1 OUT, R1 OUT							41					-1.0	0.0	+1.0	dB	
L, R in-phase gain difference 4 (1)	DG ₄₁	f = 10 kHz, Lin = 0.5 V _{rms} ,	a	a	-	80	7F	7F	60	7F	7F	7F	48	-1.0	0.0	+1.0	dB	
L, R in-phase gain difference 4 (2)	DG ₄₂	Rin = 0.5 V _{rms} ,							60					-1.0	0.0	+1.0	dB	
L, R in-phase gain difference 4 (3)	DG ₄₃	L1 OUT, R1 OUT							41					-1.0	0.0	+1.0	dB	
Muting attenuation 1	Mute 1	Lin = 0.5 V _{rms} , Rin = GND, L2 OUT	a	b	-	84	7F	7F	60	60	7F	7F	48	-80.0	-	-	dB	
Muting attenuation 2	Mute 2	Lin = GND, Rin = 0.5 V _{rms} , R2 OUT	b	a	-									-80.0	-	-	dB	
Muting attenuation 3	Mute 3	Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , L+R OUT	a	a	-	88								-80.0	-	-	dB	
Muting attenuation 4	Mute 4 (Rear)	Lin = 0.5 V _{rms} , Rin = GND, Rear OUT	a	b	-	90								-70.0	-	-	dB	
DC offset at muting mode (L1 OUT, R1 OUT)	V _{OS1}	No signal	b	b	-	80 ↓ 82	7F	7F	60	60	7F	7F	48	-50	0	+50	mV	
DC offset at muting mode (L2 OUT, R2 OUT)	V _{OS2}					80 ↓ 84								-50	0	+50	mV	
DC offset at muting mode (L+R OUT)	V _{OS3}					80 ↓ 88								-50	0	+50	mV	
DC offset at muting mode (Rear OUT)	V _{OS4}					80 ↓ 90								-50	0	+50	mV	

-: Don't care.

Note See 7. MEASURING CIRCUIT.

Matrix surround block (1/2)

Parameter	Symbol	Test conditions	Switch mode ^{Note1}			Subaddress data								MIN.	TYP.	MAX.	Unit	
			S1	S2	S3	00	01	02	03	04	05	06	07					08
In-phase gain Movie mode 1 ^{Note2}	G _{MOV1}	f = 1 kHz, Lin = 0.5 V _{rms} , Rin = GND, L1 OUT	a	b	–	80	7F	60	60	60	7F	7F	7F	C8	3.0	7.0	11.0	dB
In-phase gain Movie mode 2 ^{Note2}	G _{MOV2}	f = 1 kHz, Lin = 0.5 V _{rms} , Rin = GND, R1 OUT												0.0	4.0	8.0	dB	
In-phase gain Music mode 1 ^{Note2}	G _{MUS1}	f = 1 kHz, Lin = 0.5 V _{rms} , Rin = GND, L1 OUT												E8	3.5	5.5	7.5	dB
In-phase gain Music mode 2 ^{Note2}	G _{MUS2}	f = 1 kHz, Lin = 0.5 V _{rms} , Rin = GND, R1 OUT												–2.5	–0.5	+1.5	dB	
In-phase gain Simulated mode (L-ch) 1 ^{Note2}	G _{SIML1}	f = 250 Hz, Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , L1 OUT	a	a	–									D8	–0.5	+3.5	+6.5	dB
In-phase gain Simulated mode (L-ch) 2 ^{Note2}	G _{SIML2}	f = 1 kHz, Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , L1 OUT												–	–3.0	+4.5	dB	
In-phase gain Simulated mode (L-ch) 3 ^{Note2}	G _{SIML3}	f = 4 kHz, Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , L1 OUT												2.0	6.0	10.0	dB	
In-phase gain Simulated mode (R-ch) 1 ^{Note2}	G _{SIMR1}	f = 250 Hz, Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , R1 OUT												D8	–	–5.5	–1.0	dB
In-phase gain Simulated mode (R-ch) 2 ^{Note2}	G _{SIMR2}	f = 1 kHz, Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , R1 OUT												0.0	3.0	6.0	dB	
In-phase gain Simulated mode (R-ch) 3 ^{Note2}	G _{SIMR3}	f = 4 kHz, Lin = 0.5 V _{rms} , Rin = 0.5 V _{rms} , R1 OUT												–	–7.0	+5.0	dB	

–: Don't care.

Note 1. See 7. MEASURING CIRCUIT.

2. See 4.3 Surround Function about setting of surround mode.

Remark The values are common to both the μ PC1853CT-01 and μ PC1853CT-02.

Matrix surround block (2/2)

Parameter	Symbol	Test conditions	Switch mode ^{Note}			Subaddress data								MIN.	TYP.	MAX.	Unit	
			S1	S2	S3	00	01	02	03	04	05	06	07					08
Output noise	NO1	Lin = GND, Rin = GND, Surround: OFF, DIN-AUDIO filter, L1 OUT, R1 OUT, L2 OUT, R2 OUT, L+R OUT, Rear OUT	b	b	–	80	7F	60	60	60	7F	7F	7F	48	–	25	50	μV_{rms}
Crosstalk 1	CT1	Lin = 0.5 V_{rms} , Rin = GND, 0 dB: 0.5 V_{rms}	a	b	–	80	7F	60	60	60	7F	7F	7F	48	–	–80	–70	dB
Crosstalk 2	CT2	Lin = GND, Rin = 0.5 V_{rms} , 0 dB: 0.5 V_{rms}	b	a	–										–	–80	–70	dB
Inter-mode offset	V_{OSM}	No signal. At surround mode switching.	b	b	–	80	7F	60	60	60	7F	7F	7F	xF	–50	0	+50	mV

–: Don't care.

Note See 7. MEASURING CIRCUIT.

Remark The values are common to both the $\mu PC1853CT-01$ and $\mu PC1853CT-02$.

ELECTRICAL CHARACTERISTICS MEASUREMENT LIST

Set subaddress data as shown in **4.2 Initialization** unless otherwise specified.

General (1/1)

Parameter	Symbol	Test conditions	Subaddress	Data									
				D7	D6	D5	D4	D3	D2	D1	D0		
Supply current	I _{CC}	Current flowing to pin 15. No signal											
Maximum input voltage 1	V _{OM1}	Input signal level of pins 13, 14, 16 and 17. Distortion rate of pins 13, 14, 16 and 17: 1 % Pins 26 and 27: Input SIN wave (1 kHz, 2.8 V _{rms}).											
Maximum input voltage 2	V _{OM2}	Input signal level of pin 11. Distortion rate of pin 11: 1 % Pin 26: Input SIN wave (1 kHz, 2.8 V _{rms}). Pin 27: No signal											
Distortion rate (L-ch)	THD _L	Distortion rate of pins 14 and 17. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).											
Distortion rate (R-ch)	THD _R	Distortion rate of pins 13 and 16. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V _{rms}).											

Remark The methods are common to both the μ PC1853CT-01 and μ PC1853CT-02.

(1) μPC1853CT-01 Volume control, tone control block (1/9)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
Volume attenuation 1 (1)	ATT _{VL11}	Volume attenuation = $20 \log \frac{\text{L1 output}}{\text{L input}}$	01	0	1	1	1	1	1	1	1	1
Volume attenuation 1 (2)	ATT _{VL12}	L1 output: Output signal level of pin 14. L input: Input signal level of pin 26.		0	1	1	0	0	0	0	0	0
Volume attenuation 1 (3)	ATT _{VL13}	Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).		0	1	0	0	0	0	0	0	0
Volume attenuation 2 (1)	ATT _{VL21}	Volume attenuation = $20 \log \frac{\text{L2 output}}{\text{L input}}$	06	0	1	1	1	1	1	1	1	1
Volume attenuation 2 (2)	ATT _{VL22}	L2 output: Output signal level of pin 17. L input: Input signal level of pin 26.		0	1	1	0	0	0	0	0	0
Volume attenuation 2 (3)	ATT _{VL23}	Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).		0	1	0	0	0	0	0	0	0
L+R volume attenuation 1	ATT _{VLR1}	L+R volume attenuation = $20 \log \frac{\text{L+R output}}{\text{L, R input}}$	05	0	1	1	1	1	1	1	1	1
L+R volume attenuation 2	ATT _{VLR2}	L+R output: Output signal level of pin 12. L, R input: Input signal level of pin 26 or 27.		0	1	1	0	0	0	0	0	0
L+R volume attenuation 3	ATT _{VLR3}	Pin 26, 27: Input SIN wave (1 kHz, 0.5 V _{rms}).		0	1	0	0	0	0	0	0	0
Rear volume attenuation 1	ATT _{VRE1}	Rear volume attenuation = $20 \log \frac{\text{Rear output}}{\text{L input}}$ Rear output: Output signal level of pin 11.	07	0	1	1	1	1	1	1	1	1
Rear volume attenuation 2	ATT _{VRE2}	L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).		0	1	1	0	0	0	0	0	0

(1) μPC1853CT-01 Volume control, tone control block (2/9)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
Balance attenuation (L-ch) 1 (1)	ATT _{BL11}	$\text{Balance attenuation} = 20 \log \frac{\text{L1 output}}{\text{L input}}$ L1 output: Output signal level of pin 14. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	02	0	1	0	0	0	0	0	0	1
Balance attenuation (L-ch) 1 (2)	ATT _{BL12}		02	0	1	1	0	0	0	0	0	0
Balance attenuation (L-ch) 1 (3)	ATT _{BL13}		02	0	1	1	1	1	1	1	1	1
Balance attenuation (R-ch) 1 (1)	ATT _{BR11}	$\text{Balance attenuation} = 20 \log \frac{\text{R1 output}}{\text{R input}}$ R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V _{rms}).	02	0	1	0	0	0	0	0	0	1
Balance attenuation (R-ch) 1 (2)	ATT _{BR12}		02	0	1	1	0	0	0	0	0	0
Balance attenuation (R-ch) 1 (3)	ATT _{BR13}		02	0	1	1	1	1	1	1	1	1
Low-band boost control	V _{BB}	$\text{Bass response} = 20 \log \frac{\text{L1 output}}{\text{L input}}$ L1 output: Output signal level of pin 14. L input: Input signal level of pin 26. Pin 26: Input SIN wave (100 Hz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	03	0	1	1	1	1	1	1	1	1
Low-band flat control	V _{BF}		03	0	1	1	0	0	0	0	0	0
Low-band cut control	V _{BC}		03	0	1	0	0	0	0	0	0	0
Low-band boost control (6 dB) 1	V _{B6dB1}	$\text{Bass response} = 20 \log \frac{V_{\text{BON}}}{V_{\text{BOFF}}}$ V _{BON} : Output signal level of pin 14 (Low boost: ON). V _{BOFF} : Output signal level of pin 14 (Low boost: OFF). Pin 26: Input SIN wave (100 Hz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	00	1	0	0	0	0	0	0	0	0
			01	0	1	1	1	1	1	1	1	1
Low-band boost control (6 dB) 2	V _{B6dB2}	$\text{Bass response} = 20 \log \frac{V_{\text{BON}}}{V_{\text{BOFF}}}$ V _{BON} : Output signal level of pin 14 (Low boost: ON). V _{BOFF} : Output signal level of pin 14 (Low boost: OFF). Pin 26: Input SIN wave (100 Hz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	00	1	0	0	0	0	0	0	0	0
			01	0	1	1	0	0	0	0	0	0

(1) μPC1853CT-01 Volume control, tone control block (3/9)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
Low-band boost control (6 dB) 3	V _{B6dB3}	Bass response = $20 \log \frac{V_{BON}}{V_{BOFF}}$ V _{BON} : Output signal level of pin 14 (Low boost: ON). V _{BOFF} : Output signal level of pin 14 (Low boost: OFF). Pin 26: Input SIN wave (100 Hz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	00	1	0 ↓ 1	0	0	0	0	0	0	0
			01	0	1	0	1	0	0	0	0	0
Low-band boost control (3 dB) 1	V _{B3dB1}	Bass response = $20 \log \frac{V_{BON}}{V_{BOFF}}$ V _{BON} : Output signal level of pin 14 (Low boost: ON). V _{BOFF} : Output signal level of pin 14 (Low boost: OFF).	00	1	0 ↓ 1	1	0	0	0	0	0	0
			01	0	1	1	1	1	1	1	1	1
Low-band boost control (3 dB) 2	V _{B3dB2}	V _{BOFF} : Output signal level of pin 14 (Low boost: OFF). Pin 26: Input SIN wave (100 Hz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	00	1	0 ↓ 1	1	0	0	0	0	0	0
			01	0	1	1	0	0	0	0	0	0
Low-band boost control (3 dB) 3	V _{B3dB3}		00	1	0 ↓ 1	1	0	0	0	0	0	0
			01	0	1	0	1	0	0	0	0	0
High-band boost control	V _{TB}	Treble response = $20 \log \frac{L1 \text{ output}}{L \text{ input}}$ L1 output: Output signal level of pin 14. L input: Input signal level of pin 26. Pin 26: Input SIN wave (10 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	04	0	1	1	1	1	1	1	1	1
High-band flat control	V _{TF}			0	1	1	0	0	0	0	0	
High-band cut control	V _{TC}			0	1	0	0	0	0	0	0	1

(1) μ PC1853CT-01 Volume control, tone control block (4/9)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
L, R in-phase gain difference 1 (1)	DG ₁₁	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - \text{ATT}_{\text{VL11}}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. ATT_{VL11}: Gain of the Volume attenuation 1 (1). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>	01	0	1	1	1	1	1	1	1	1
L, R in-phase gain difference 1 (2)	DG ₁₂	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - \text{ATT}_{\text{VL12}}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. ATT_{VL12}: Gain of the Volume attenuation 1 (2). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>		0	1	1	0	0	0	0	0	0
L, R in-phase gain difference 2 (1)	DG ₂₁	$\text{Channel to channel error} = 20 \log \frac{\text{R2 output}}{\text{R input}} - \text{ATT}_{\text{VL21}}$ <p>R2 output: Output signal level of pin 16. R input: Input signal level of pin 27. ATT_{VL21}: Gain of the Volume attenuation 2 (1). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>	06	0	1	1	1	1	1	1	1	1
L, R in-phase gain difference 2 (2)	DG ₂₂	$\text{Channel to channel error} = 20 \log \frac{\text{R2 output}}{\text{R input}} - \text{ATT}_{\text{VL22}}$ <p>R2 output: Output signal level of pin 16. R input: Input signal level of pin 27. ATT_{VL22}: Gain of the Volume attenuation 2 (2). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>		0	1	1	0	0	0	0	0	0

(1) μPC1853CT-01 Volume control, tone control block (5/9)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
L, R in-phase gain difference 3 (1)	DG ₃₁	Channel to channel error = $20 \log \frac{R1 \text{ output}}{R \text{ input}} - V_{BB}$ R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V _{BB} : Gain of the Low-band boost control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V _{rms}).	03	0	1	1	1	1	1	1	1	1
L, R in-phase gain difference 3 (2)	DG ₃₂	Channel to channel error = $20 \log \frac{R1 \text{ output}}{R \text{ input}} - V_{BF}$ R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V _{BF} : Gain of the Low-band flat control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V _{rms}).		0	1	1	0	0	0	0	0	0
L, R in-phase gain difference 3 (3)	DG ₃₃	Channel to channel error = $20 \log \frac{R1 \text{ output}}{R \text{ input}} - V_{BC}$ R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V _{BC} : Gain of the Low-band cut control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V _{rms}).		0	1	0	0	0	0	0	0	1
L, R in-phase gain difference 4 (1)	DG ₄₁	Channel to channel error = $20 \log \frac{R1 \text{ output}}{R \text{ input}} - V_{TB}$ R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V _{TB} : Gain of the High-band boost control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (10 kHz, 0.5 V _{rms}).	05	0	1	1	1	1	1	1	1	1

(1) μ PC1853CT-01 Volume control, tone control block (6/9)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
L, R in-phase gain difference 4 (2)	DG42	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{TF}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{TF}: Gain of the High-band flat control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (10 kHz, 0.5 V_{rms}).</p>	05	0	1	1	0	0	0	0	0	0
L, R in-phase gain difference 4 (3)	DG43	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{TC}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{TC}: Gain of the High-band cut control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (10 kHz, 0.5 V_{rms}).</p>		0	1	0	0	0	0	0	0	1
L, R in-phase gain difference 5 (1)	DG51	$\text{Channel to channel error} = 20 \log \frac{V_{BON}}{V_{BOFF}} - V_{B6dB1}$ <p>V_{BON} : Output signal level of pin 13 (Low boost: ON). V_{BOFF} : Output signal level of pin 13 (Low boost: OFF). V_{B6dB1}: Gain of the Low-band boost control (6 dB) 1. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V_{rms}).</p>	00	1	0	0	0	0	0	0	0	0
					↓							
			01	0	1	1	1	1	1	1	1	1
L, R in-phase gain difference 5 (2)	DG52	$\text{Channel to channel error} = 20 \log \frac{V_{BON}}{V_{BOFF}} - V_{B6dB2}$ <p>V_{BON} : Output signal level of pin 13 (Low boost: ON). V_{BOFF} : Output signal level of pin 13 (Low boost: OFF). V_{B6dB2}: Gain of the Low-band boost control (6 dB) 2. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V_{rms}).</p>	00	1	0	0	0	0	0	0	0	0
					↓							
			01	0	1	1	0	0	0	0	0	0

(1) μPC1853CT-01 Volume control, tone control block (7/9)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
L, R in-phase gain difference 5 (3)	DG ₅₃	Channel to channel error = $20 \log \frac{V_{BON}}{V_{BOFF}} - V_{B6dB3}$ V_{BON} : Output signal level of pin 13 (Low boost: ON). V_{BOFF} : Output signal level of pin 13 (Low boost: OFF). V_{B6dB3} : Gain of the Low-band boost control (6 dB) 3. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V _{rms}).	00	1	0	0	0	0	0	0	0
			01	0	1	0	0	1	0	0	0
L, R in-phase gain difference 6 (1)	DG ₆₁	Channel to channel error = $20 \log \frac{V_{BON}}{V_{BOFF}} - V_{B3dB1}$ V_{BON} : Output signal level of pin 13 (Low boost: ON). V_{BOFF} : Output signal level of pin 13 (Low boost: OFF). V_{B3dB1} : Gain of the Low-band boost control (3 dB) 1. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V _{rms}).	00	1	0	1	0	0	0	0	0
			01	0	1	1	1	1	1	1	1
L, R in-phase gain difference 6 (2)	DG ₆₂	Channel to channel error = $20 \log \frac{V_{BON}}{V_{BOFF}} - V_{B3dB2}$ V_{BON} : Output signal level of pin 13 (Low boost: ON). V_{BOFF} : Output signal level of pin 13 (Low boost: OFF). V_{B3dB2} : Gain of the Low-band boost control (3 dB) 2. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V _{rms}).	00	1	0	1	0	0	0	0	0
			01	0	1	1	0	0	0	0	0
L, R in-phase gain difference 6 (3)	DG ₆₃	Channel to channel error = $20 \log \frac{V_{BON}}{V_{BOFF}} - V_{B3dB3}$ V_{BON} : Output signal level of pin 13 (Low boost: ON). V_{BOFF} : Output signal level of pin 13 (Low boost: OFF). V_{B3dB3} : Gain of the Low-band boost control (3 dB) 3. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V _{rms}).	00	1	0	1	0	0	0	0	0
			01	0	1	0	0	1	0	0	0

(1) μPC1853CT-01 Volume control, tone control block (8/9)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
Muting attenuation 1	Mute 1	$\text{Mute 1} = 20 \log \frac{\text{L1 output}}{\text{L input}}$ <p>L1 output: Output signal level of pin 14. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V_{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).</p>	00	1	0	0	0	0	0	1	0
Muting attenuation 2	Mute 2	$\text{Mute 2} = 20 \log \frac{\text{R1 output}}{\text{R input}}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>									
Muting attenuation 3	Mute 3	$\text{Mute 3} = 20 \log \frac{\text{L2 output}}{\text{L input}}$ <p>L2 output: Output signal level of pin 17. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V_{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).</p>		1	0	0	0	0	1	0	0
Muting attenuation 4	Mute 4	$\text{Mute 4} = 20 \log \frac{\text{R2 output}}{\text{R input}}$ <p>R2 output: Output signal level of pin 16. R input: Input signal level of pin 27. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>									

(1) μPC1853CT-01 Volume control, tone control block (9/9)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
Muting attenuation 5	Mute 5	$\text{Mute 5} = 20 \log \frac{\text{L+R output}}{\text{L, R input}}$ <p>L+R output: Output signal level of pin 12. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>	00	1	0	0	0	1	0	0	0
Muting attenuation 6	Mute 6 (Rear)	$\text{Mute 6} = 20 \log \frac{\text{Rear output}}{\text{L input}}$ <p>Rear output: Output signal level of pin 11. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V_{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).</p>		1	0	0	1	0	0	0	0
DC offset at muting mode (L1 OUT, R1 OUT)	V _{OS1}	$V_{OS1} = V_1 - V_0$ <p>V₁: DC voltage of pin 14 or 13 (Main output mute: ON). V₀: DC voltage of pin 14 or 13 (Main output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>	00	1	0	0	0	0	0	0	0
DC offset at muting mode (L2 OUT, R2 OUT)	V _{OS2}	$V_{OS2} = V_1 - V_0$ <p>V₁: DC voltage of pin 17 or 16 (Audio output mute: ON). V₀: DC voltage of pin 17 or 16 (Audio output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>		1	0	0	0	0	0	0	0
DC offset at muting mode (L+R OUT)	V _{OS3}	$V_{OS3} = V_1 - V_0$ <p>V₁: DC voltage of pin 12 (L+R output mute: ON). V₀: DC voltage of pin 12 (L+R output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>		1	0	0	0	0	0	0	0
DC offset at muting mode (Rear OUT)	V _{OS4}	$V_{OS4} = V_1 - V_0$ <p>V₁: DC voltage of pin 11 (Rear output mute: ON). V₀: DC voltage of pin 11 (Rear output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>		1	0	0	0	0	0	0	0

(2) μPC1853CT-02 Volume control, tone control block (1/6)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
Volume attenuation 1 (1) L-ch	ATT _{VL11}	$\text{Volume attenuation} = 20 \log \frac{\text{L1 output}}{\text{L input}}$ L1 output: Output signal level of pin 14. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	02	0	1	1	1	1	1	1	1	1
Volume attenuation 1 (2) L-ch	ATT _{VL12}			0	1	1	0	0	0	0	0	
Volume attenuation 1 (3) L-ch	ATT _{VL13}			0	1	0	0	0	0	0	0	
Volume attenuation 1 (4) R-ch	ATT _{VR14}	$\text{Volume attenuation} = 20 \log \frac{\text{R1 output}}{\text{R input}}$ R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V _{rms}).	01	0	1	1	1	1	1	1	1	
Volume attenuation 1 (5) R-ch	ATT _{VR15}			0	1	1	0	0	0	0	0	
Volume attenuation 1 (6) R-ch	ATT _{VR16}			0	1	0	0	0	0	0	0	
Volume attenuation 2 (1)	ATT _{VL21}	$\text{Volume attenuation} = 20 \log \frac{\text{L2 output}}{\text{L input}}$ L2 output: Output signal level of pin 17. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	06	0	1	1	1	1	1	1	1	
Volume attenuation 2 (2)	ATT _{VL22}			0	1	1	0	0	0	0	0	
Volume attenuation 2 (3)	ATT _{VL23}			0	1	0	0	0	0	0	0	
L+R volume attenuation 1	ATT _{VLR1}	$\text{L+R volume attenuation} = 20 \log \frac{\text{L+R output}}{\text{L, R input}}$ L+R output: Output signal level of pin 12. L, R input: Input signal level of pin 26 or 27. Pin 26, 27: Input SIN wave (1 kHz, 0.5 V _{rms}).	05	0	1	1	1	1	1	1	1	
L+R volume attenuation 2	ATT _{VLR2}			0	1	1	0	0	0	0	0	
L+R volume attenuation 3	ATT _{VLR3}			0	1	0	0	0	0	0	0	

(2) μPC1853CT-02 Volume control, tone control block (2/6)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
Rear volume attenuation 1	ATT _{VRE1}	Rear volume attenuation = $20 \log \frac{\text{Rear output}}{\text{L input}}$ Rear output: Output signal level of pin 11.	07	0	1	1	1	1	1	1	1	1
Rear volume attenuation 2	ATT _{VRE2}	L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).		0	1	1	0	0	0	0	0	0
Low-band boost control	V _{BB}	Bass response = $20 \log \frac{\text{L1 output}}{\text{L input}}$ L1 output: Output signal level of pin 14.	03	0	1	1	1	1	1	1	1	1
Low-band flat control	V _{BF}	L input: Input signal level of pin 26.		0	1	1	0	0	0	0	0	0
Low-band cut control	V _{BC}	Pin 26: Input SIN wave (100 Hz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).		0	1	0	0	0	0	0	0	1
High-band boost control	V _{TB}	Treble response = $20 \log \frac{\text{L1 output}}{\text{L input}}$ L1 output: Output signal level of pin 14.	04	0	1	1	1	1	1	1	1	1
High-band flat control	V _{TF}	L input: Input signal level of pin 26.		0	1	1	0	0	0	0	0	0
High-band cut control	V _{TC}	Pin 26: Input SIN wave (10 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).		0	1	0	0	0	0	0	0	1
L, R in-phase gain difference 1 (1)	DG ₁₁	Channel to channel error = $20 \log \frac{\text{R1 output}}{\text{R input}} - \text{ATT}_{\text{VL11}}$ R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. ATT _{VL11} : Gain of the Volume attenuation 1 (1). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V _{rms}). Same method about L-ch input/output signal	01 02	0	1	1	1	1	1	1	1	1

(2) μ PC1853CT-02 Volume control, tone control block (3/6)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
L, R in-phase gain difference 1 (2)	DG ₁₂	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - \text{ATT}_{\text{VL12}}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. ATT_{VL12}: Gain of the Volume attenuation 1 (2). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}). Same method about L-ch input/output signal</p>	01 02	0	1	1	0	0	0	0	0
L, R in-phase gain difference 2 (1)	DG ₂₁	$\text{Channel to channel error} = 20 \log \frac{\text{R2 output}}{\text{R input}} - \text{ATT}_{\text{VL21}}$ <p>R2 output: Output signal level of pin 16. R input: Input signal level of pin 27. ATT_{VL21}: Gain of the Volume attenuation 2 (1). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>	06	0	1	1	1	1	1	1	1
L, R in-phase gain difference 2 (2)	DG ₂₂	$\text{Channel to channel error} = 20 \log \frac{\text{R2 output}}{\text{R input}} - \text{ATT}_{\text{VL22}}$ <p>R2 output: Output signal level of pin 16. R input: Input signal level of pin 27. ATT_{VL22}: Gain of the Volume attenuation 2 (2). Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>		0	1	1	0	0	0	0	0
L, R in-phase gain difference 3 (1)	DG ₃₁	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{\text{BB}}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{BB}: Gain of the Low-band boost control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V_{rms}).</p>	03	0	1	1	1	1	1	1	1

(2) μPC1853CT-02 Volume control, tone control block (4/6)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
L, R in-phase gain difference 3 (2)	DG ₃₂	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{BF}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{BF}: Gain of the Low-band flat control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V_{rms}).</p>	03	0	1	1	0	0	0	0	0
L, R in-phase gain difference 3 (3)	DG ₃₃	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{BC}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{BC}: Gain of the Low-band cut control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (100 Hz, 0.5 V_{rms}).</p>		0	1	0	0	0	0	0	1
L, R in-phase gain difference 4 (1)	DG ₄₁	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{TB}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{TB}: Gain of the High-band boost control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (10 kHz, 0.5 V_{rms}).</p>	05	0	1	1	1	1	1	1	1
L, R in-phase gain difference 4 (2)	DG ₄₂	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{TF}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{TF}: Gain of the High-band flat control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (10 kHz, 0.5 V_{rms}).</p>		0	1	1	0	0	0	0	0

(2) μ PC1853CT-02 Volume control, tone control block (5/6)

Parameter	Symbol	Test conditions	Subaddress	Data								
				D7	D6	D5	D4	D3	D2	D1	D0	
L, R in-phase gain difference 4 (3)	DG ₄₃	$\text{Channel to channel error} = 20 \log \frac{\text{R1 output}}{\text{R input}} - V_{TC}$ <p>R1 output: Output signal level of pin 13. R input: Input signal level of pin 27. V_{TC}: Gain of the High-band cut control. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (10 kHz, 0.5 V_{rms}).</p>	05	0	1	0	0	0	0	0	0	1
Muting attenuation 1	Mute 1	$\text{Mute 1} = 20 \log \frac{\text{L2 output}}{\text{L input}}$ <p>L2 output: Output signal level of pin 17. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V_{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).</p>	00	1	0	0	0	0	1	0	0	
Muting attenuation 2	Mute 2	$\text{Mute 2} = 20 \log \frac{\text{R2 output}}{\text{R input}}$ <p>R2 output: Output signal level of pin 16. R input: Input signal level of pin 27. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>		1	0	0	0	1	0	0	0	
Muting attenuation 3	Mute 3	$\text{Mute 3} = 20 \log \frac{\text{L+R output}}{\text{L, R input}}$ <p>L+R output: Output signal level of pin 12. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>		1	0	0	0	1	0	0	0	

(2) μPC1853CT-02 Volume control, tone control block (6/6)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
Muting attenuation 4	Mute 4 (Rear)	$\text{Mute 4} = 20 \log \frac{\text{Rear output}}{\text{L input}}$ <p>Rear output : Output signal level of pin 11. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V_{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).</p>	00	1	0	0	1	0	0	0	0
DC offset at muting mode (L1OUT, R1 OUT)	V _{OS1}	$V_{OS1} = V_1 - V_0$ <p>V₁: DC voltage of pin 14 or 13 (Main output mute: ON). V₀: DC voltage of pin 14 or 13 (Main output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>	00	1	0	0	0	0	0	0	0
DC offset at muting mode (L2 OUT, R2 OUT)	V _{OS2}	$V_{OS2} = V_1 - V_0$ <p>V₁: DC voltage of pin 17 or 16 (Audio output mute: ON). V₀: DC voltage of pin 17 or 16 (Audio output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>		1	0	0	0	0	0	0	0
DC offset at muting mode (L+R OUT)	V _{OS3}	$V_{OS3} = V_1 - V_0$ <p>V₁: DC voltage of pin 12 (L+R output mute: ON). V₀: DC voltage of pin 12 (L+R output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>		1	0	0	0	0	0	0	0
DC offset at muting mode (Rear OUT)	V _{OS4}	$V_{OS4} = V_1 - V_0$ <p>V₁: DC voltage of pin 11 (Rear output mute: ON). V₀: DC voltage of pin 11 (Rear output mute: OFF). Pins 26 and 27: Connect to GND with an input coupling capacitor.</p>		1	0	0	0	0	0	0	0

Matrix surround block (1/3)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
In-phase gain Movie mode 1	G _{MOV1}	Response = $20 \log \frac{L1, R1 \text{ output}}{L \text{ input}}$ L1, R1 output: Output signal level of pin 14 or 13. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	08	1	1	0	0	1	0	0	0
In-phase gain Movie mode 2	G _{MOV2}	L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).									
In-phase gain Music mode 1	G _{MUS1}	Response = $20 \log \frac{L1, R1 \text{ output}}{L \text{ input}}$ L1, R1 output: Output signal level of pin 14 or 13. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).	08	1	1	1	0	1	0	0	0
In-phase gain Music mode 2	G _{MUS2}	L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V _{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).									
In-phase gain Simulated mode (L-ch) 1	G _{SIML1}	Response = $20 \log \frac{L1 \text{ output}}{L, R \text{ input}}$ L1 output: Output signal level of pin 14. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (250 Hz, 0.5 V _{rms}).	08	1	1	0	1	1	0	0	0
In-phase gain Simulated mode (L-ch) 2	G _{SIML2}	Response = $20 \log \frac{L1 \text{ output}}{L, R \text{ input}}$ L1 output: Output signal level of pin 14. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (1 kHz, 0.5 V _{rms}).									
In-phase gain Simulated mode (L-ch) 3	G _{SIML3}	Response = $20 \log \frac{L1 \text{ output}}{L, R \text{ input}}$ L1 output: Output signal level of pin 14. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (4 kHz, 0.5 V _{rms}).									

Remark The methods are common to both the μ PC1853CT-01 and μ PC1853CT-02.

Matrix surround block (2/3)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
In-phase gain Simulated mode (R-ch) 1	G _{SIMR1}	$\text{Response} = 20 \log \frac{\text{R1 output}}{\text{L, R input}}$ <p>R1 output: Output signal level of pin 13. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (250 Hz, 0.5 V_{rms}).</p>	08	1	1	0	1	1	0	0	0
In-phase gain Simulated mode (R-ch) 2	G _{SIMR2}	$\text{Response} = 20 \log \frac{\text{R1 output}}{\text{L, R input}}$ <p>R1 output: Output signal level of pin 13. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>									
In-phase gain Simulated mode (R-ch) 3	G _{SIMR3}	$\text{Response} = 20 \log \frac{\text{R1 output}}{\text{L, R input}}$ <p>R1 output: Output signal level of pin 13. L, R input: Input signal level of pin 26 or 27. Pins 26 and 27: Input SIN wave (4 kHz, 0.5 V_{rms}).</p>									
Output noise	NO1	<p>NO1: Output noise voltage of pins 11, 12, 13, 14, 16 and 17. Pins 26 and 27: Connect to GND with an input coupling capacitor. Filter of noise meter: DIN-AUDIO filter</p>									
Crosstalk 1	CT1	$\text{Crosstalk} = 20 \log \frac{\text{R output}}{\text{L input}}$ <p>R output: Output signal level of pin 13 or 16. L input: Input signal level of pin 26. Pin 26: Input SIN wave (1 kHz, 0.5 V_{rms}). Pin 27: No signal (Connect to GND with an input coupling capacitor).</p>									

Remark The methods are common to both the μPC1853CT-01 and μPC1853CT-02.

Matrix surround block (3/3)

Parameter	Symbol	Test conditions	Subaddress	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
Crosstalk 2	CT2	$\text{Crosstalk} = 20 \log \frac{\text{L output}}{\text{R input}}$ <p>L output: Output signal level of pin 14 or 17. R input: Input signal level of pin 27. Pin 26: No signal (Connect to GND with an input coupling capacitor). Pin 27: Input SIN wave (1 kHz, 0.5 V_{rms}).</p>									
Inter-mode offset	V _{OSM}	No signal. At surround mode switching. ^{Note}	08	×	1	×	×	1	1	1	1

Note See 4.3 Surround Function.

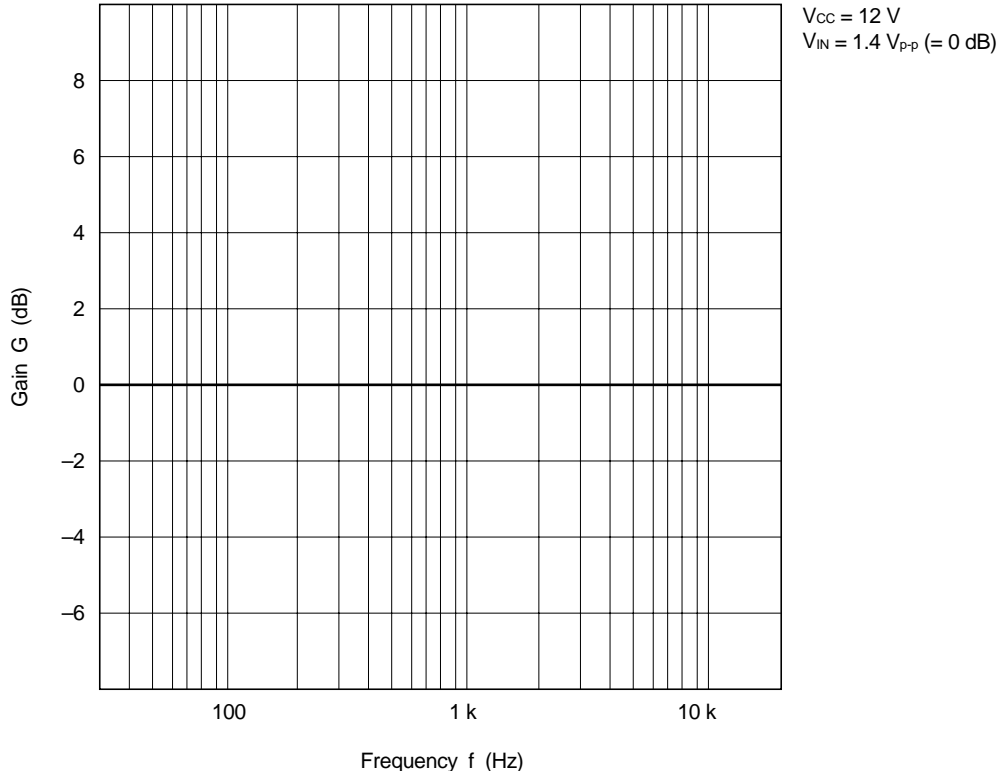
Remark The methods are common to both the μPC1853CT-01 and μPC1853CT-02.

6. CHARACTERISTIC CURVES

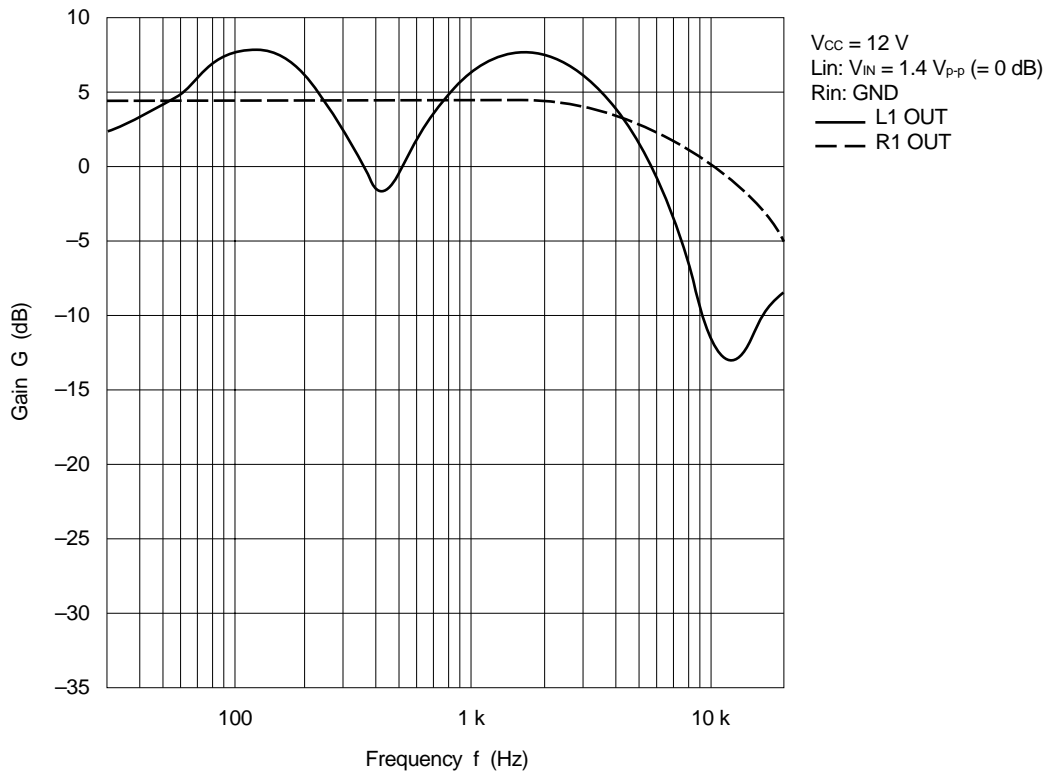
About surround mode, see 4.3 Surround Function.

6.1 Frequency Response Characteristics in Each Mode

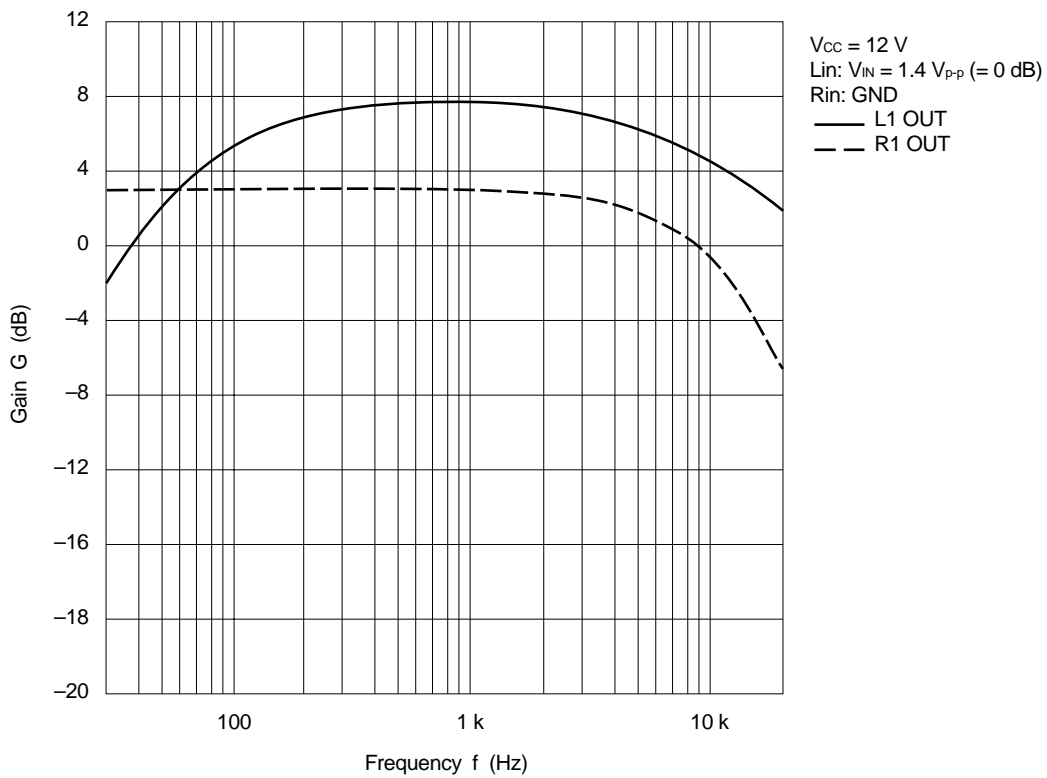
(1) OFF mode (L-channel, R-channel)



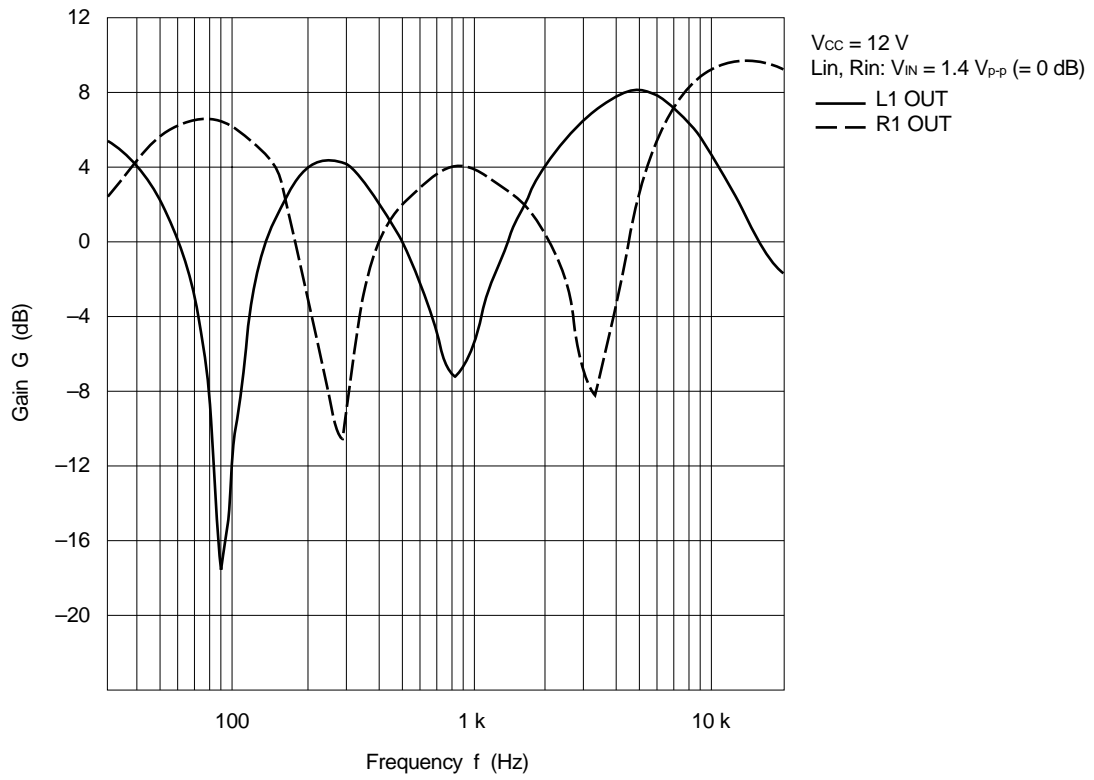
(2) Movie Mode



(3) Music Mode

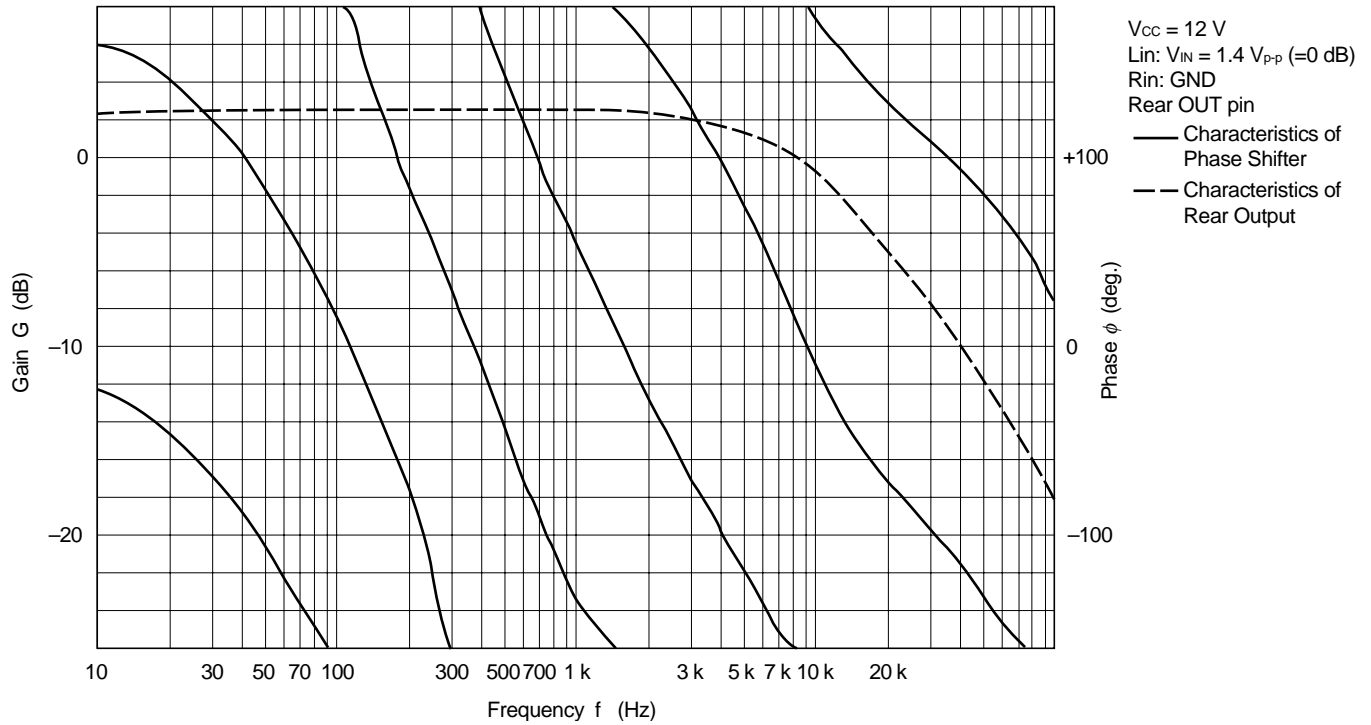


(4) Simulated Mode

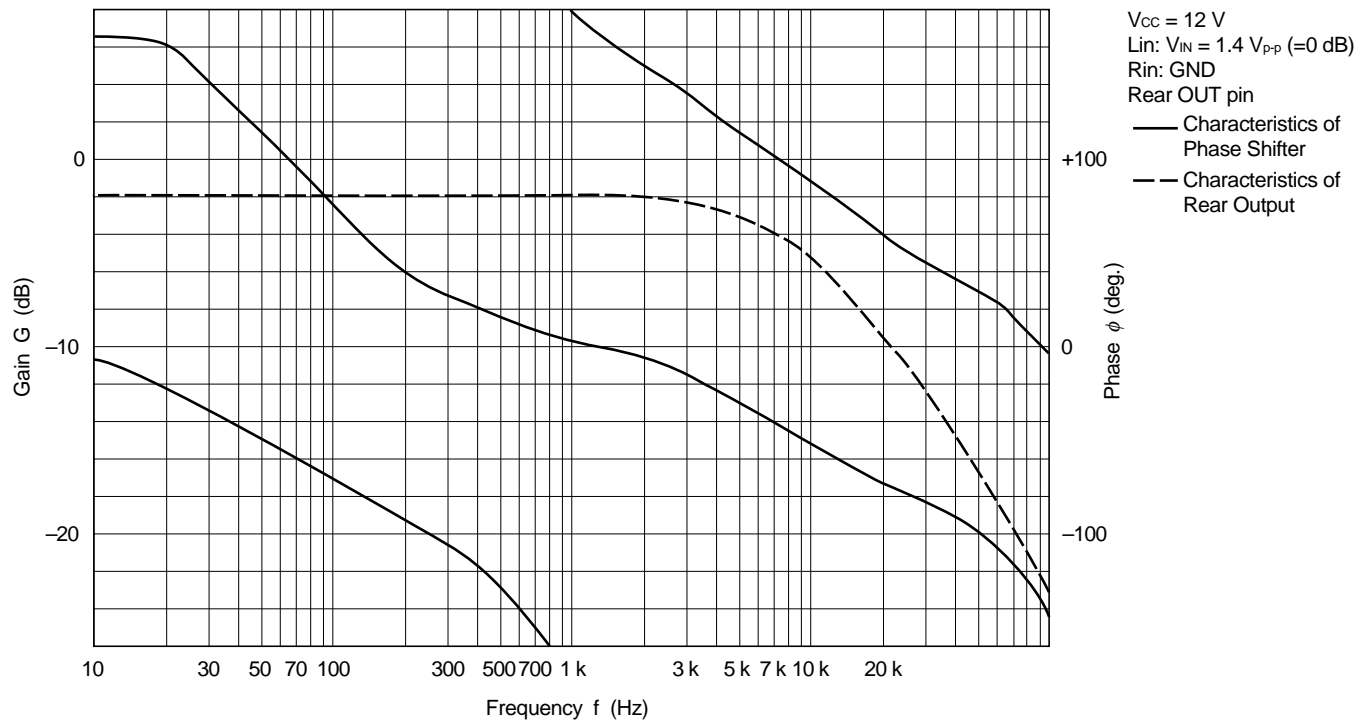


6.2 Characteristics of Phase Shifter and Rear Output

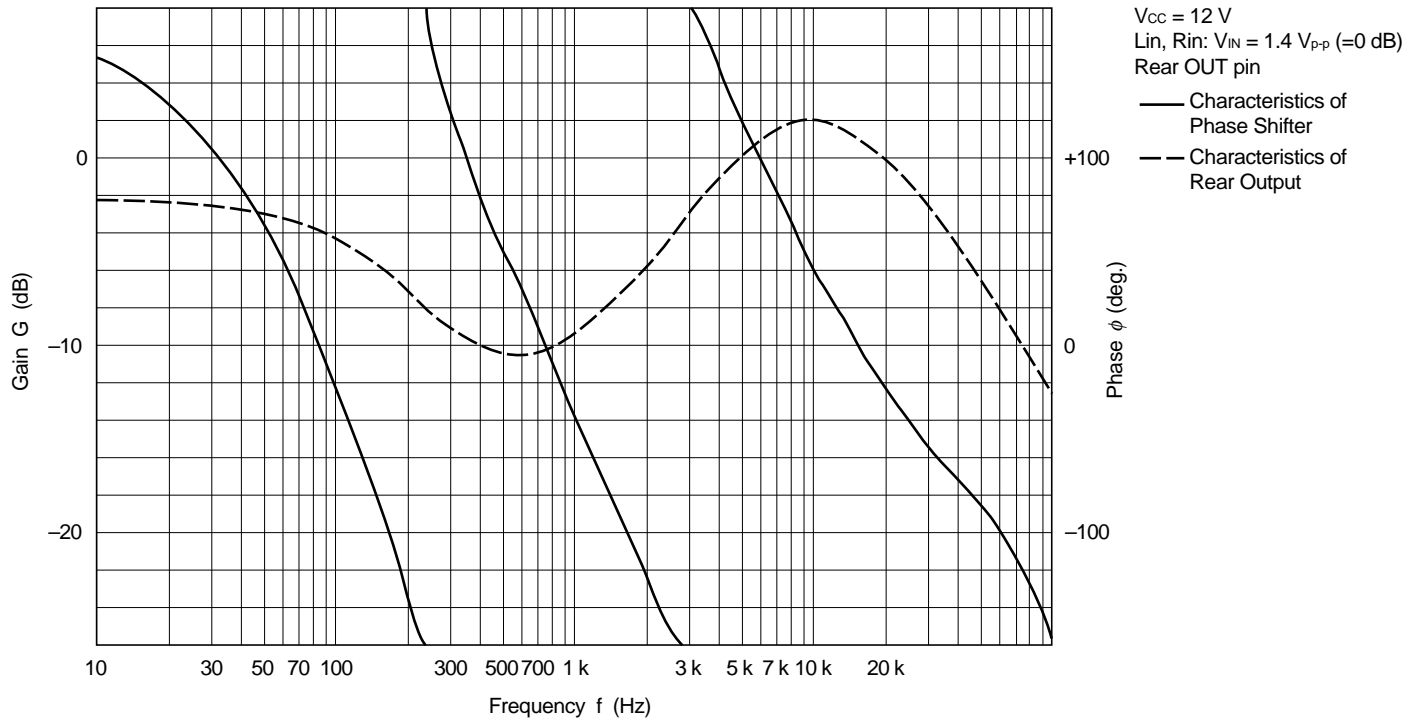
(1) Movie Mode



(2) Music Mode

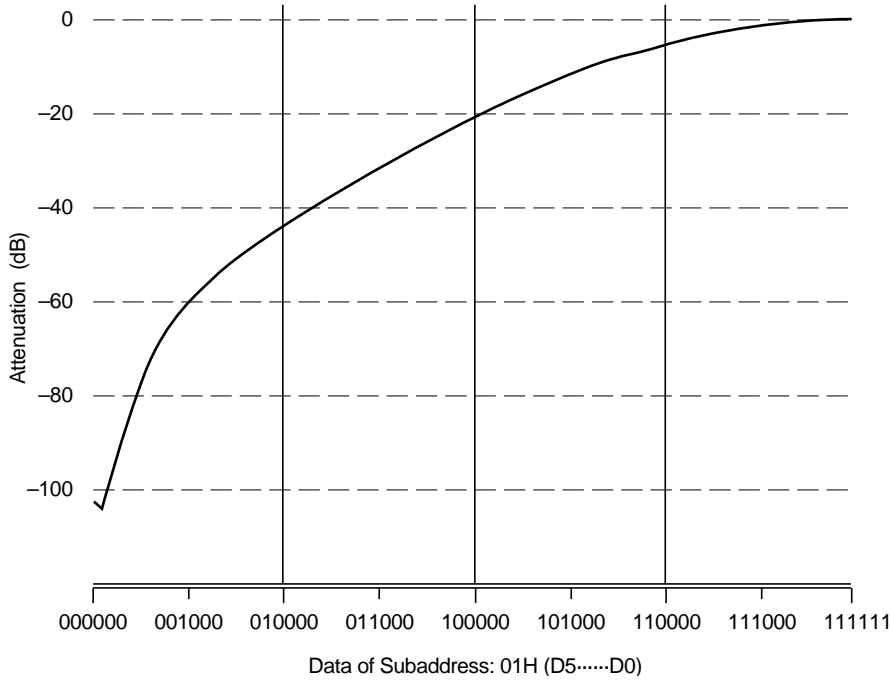


(3) Simulated Mode



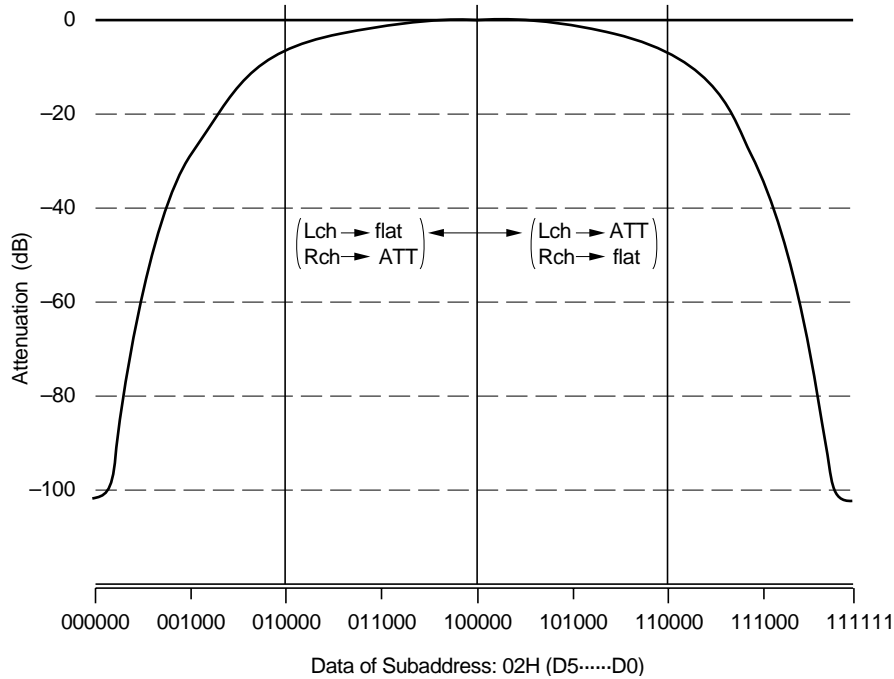
6.3 Control Characteristics

(1) Volume Control Characteristics



OFF mode
 f = 1 kHz
 Lin or Rin: $V_{IN} = 1.4 V_{p-p}$ (=0 dB)
 Lin or Rin: GND

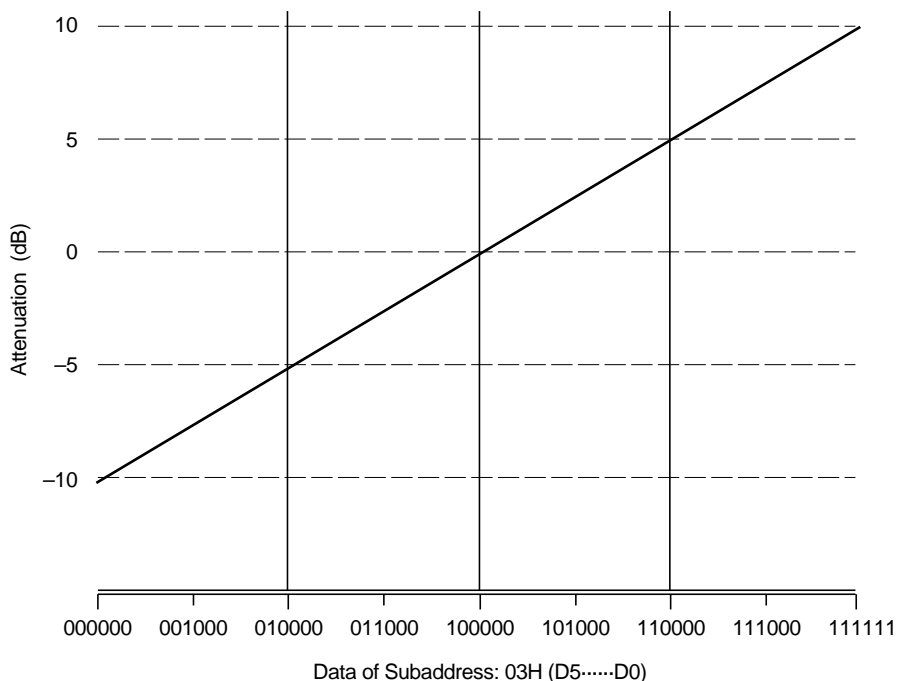
(2) Balance Control Characteristics



OFF mode
 f = 1 kHz
 L1 OUT
 Lin: $V_{IN} = 1.4 V_{p-p}$ (=0 dB)
 Rin: GND
 R1 OUT
 Lin: GND
 Rin: $V_{IN} = 1.4 V_{p-p}$ (=0 dB)

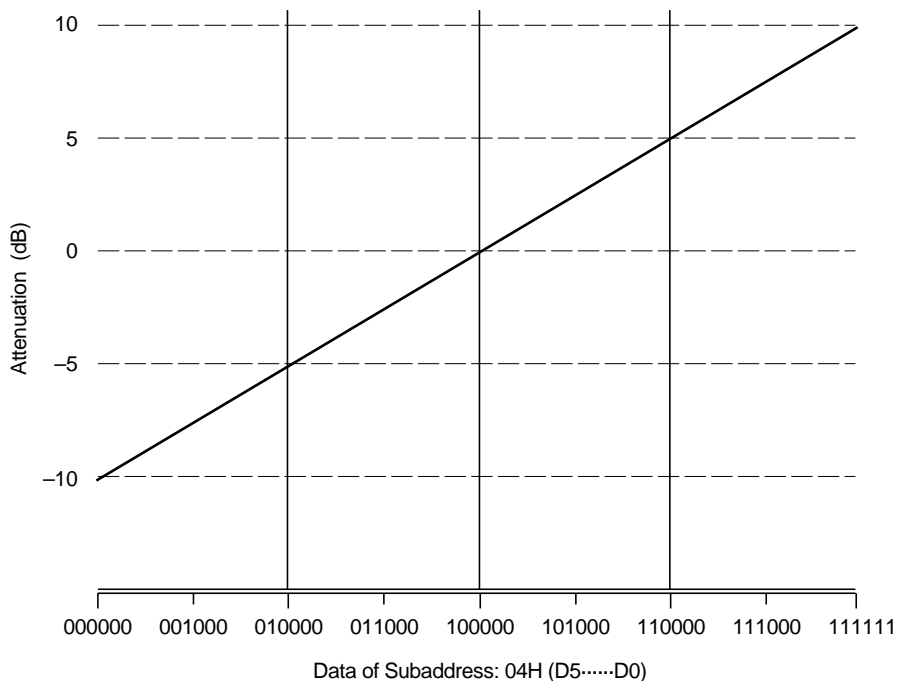
(Lch → flat, Rch → ATT) ← (Lch → ATT, Rch → flat)

(3) Tone Control Characteristics (Bass)



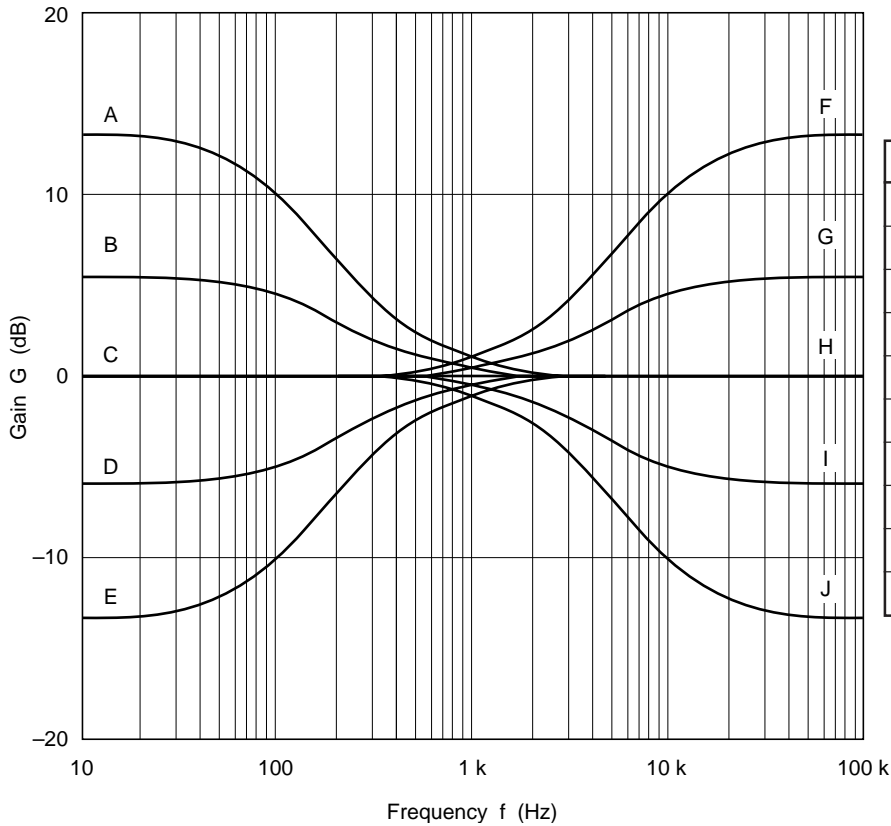
OFF mode
 Bass: f = 100 Hz
 Lin: $V_{IN} = 1.4 V_{p-p}$ (=0 dB)
 Rin: GND
 L1 OUT

(4) Tone Control Characteristics (Treble)



OFF mode
 Treble: f = 10 kHz
 Lin: $V_{IN} = 1.4 V_{p-p}$ (=0 dB)
 Rin: GND
 L1 OUT

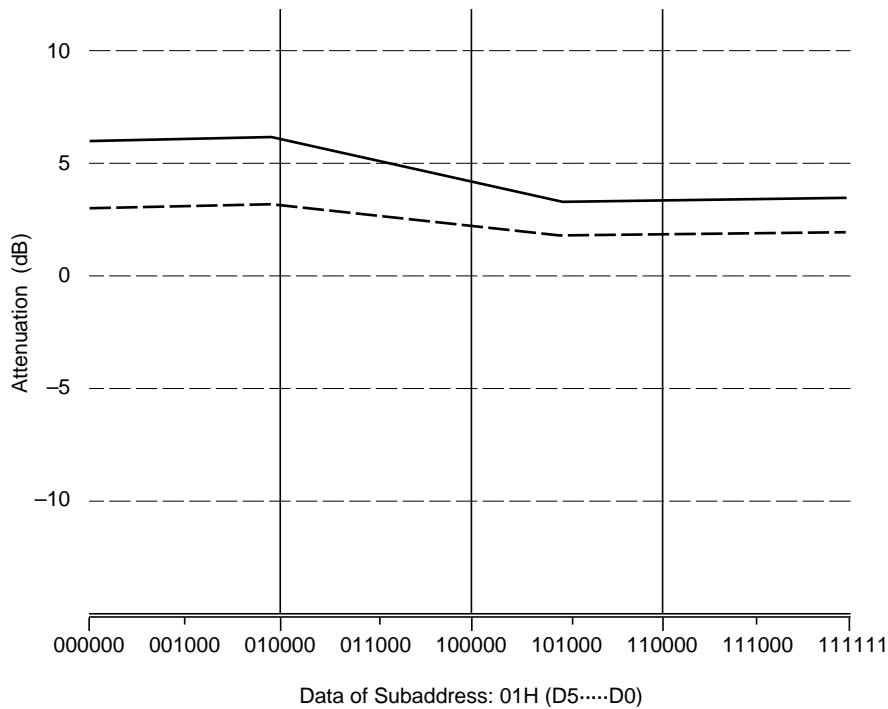
(5) Tone Frequency Characteristics



OFF mode
 Lin: $V_{IN} = 1.4 V_{p-p}$ (=0 dB)
 Rin: GND
 L1 OUT

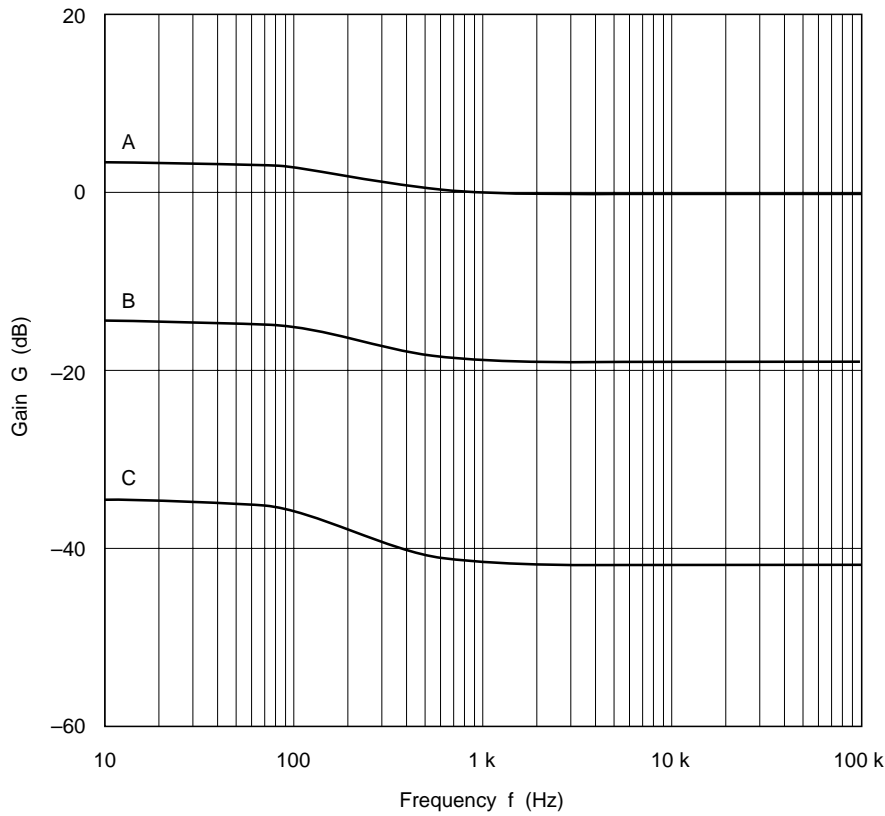
Curve	Subaddress	Data (D5D0)
A	03H	111111
B		110000
C		100000
D		010000
E		000001
F	04H	111111
G		110000
H		100000
I		010000
J		000001

(6) Low Boost Control Characteristics



OFF mode
 f = 100 Hz
 Lin: $V_{IN} = 1.4 V_{p-p}$ (= 0 dB)
 Rin : GND
 L1 OUT
 — Low Boost 1 (6 dB)
 - - Low Boost 2 (3 dB)

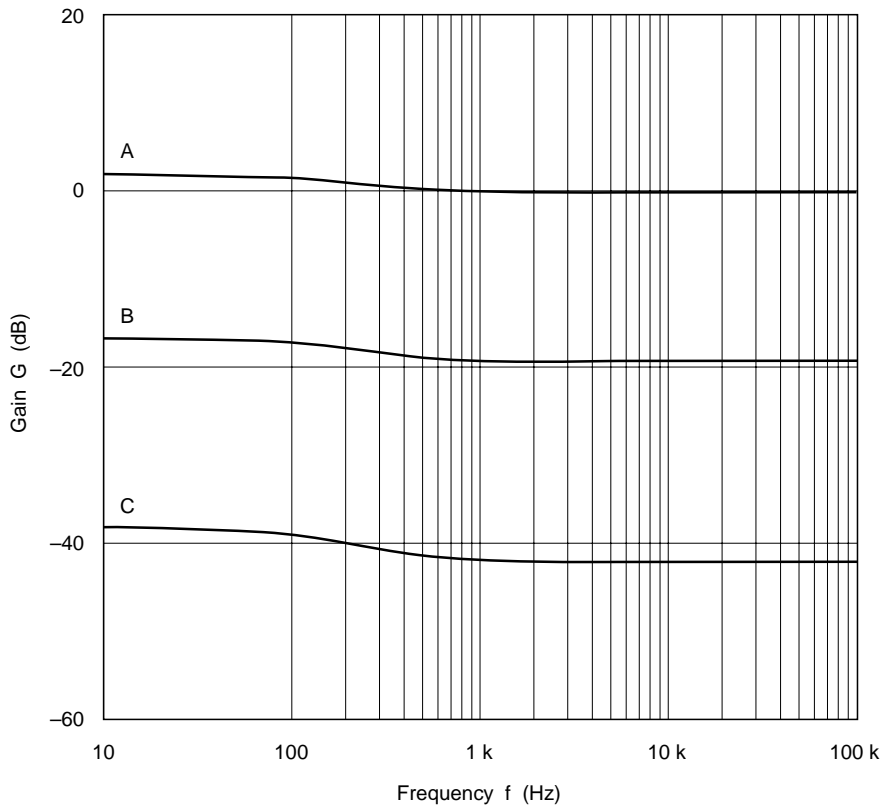
(7) Low Boost 1 (6 dB)



V_{CC} = 12 V
 Lin: V_{IN} = 1.4 V_{p-p} (= 0 dB)
 Rin: GND
 L1 OUT

Curve	Subaddress	Data (D5D0)
A	01H	111111
B		100000
C		010000

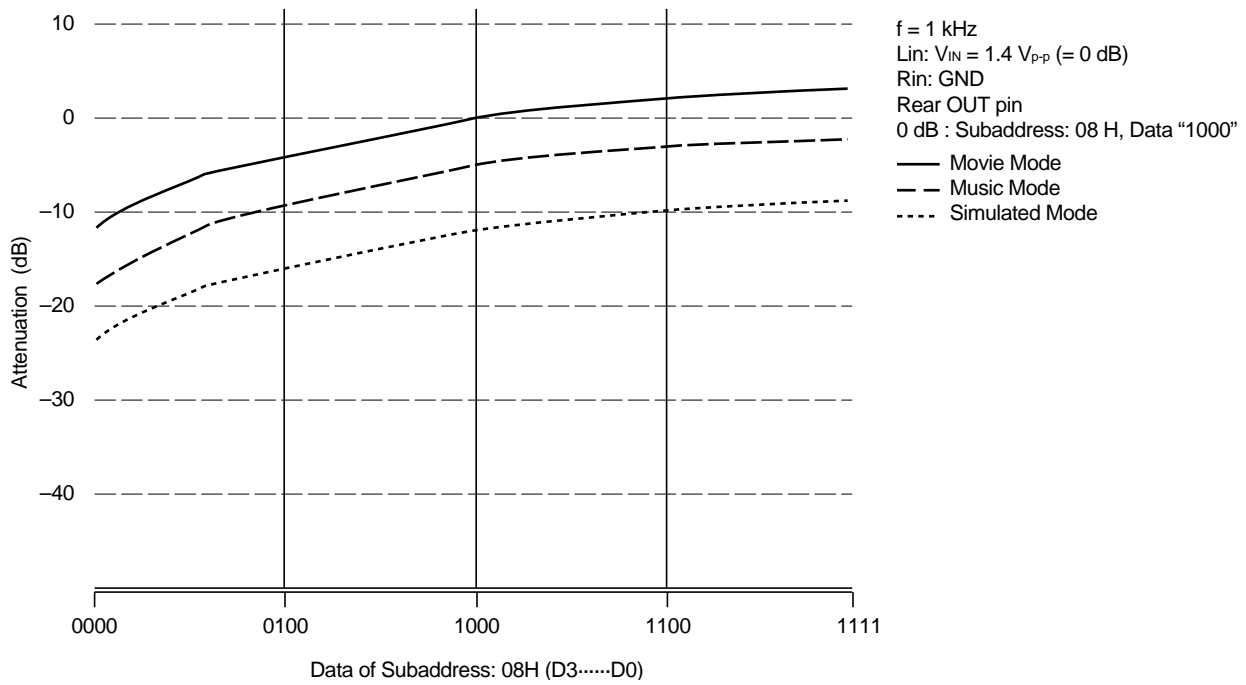
(8) Low Boost 2 (3 dB)



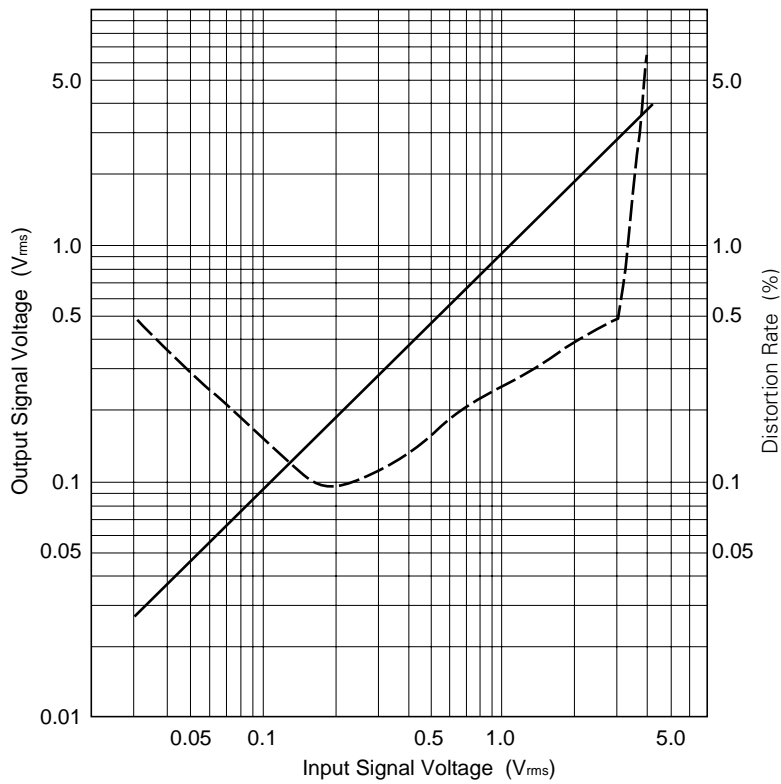
V_{CC} = 12 V
 Lin: V_{IN} = 1.4 V_{p-p} (= 0 dB)
 Rin: GND
 L1 OUT

Curve	Subaddress	Data (D5D0)
A	01H	111111
B		100000
C		010000

(9) Effect Control Characteristics

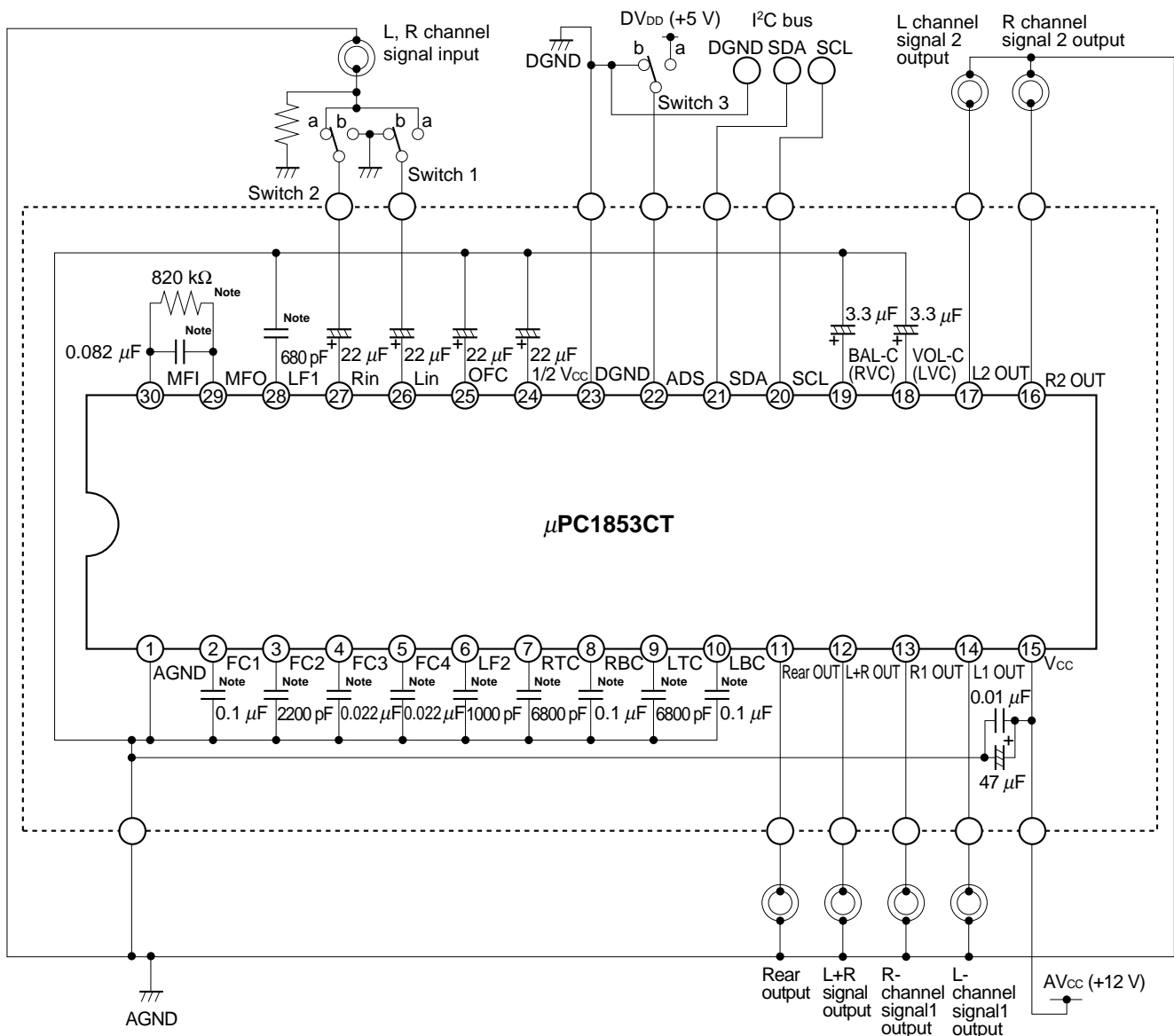


6.4 Input/Output Characteristics, Distortion Rate



f = 1 kHz
 Lin or Rin: $V_{IN} = 1.4 V_{p-p}$ (= 0 dB)
 Lin or Rin: GND
 μPC1853-01
 Subaddress: 01H, Data "111111"
 Subaddress: 02H, Data "100000"
 μPC1853-02
 Subaddress: 01H, 02H,
 Data "111111"
 — Output Signal Voltage
 - - Distortion Rate

7. MEASURING CIRCUIT



Note Recommended external parts.

- Carbon-film resistor : ±1 %
- Film capacitor : ±1 %
- Ceramic capacitor : ±1 %

Use external parts as follows unless otherwise specified.

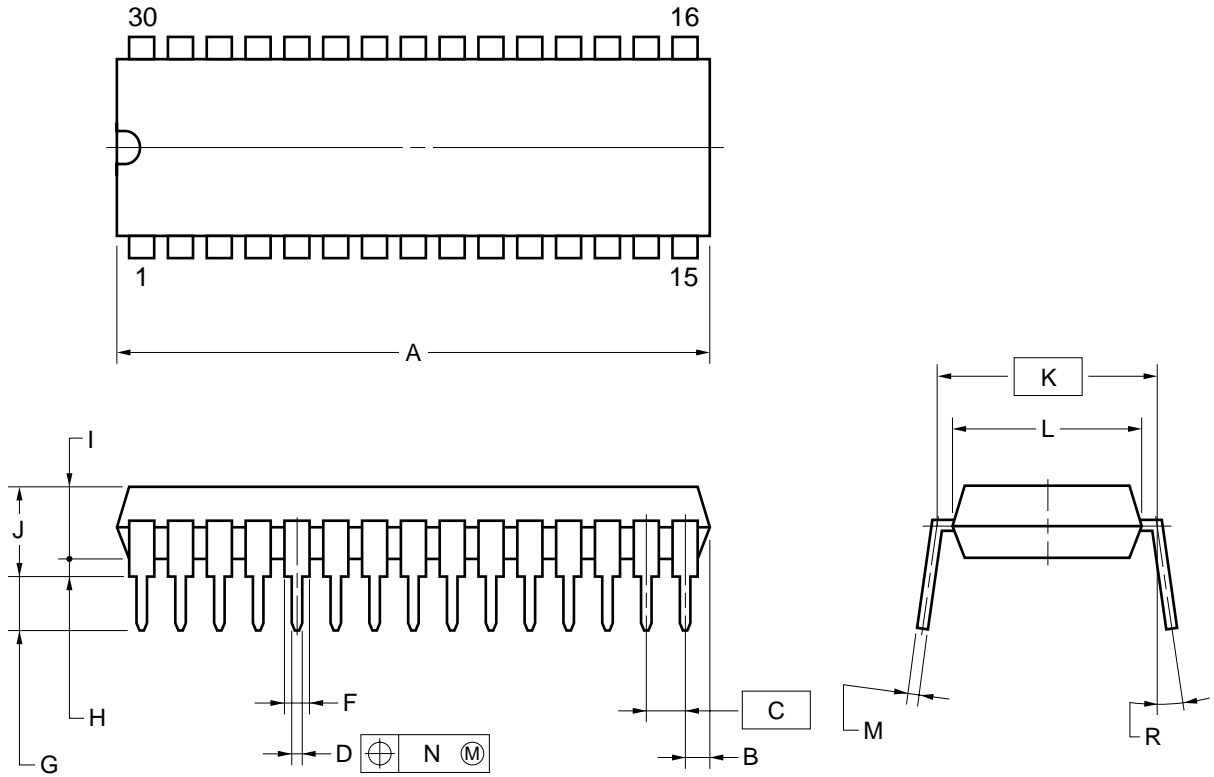
- Carbon-film resistor : ±5 %
- Film capacitor : ±20 %
- Electrolytic capacitor : ±20 %

Attention on Printed Wiring

1. AGND: Wide area grounding.
2. Connect terminating resistors as near pins 26 and 27 as possible.
3. Make the wiring of I²C bus block distant from the wiring of analog block.
4. Connect by-pass capacitor near pin 15 (V_{cc} pin).

8. PACKAGE DIMENSIONS

30PIN PLASTIC SHRINK DIP (400 mil)



NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

S30C-70-400B-1

[MEMO]

Caution: Purchase of NEC I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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Anti-radioactive design is not implemented in this product.

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