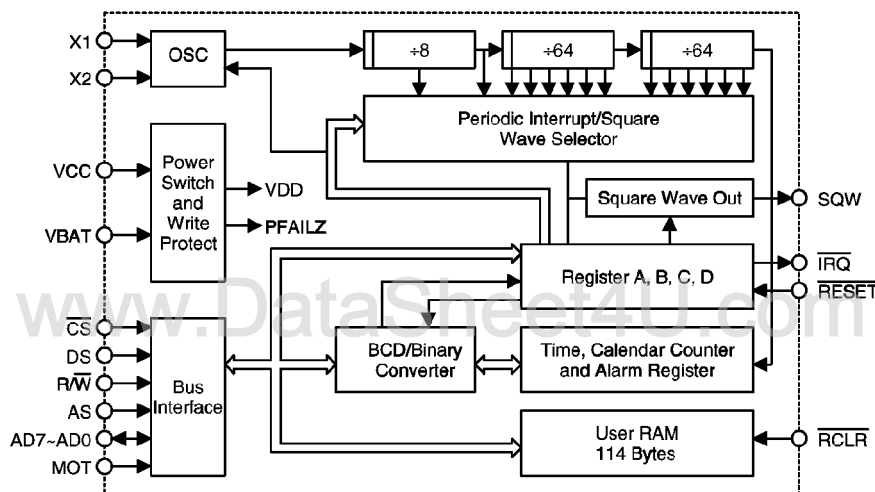# HOLTEK

HT12885
Real Time Clock

Features

- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Supports Motorola and Intel bus timing
- Time, calendar and alarm data in binary or BCD format
- Selectable 12-hour or 24-hour mode with AM and PM in 12-hour mode
- Supports daylight saving function

- 128 bytes RAM includes 14 bytes for clock and control and 114 bytes for general purpose
- Programmable square wave output signal
- Three independent software-maskable interrupts:
  - Time-of-day alarm: once/second to once/day
  - Periodic rates from 122μs to 500ms
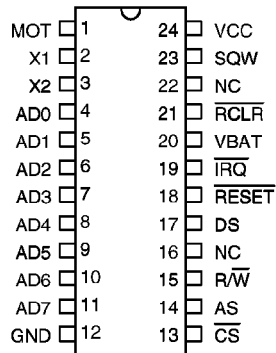 - End of clock update cycle

General Description

The HT12885 is a Real Time Clock with Builtin 128 Bytes RAM. To ensure that the clock keeps operating normally and the RAM data is not lost during power down; an external crystal and battery is required.

Block Diagram

Pin Assignment

```
         ┌──┬─┐
MOT   □ 1│  U│24 □ VCC
X1    □ 2│   │23 □ SQW
X2    □ 3│   │22 □ NC
AD0   □ 4│   │21 □ RCLR
AD1   □ 5│   │20 □ VBAT
AD2   □ 6│   │19 □ IRQ
AD3   □ 7│   │18 □ RESET
AD4   □ 8│   │17 □ DS
AD5   □ 9│   │16 □ NC
AD6   □ 10│  │15 □ R/W
AD7   □ 11│  │14 □ AS
GND   □ 12│  │13 □ CS
         └────┘
```

HT12885
– 24 DIP/SOP

Pin Description

Pin Name	I/O	Description
MOT	I	Bus type selection
X1, X2	—	32.768kHz crystal connection
AD0~AD7	I/O	Multiplexed address/data bus
GND	—	Ground
$\overline{CS}$	I	Chip select
AS	I	Address strobe
R/$\overline{W}$	I	Write strobe
NC	—	No connection
DS	I	Data strobe
$\overline{RESET}$	I	Reset input
$\overline{IRQ}$	O	Interrupt request output
VBAT	—	+3V battery input
$\overline{RCLR}$	I	RAM clear
SQW	O	Square wave output
VCC	—	+5V supply

Absolute Maximum Ratings*

Supply Voltage ....–0.5V to +6V   Storage Temperature.................–40°C to +70°C

Input Voltage................. V_{SS}–0.5V to V_{DD}+0.5V   Operating Temperature...................0°C to 70°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
I_{CC1}	Power Supply Current[1]	4.5~5.5V			7	15	mA
I_{IL}	Input Leakage[2]	4.5~5.5V		–1		1	µA
I_{LO}	I/O Leakage[3]	4.5~5.5V		–1		1	µA
R_{PL}	Pin MOT Pull-low Resistance	4.5~5.5V		5	11	2	kΩ
I_{OH}	Output @ 2.4V[4]	4.5~5.5V		2			mA
I_{OL}	Output @ 0.4V	4.5~5.5V		6			mA
V_{pf}	Write Protect Voltage (i.e. VCC Power Fail)	4.5~5.5V		3.8	4.25	4.5	V
I_{BAT}	Battery Supply Current[5]				0.7	1	µA

Notes: 1. All outputs are unload.

2. The MOT pin has an internal Pull-down of 10kΩ.

3. Applies to the AD0~AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in the high impedance state.

4. The $\overline{IRQ}$ pin is open drain.

5. The external Battery supplies power for the Real Time Clock keep working and RAM data retention in the absence of V_{CC} power.

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
t_{CYC}	Cycle Time	4.5~5.5V		385			ns
PW_{EL}	Pulse Width, DS/E Low or RD/$\overline{WR}$ High	4.5~5.5V		150			ns
PW_{EH}	Pulse Width, DS/E High or RD/$\overline{WR}$ Low	4.5~5.5V		125			ns
t_R, t_F	Input Rise and Fall Time	4.5~5.5V				30	ns
t_{RWH}	R/$\overline{W}$ Hold Time	4.5~5.5V		10			ns
t_{RWS}	R/$\overline{W}$ Setup Time Before DS/E	4.5~5.5V		50			ns
t_{CS}	Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	4.5~5.5V		20			ns
t_{CH}	Chip Select Hold Time	4.5~5.5V		0			ns
t_{DHR}	Read Data Hold Time	4.5~5.5V		10			ns
t_{DHW}	Write Data Hold Time	4.5~5.5V		0			ns
t_{ASL}	Muxed Address Vaild Time to AS/ALE Fall	4.5~5.5V		30			ns
t_{AHL}	Muxed Address Hold Time	4.5~5.5V		10			ns
t_{ASD}	Delay Time DS/E to AS/ALE Rise	4.5~5.5V		20			ns
PW_{ASH}	Pulse Width AS/ALE High	4.5~5.5V		60			ns
t_{ASED}	Delay Time, AS/ALE to DS/E Rise	4.5~5.5V		40			ns
t_{DDR}	Output Data Delay Time From DS/E or $\overline{RD}$	4.5~5.5V				70	ns
t_{DSW}	Data Setup Time	4.5~5.5V		100			ns
t_{RWL}	Reset Pulse Width	4.5~5.5V		5			μs
t_{IRDS}	$\overline{IRQ}$ Release From DS	4.5~5.5V				2	μs
t_{IRR}	$\overline{IRQ}$ Release From RESET	4.5~5.5V				2	μs

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Functional Description

Power-down/Power-up functions

If V_{CC} falls below V_{pf} (4.25), the interface will be turned off, i.e., it is not accessible. When VCC falls below the level VBAT, the internal power switch will select VBAT as the power source for the internal circuit (including the clock circuit and RAM). During power on, when VCC is greater than VBAT, the power switch will select VCC as the power source for the internal circuit and RAM. If VCC reaches Vpf then this Real Time Clock will be accessible after 200ms, as long as the oscillator is running and the divider chain is not in reset (see Register A).

Signal descriptions

• MOT (Mode Select)

This pin defines the bus timing mode. When it is connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left floating, Intel bus timing is selected. This pin has an internal pull-down resistor of approximately 10kΩ.

• SQW (Square Wave Output)

The SQW pin can drive a square wave signal which can be selected from the 13 taps of the internal divider chain of the Real Time Clock. By programming Register A as shown in Table 1, the output signal frequency of the SQW pin can be changed, or turned on or off by changing the Register B SQWE bit. The SQW signal will be turned off (floating) when V_{CC} falls bellow V_{pf}.

• X1, X2

These pins connect to a standard 32.768kHz quartz crystal. X1 should be connected to ground a 10MΩ resistor.

• $\overline{RCLR}$

This $\overline{RCLR}$ pin will clear all 114 bytes of the general purpose RAM with the exception of the clock and control RAM, by forcing it to logic 0 in back-up mode (when V_{CC} is not applied). This pin is pulled up internally.

• AD0~AD7 (Multiplexed bidirectional address/data bus)

AD6 to AD0 will be latched on the falling edge of the AS signal when accessing the address of the Real Time Clock. After this, AD7 to AD0 will be considered as write data to the Real Time Clock if they are stable while DS is a logic high and the R/$\overline{W}$ pulse is active low (Intel) or R/$\overline{W}$ is low and the DS pulse is active high (Motorola). In the read cycle, the accessed data will be present on AD7 to AD0 after the falling edge of the DS signal (Intel) or the rising edge of the DS signal (Motorola) if R/$\overline{W}$ is high.

• AS (Address Strobe Input)

AD6 to AD0 will be latched into the Real Time Clock at the falling edge of the AS signal when accessing the address.

Register a Select bits				tₚₗ Periodic Interrupt Rate	SQW Output Frequency
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625ms	256Hz
0	0	1	0	7.8125ms	128Hz
0	0	1	1	122.070μs	8.192kHz
0	1	0	0	244.141μs	4.096kHz
0	1	0	1	488.281μs	2.048kHz
0	1	1	0	976.5625μs	1.024kHz
0	1	1	1	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz
1	1	0	1	125ms	8Hz
1	1	1	0	250ms	4Hz
1	1	1	1	500ms	2Hz

Table 1. Periodic interrupt rate and square wave output frequency

• DS/$\overline{\text{RD}}$ (Data Strobe or Read Input)

The DS/$\overline{\text{RD}}$ pin has two modes of operation dependent upon on the MOT pin level. When connected to V$_{CC}$, Motorola bus timing is selected. In this mode DS or Data Strobe generates a positive pulse during the later portion of the bus cycle. During read cycles, DS identifies drives the time when the HT12885 to drives the bidirectional bus. In write cycles the trailing edge of DS causes the HT12885 to latch the written data. Intel bus timing is selected when the MOT pin is connected to GND. In this mode the DS pin is called Read ($\overline{\text{RD}}$), and it identifies the time period when the HT12885 drives the bus with read data. The $\overline{\text{RD}}$ signals have the same definition as the Output Enable ($\overline{\text{OE}}$) signal on typical memory devices.

• R/$\overline{\text{W}}$ (Read/Write Input)

The R/$\overline{\text{W}}$ pin also has two modes of operation. When the MOT pin is connected to V$_{CC}$ for Motorola timing, R/$\overline{\text{W}}$ is at a level which indicates whether the current cycle is read or write. A read cycle is indicated by a high level on R/$\overline{\text{W}}$ while DS is high. A write cycle is indicated when R/$\overline{\text{W}}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{\text{W}}$ is an active low signal called $\overline{\text{WR}}$. In this mode the R/$\overline{\text{W}}$ pin has the same meaning as the Write Enable signal ($\overline{\text{WE}}$) on generic RAMs.

• $\overline{\text{CS}}$ (Chip Select input)

The chip select signal must be kept low during the entire accessing cycle.

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- **IRQ** (Interrupt Request output)

  The IRQ pin is an active low output. The IRQ output is low if the status bit causing the interrupt is set and the corresponding interrupt-enable bit is set. Reading the C register will clear the IRQ pin. The RESET pin also clears the interrupts. The IRQ pin is an open drain output and needs an external pull-up resistor.

- **RESET** (Reset input)

  The RESET pin does not change the contents of the clock, calendar, or RAM. During power up, the RESET pin should be kept low, for a time exceeding 200ms before accessing the data, otherwise, accessing will fail (interface is turned off).When RESET is low and V_{CC} is above Vpf, the following occurs.

  - Periodic Interrupt Enable (PIE) bit is cleared to zero.
  - Alarm Interrupt Enable (AIE) bit is cleared to zero.
  - Update Ended Interrupt Enable (UIE) is cleared to zero.
  - Square Wave Output Enable (SQWE) bit is cleared to zero.
  - Interrupt Request status Flag (IRQF) bit is cleared to zero.
  - Periodic Interrupt Flag (PF) bit is cleared to zero.
  - Alarm Interrupt Flag (AF) bit is cleared to zero.
  - Update Ended Interrupt Flag (UF) bit is cleared to zero.
  - The device is not accessible until RESET is returned high.

Address map

Figure 2 on the next page illustrates the address map of the HT12885. It consists of 10 bytes for RTC time, calendar and alarm data, and 4 bytes for control and status, and 114 bytes for general purpose. All of these can be written to or read except for the following conditions:

- Registers C and D are read-only
- Bit 7 of Register A is read-only

The detailed definitions of the four registers (A, B, C and D) are described in the "Register" section.

Time, calendar and alarm

The data of the ten time, calendar and alarm bytes can be in Binary or Binary-Coded Decimal (BCD) format. The data mode bit (DM) of Register B must be set to the appropriate logic level before setting the contents of time, calendar and alarm. All ten time, calendar and alarm bytes must use the same data mode. To enable the Real Time Clock to update the time and calendar bytes, the SET bit in Register B must be cleared. After proper setting, the Real Time Clock will be updated in the selected mode. If the data mode is changed, all the ten time, calendar and alarm data bytes should be re-initialized. The binary and BCD formats of the ten time, calendar and alarm bytes are illustrated in Table 2. If the 24hr/12hr bit in Register B is changed, the hour byte should be re-initialized.

When the 12-hour format is selected, the high order bit of the hour byte represents A.M. when it is a logic 0, or P.M. when it is a logic 1. When the ten bytes advance by one second the Real Time Clock will check for an alarm condition (once per second). If a read of the ten bytes occurs during an update cycle, the seconds, minutes, hours, etc. possibly may not be correct.

The Real Time Clock alarm can operate in two ways. First, set the alarm time (second alarm, minute alarm and hour alarm) properly and set the alarm interrupt enable bit in register B. The alarm interrupt will then be generated at the specified time each day. The second method is to fill a "don't care" code in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF, i.e., the two most significant bits of the alarm byte are at logic 1. If the "don't care" code is set in the hour byte, an alarm interrupt will be generated each hour. Similarly, when the "don't care" code is set in the hour and minute bytes, an alarm interrupt will be generated every minute. If "don't care" codes fill all three alarm bytes an interrupt will be generates every second.
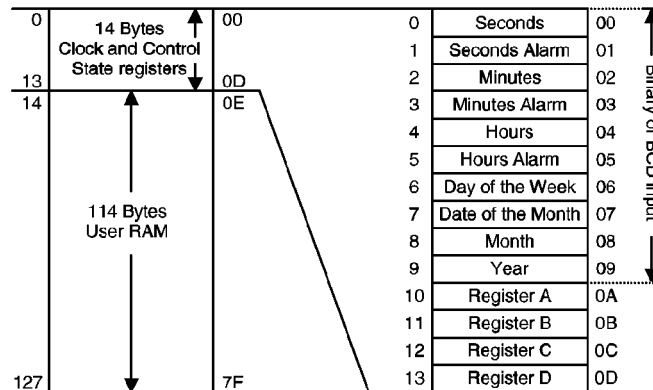
Figure 2: Address map

Address Location	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
0	Seconds	0~59	00~3B	00~59
1	Seconds Alarm	0~59	00~3B	00~59
2	Minutes	0~59	00~3B	00~59
3	Minutes Alarm	0~59	00~3B	00~59
4	Hours-12-hr Mode	1~12	01~0C AM, 81~8C PM	01~12 AM, 81-92 PM
	Hours-24-hr Mode	0~23	00~17	00~23
5	Hours Alarm-12-hr	1~12	01~0C AM, 81~8C PM	01~12 AM, 81-92 PM
	Hours Alarm-24-hr	0~23	00~17	00~23
6	Day of the week, Sunday=1	1~7	01~07	01~07
7	Date of the month	1~31	01~1F	01~31
8	Month	1~12	01~0C	01~12
9	Year	0~99	00~63	00~99

Table 2: Time, calendar and alarm data modes

General purpose RAM

The 114 general purpose RAM bytes are re-served for the user and are available any time even during the update cycle.

Interrupts

By programming, the alarm interrupt can be gen-erated at rates from once per second to once per day. The periodic interrupt can be generated at rates from 500ms to 122μs. The update-ended interrupt can be used to inform the system that an update cycle is complete.

The user can select which interrupt will be used by setting the corresponding enable bit in Regis-ter B to a logic 1. When an interrupt condition occurs (one or more flag bits are set), a zero in an interrupt enable bit will prevent the interrupt from being initiated. If an interrupt flag is already set when the interrupt is enabled, $\overline{IRQ}$ will imme-diately generate an active low level. For this rea-son, the programmer should ensure that all previously enabled interrupts are cleared before new ones are enabled.

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When an interrupt event occurs, the corresponding flag bit is set to logic 1 in Register C, independent of the level of the corresponding enable bit in Register B. A typical application is to check the flag bits to see if the corresponding enable bits are enabled or not. When the flag is set, it means that an interrupt event has occurred since the flag bit was last read. All flag bits that are set (high) are cleared after reading.

When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is active low. $\overline{IRQ}$ will remain active low until all of the flag bits of the interrupt sources with enable bit set are cleared. If the IRQF bit in Register C is a 1, it means that at least one interrupt has occurred. Reading Register C will clear all active flag bits and the IRQF bit.

Oscillator control bits

The internal oscillator of the Real Time Clock can be turned on or off as needed. A pattern of 010 from bits 6 through 4 of Register A will enable the oscillator and the divider chain. A pattern of 11X will enable the oscillator, but reset the divider chain. All other combinations of bits 6 to 4 disable the oscillator.

Square wave output

The square wave output frequency can be changed by programming the RS3~RS0 bits in Register A. One of the 13 frequencies as shown in Table 1 can be selected. The selected SQW frequency is the same as the frequency of the periodic interrupt, and the SQW pin can be turned off if the square wave enable bit (SQWE) is 0.

Periodic interrupt

The periodic interrupt will drive the $\overline{IRQ}$ pin to an active low state from once every 500ms to once every 122μs. The periodic interrupt rate is the same as the square wave frequency programmed by the RS3 to RS0 bits in Register A (as shown in Table 1). These two functions have different enable bits in Register B (PIE and SQWE).

Update cycle

The HT12885 performs an update cycle once per second no matter what the value of the SET bit in Register B. If the SET bit is set to 1, the user copy of the double buffered time, calendar and alarm bytes is stopped and will not be updated while the time advances. However, the Real Time Clock keeps on updating the internal copy of the buffer. As a result, the Real Time Clock is time independent of reading or writing to the time, calendar and alarm buffers. During the update cycle the Real Time Clock will compare each alarm byte with the corresponding time byte and generate an alarm if the condition occurs as described in the Time, Calendar and Alarm section.

Registers

The four Real Time Clock registers are always accessible, even during on update cycle.

- Register A

MSB   LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

⬧ UIP

The Update In Progress (UIP) bit is a status flag which indicates whether an update cycle is in progress or not. When the bit is 1, this indicates that a update cycle is in progress. When it is 0, the update transfer will not occur for at least 244μs. The UIP is a read only bit and is not affected by RESET. Writing a 1 to the SET bit in Register B inhibits any update operation and clears the UIP status bit.

⬧ DV2, DV1, DV0

These three bits are used to turn the oscillator on or off and to reset the divider chain. The pattern of 010 is the only combination that can turn the oscillator on and allow the Real Time Clock to keep time. A pattern of 11X will enable the oscillator but keep the divider chain in a reset condition. After a pattern of 010 is written to these bits an update will occur after 500ms.

♦ RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the internal divider chain. The selected rate can be used as the square wave (SQW pin) output frequency and/or a periodic interrupt rate. The different combination of RS3~RS0 maps to the corresponding frequency as shown in Table 1.

• Register B

MSB   LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

♦ SET

If the SET bit is high then the update transfer is inhibited, otherwise the update transfer operates normally. SET is a read/write bit and is not modified by RESET.

♦ PIE

If the PIE bit is high then a periodic interrupt will be generated via the IRQ pin at a frequency defined by the RS3~RS0 bits of Register A. A zero in the PIE bit disables the IRQ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at a periodic rate. PIE is a read/write bit and is not modified by any internal functions, but is cleared to 0 during a RESET.

♦ AIE

The read/write Alarm Interrupt Enable (AIE) bit enables the Alarm Flag (AF) bit in Register C to assert IRQ when it is high. The active low RESET pin clears the AIE bit.

♦ UIE

The read/write Update Ended Interrupt Enable (UIE) bit enables the Update End Flag (UF) bit in Register C to assert IRQ when it is high. The active low RESET pin clears the UIE bit.

♦ SQWE

The read/write Square Wave Enable (SQWE) bit enables the SQW pin to drive a square wave out at a frequency specified by RS3~RS0 when it is high. When the SQWE

bit is low, the SQW pin is held low. The active low RESET pin clears the SQWE bit.

♦ DM

The Data Mode (DM) bit defines the format of the time and calendar information. If it is a 1 then it denotes that the data is in binary format, otherwise it is in BCD format. The RESET pin does not change it.

♦ 24/12

The 24/12 control bit specifies the hour byte format. A 24-hour mode is indicated by a 1, and a 12-hour mode by a 0. This bit is read/write and is not changed by internal functions or RESET.

♦ DSE

The read/write Daylight Savings Enable (DSE) bit enables the daylight saving function when it is a 1. The daylight saving function ensures that the time on the first Sunday in April increments from 1:59:59 AM to 3:00:00 AM and on the last Sunday in October from 1:59:59 AM to 1:00:00 AM. If it is a 0 then the daylight saving function is disabled. This bit is not changed by internal functions or RESET.

• Register C

MSB   LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQF	PF	AF	UF	0	0	0	0

♦ IRQF

The interrupt Request Flag (IRQF) bit is set to a 1 when one or more of the following conditions occur:

PF=PIE=1

AF=AIE=1

UF=UIE=1

That is, IRQF=(PF•PIE)+(AF•AIE)+(UF•UIE)

If the IRQF bit is 1 then the IRQ pin will be active low. Reading Register C or when the RESET pin is low will clear all flag bits.

- PF

   The Periodic Interrupt Flag (PF) is a read-only bit, If it is a 1 it means that an edge is detected on the selected tap of the divider chain. When both PF and PIE are set to 1, the IRQ signal is active and will set the IRQF bit. Reading Register C or a RESET will clear the PF bit.

- AF

   A 1 in the Alarm Interrupt Flag (AF) bit means that the current time is equal to the alarm time. If the AIE bit is also a 1 then the IRQ pin will go low and IRQF bit will be set to 1. Reading Register C or a RESET will clear this bit.

- UF

   After each update cycle the Update Ended Interrupt Flag (UF) bit will be set. If the UIE bit is also set to 1 then the IRQ pin will be driven low and the IRQF bit be set to 1. Reading Register C or a RESET will clear this bit.

- Bit 0 through bit 3

   These bits are unused and always read zero and cannot be written to.

- Register D

   MSB   LSB

 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
   |-------|-------|-------|-------|-------|-------|-------|-------|
   | VRT | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- VRT

   This bit is read only. If it is a zero, it means that the external lithium energy source is exhausted and the contents of the RTC data and RAM data maybe incorrect.

- Bit 6 through Bit 0

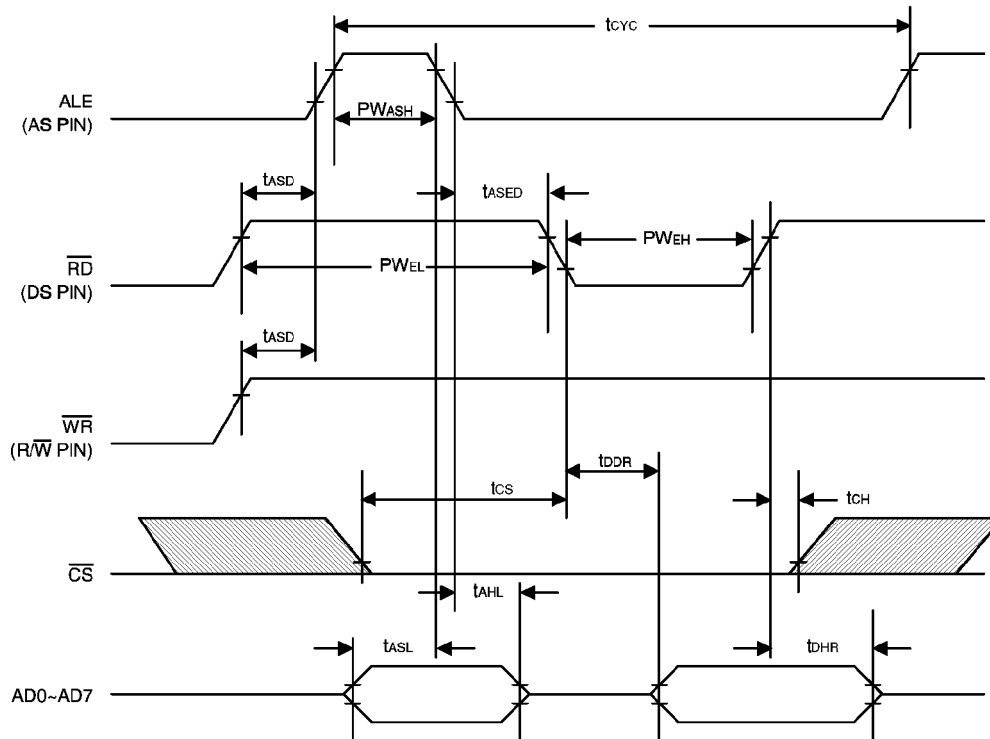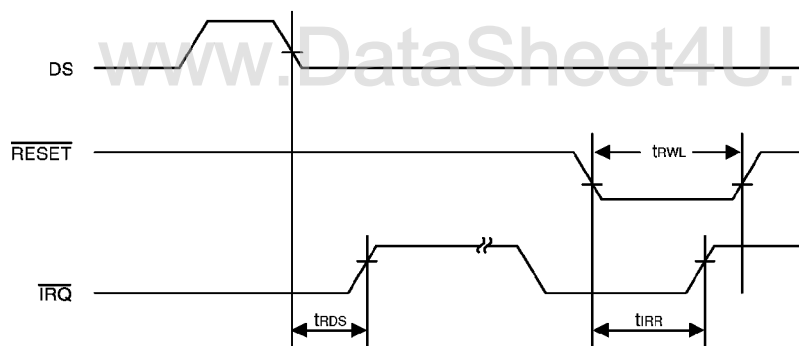   Bit 6 to bit 0 are unused and always read zero and cannot be written to.

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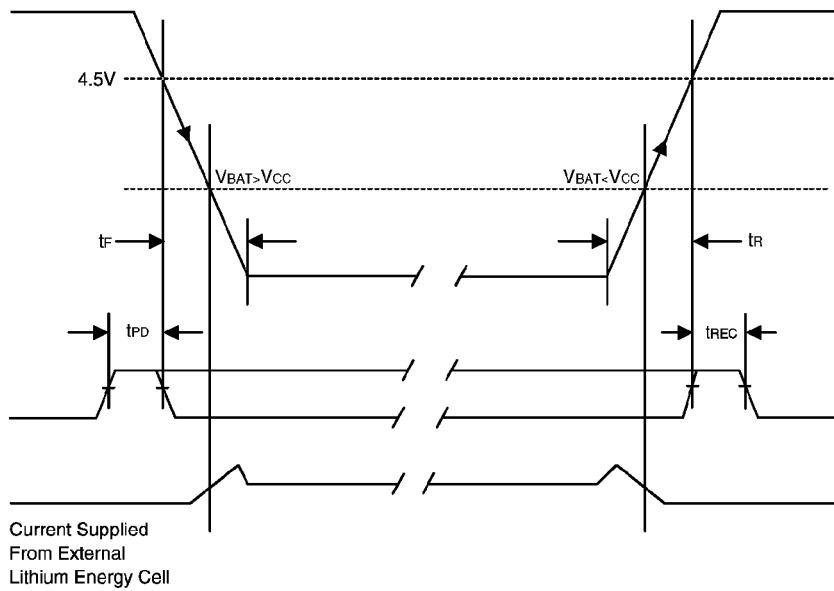
Timing Diagrams

HT12885 bus timing for motorola interface

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HT12885 bus timing for intel interface write cycle

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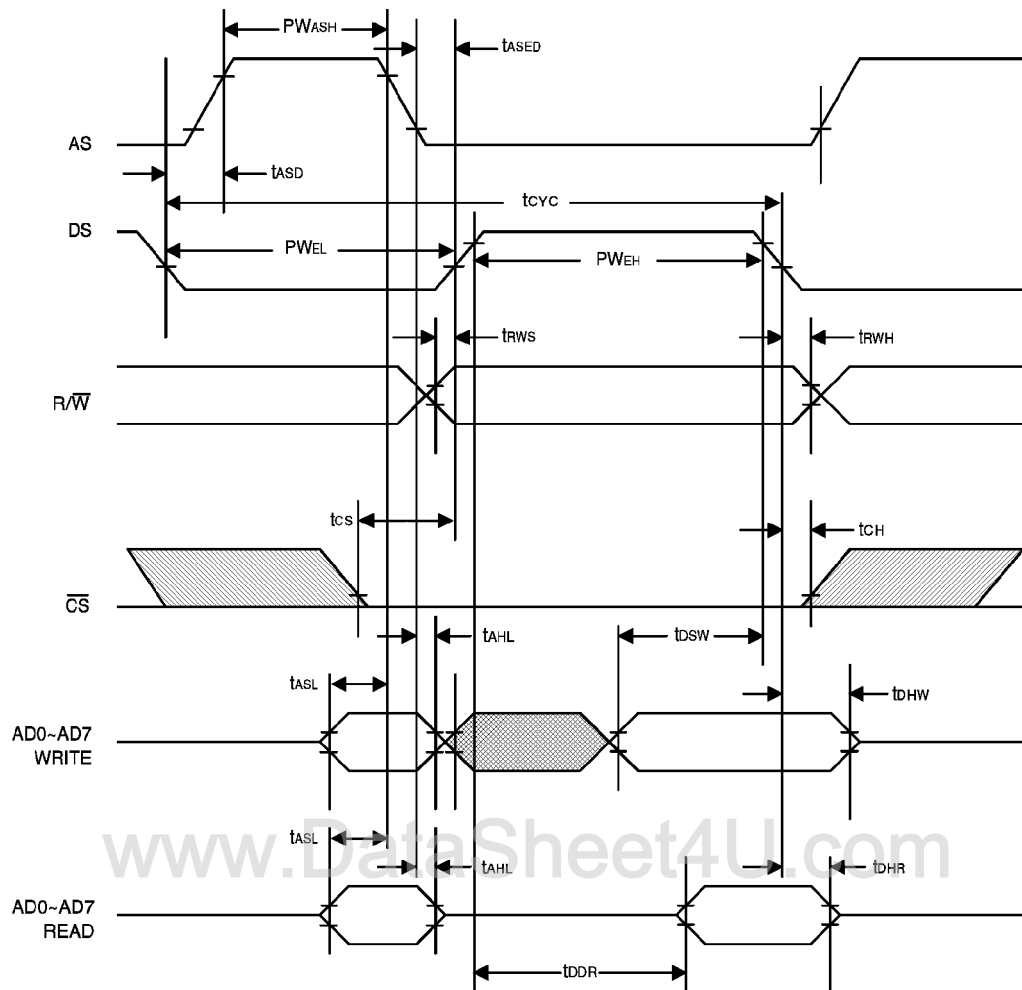
HT12885 bus timing for intel interface read cycle

HT12885 IRQ release delay timing

Power down/power up timing

Current Supplied
From External
Lithium Energy Cell

Power down/power up timing

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
t_{PD}	$\overline{CS}$ at V_{IH} Before Power-down			0			μs
t_F	V_{CC} Slew From 4.5V to 0V ($\overline{CS}$ at V_{IH})			1000			μs
t_R	V_{CC} Slew From 0V to 4.5V ($\overline{CS}$ at V_{IH})			100			μs
t_{REC}	$\overline{CS}$ at V_{IH} After Power-up			20		200	ms

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Application Circuits

```
        ┌─────────────┐                    5V
   MOT ─┤ MOT    VCC  ├──────┬──────┬──────○
        │ X1     SQW  │    104│   +  │10µF
        │ X2     NC   │      ═╧═    ═╧═
   AD0 ─┤ AD0   RCLR  │      ─┬─    ─┬─
   AD1 ─┤ AD1   VBAT  ├───┐   ╧      ╧
 10MΩ   │ AD2    IRQ  │   │
        │ AD3   RESET ├───┤
        │ AD4    DS   │   │  ═╧═ Battery
        │ AD5    NC   │   │   ╧
        │ AD6   R/W   │
        │ AD7    AS   │
   GND ─┤ GND    CS   │
        └─────────────┘
            HT12885
```

X'tal
32768Hz