



HIGH SPEED CMOS SRAM

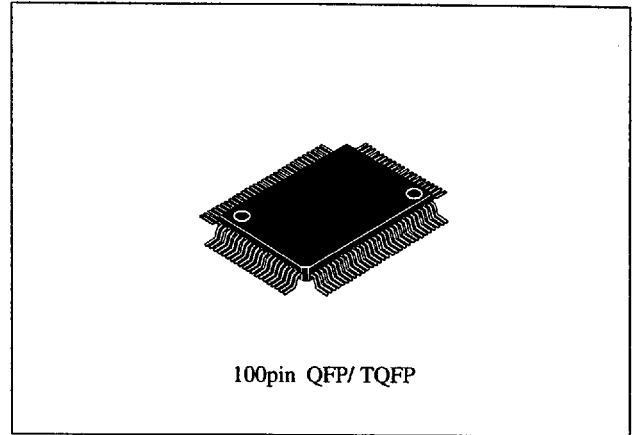
Fast Synchronous with Burst Counter
1M-BIT(32K X 32)

N343532L

-7N

■ Features

- CMOS SRAM organized as 32,768 x 32bits
- +Single+3.3V (+0.3V/-0.2V) Power Supply
- Fast Clock Access time : 7ns/66MHz
- Single Clock, Synchronous operation
- Burst Read/Write :
 - Interleaved Burst and Linear Burst Sequence
- Fully Registered Inputs and Outputs for Pipelined Operation
- All Registers triggered off Positive Clock Edge
- Asynchronous Output Enable : \overline{OE}
- Burst Mode Selectable : MODE
- Separate Byte Write Enable : $\overline{BW1}$ - $\overline{BW4}$, \overline{BWE}
and Global Write Enable : \overline{GW}
- Three Chip Enables for Easy Depth Expansion
- 2 Clock Enable and 1 Clock Disable to eliminate multiple bank bus contention
- Common I/O Using Three State Outputs
- 5V Tolerant Clock Pin
- Flow-Through Mode
- Sleep Mode Pin (ZZ) for Power Down
- Packages : 100 pin QFP, 100 pin TQFP

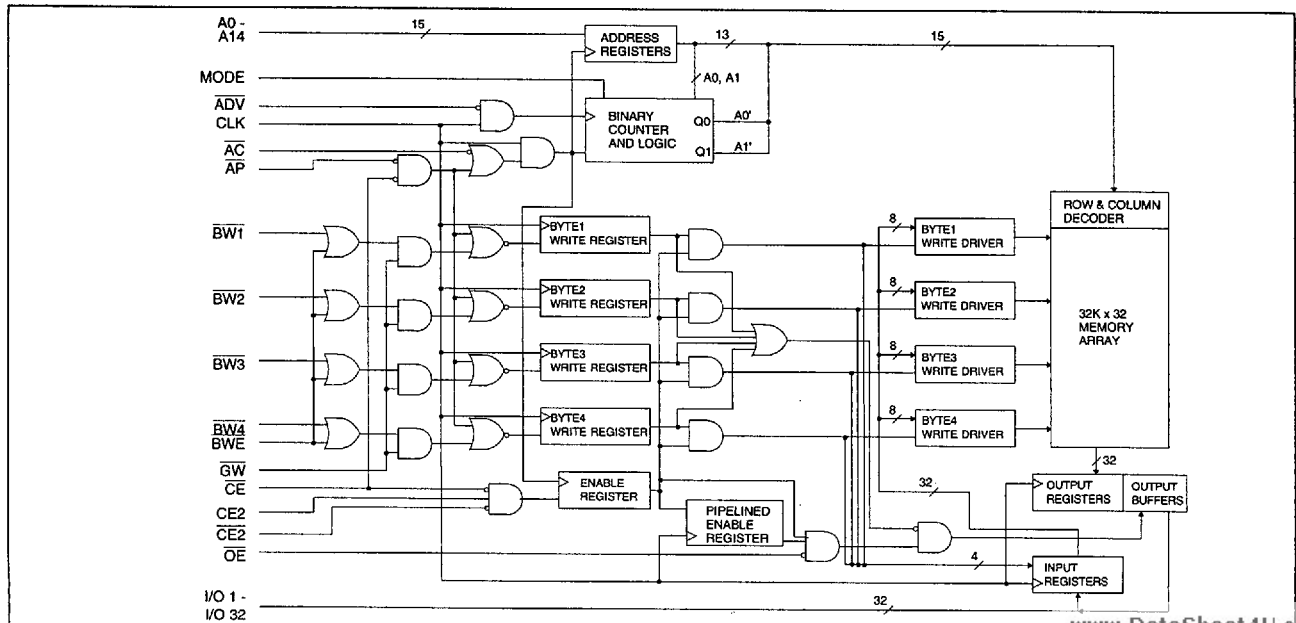


■ Description

The N343532L is a 32,768 x 32bits synchronous static RAM. The N343532L is suitable for applications which require high-

speed device, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

■ Functional Block Diagram





■ Pin Configuration

100 pin QFP/TQFP

Pin Description

| Symbol | PIN NAME |
|--------------|--|
| A0-A14 | Address input |
| I/O1 - I/O32 | Data input/output |
| ADV | Burst Address Advance |
| AC | Controller Address Status |
| AP | Processor Address Status |
| CE | Chip Enable input |
| CE2 | Chip Enable input |
| CE2 | Chip Enable input |
| BW1 - BW4 | Byte Write Enable, BW1 controls I/O1-8, BW2 controls I/O9-16, BW3 controls I/O17-24, BW4 controls I/O25-32 |
| BWE | Byte Write Enable |
| GW | Global Write Enable |
| OE | Output Enable input |
| CLK | System Clock input |
| MODE | Mode Select |
| FT | Flow-Through Pin |
| ZZ | Sleep Mode Pin |
| VCC | Power Supply Pin(+3.3V) |
| GND | Ground Pin |
| VCCQ | Power Supply Pin for Outputs (+3.3V) |
| GNDQ | Ground Pin for Outputs |
| NC | No Connection |

Note : MODE and FT are DC operated pins. Do not alter input state while device is operating.

■ Interleaved Burst Sequence Table (MODE = NC or VCC)

| | |
|-------------------|---|
| External Address | A14 - A2, A1, A0 |
| 1st Burst Address | A14 - A2, A1, $\overline{A0}$ |
| 2nd Burst Address | A14 - A2, $\overline{A1}$, A0 |
| 3rd Burst Address | A14 - A2, $\overline{A1}$, $\overline{A0}$ |

■ Linear Burst Sequence Table (MODE = GND)

| | | | | |
|-------------------|----------------|----------------|----------------|----------------|
| External Address | A14 - A2, 0, 0 | A14 - A2, 0, 1 | A14 - A2, 1, 0 | A14 - A2, 1, 1 |
| 1st Burst Address | A14 - A2, 0, 1 | A14 - A2, 1, 0 | A14 - A2, 1, 1 | A14 - A2, 0, 0 |
| 2nd Burst Address | A14 - A2, 1, 0 | A14 - A2, 1, 1 | A14 - A2, 0, 0 | A14 - A2, 0, 1 |
| 3rd Burst Address | A14 - A2, 1, 1 | A14 - A2, 0, 0 | A14 - A2, 0, 1 | A14 - A2, 1, 0 |

Note : The burst sequence wraps around to its initial state upon completion.


■ Asynchronous Truth Table

| Operation | ZZ | \overline{OE} | \overline{FT} | I/O |
|---|----|-----------------|-----------------|--------|
| Non-Pipelined Read Cycle ⁽³⁾ | L | L | L | Dout |
| Non-Pipelined Read Cycle ⁽³⁾ | L | H | L | High-Z |
| Pipelined Read Cycle | L | L | H | Dout |
| Pipelined Read Cycle | L | H | H | High-Z |
| Write Cycle | L | X | X | Din |
| Deselected | L | X | X | High-Z |
| Sleep | H | X | X | High-Z |

Note : (1) X = "don't care"

(2) For a write operation following a read operation, \overline{OE} must be high before the input data required setup time and held through the input data hold time.

(3) Normally, \overline{FT} is pulled to High or NC. \overline{FT} = Low is only used for a test mode.(Flow-Through Mode)

■ Synchronous Truth Table

| Operation | \overline{CE} | CE2 | CE2 | AP | \overline{AC} | ADV | \overline{WRITE} | CLK | Address | I/O |
|------------------------------|-----------------|-----|-----|----|-----------------|-----|--------------------|-----|----------|-------------|
| Deselected | H | X | X | X | L | X | X | ↑ | N/A | High-Z |
| Deselected | L | X | L | L | X | X | X | ↑ | N/A | High-Z |
| Deselected | L | H | X | L | X | X | X | ↑ | N/A | High-Z |
| Deselected | L | X | L | H | L | X | X | ↑ | N/A | High-Z |
| Deselected | L | H | X | H | L | X | X | ↑ | N/A | High-Z |
| Read Cycle / Begin Burst | L | L | H | L | X | X | X | ↑ | External | High-Z |
| Read Cycle / Begin Burst | L | L | H | H | L | X | H | ↑ | External | High-Z |
| Read Cycle / Continue Burst | X | X | X | H | H | L | H | ↑ | Next | Dout/High-Z |
| Read Cycle / Continue Burst | H | X | X | X | H | L | H | ↑ | Next | Dout/High-Z |
| Read Cycle / Suspend Burst | X | X | X | H | H | H | H | ↑ | Current | Dout/High-Z |
| Read Cycle / Suspend Burst | H | X | X | X | H | H | H | ↑ | Current | Dout/High-Z |
| Write Cycle / Begin Burst | L | L | H | H | L | X | L | ↑ | External | Din |
| Write Cycle / Continue Burst | X | X | X | H | H | L | L | ↑ | Next | Din |
| Write Cycle / Continue Burst | H | X | X | X | H | L | L | ↑ | Next | Din |
| Write Cycle / Suspend Burst | X | X | X | H | H | H | L | ↑ | Current | Din |
| Write Cycle / Suspend Burst | H | X | X | X | H | H | L | ↑ | Current | Din |

Note : (1) X = "don't care", \overline{WRITE} = L means any one or more byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) and \overline{BWE} are Low or \overline{GW} is Low.

\overline{WRITE} = H means all byte write enables and \overline{GW} are High.

(2) ADV must be High at the rising edge of the first clock after a AP cycle is initiated if a Write Cycle is desired.(to ensure use of correct address)

(3) Dout/High-Z means that the condition of the I/O's are controlled by \overline{OE} . I/O outputs data when \overline{OE} is Low, otherwise I/O = High-Z.

(4) The initial state of the registers at power up are not guaranteed.


■ Partial Truth Table for Write Enable

| Operation | $\overline{\text{GW}}$ | $\overline{\text{BWE}}$ | $\overline{\text{BW1}}$ | $\overline{\text{BW2}}$ | $\overline{\text{BW3}}$ | $\overline{\text{BW4}}$ |
|--------------------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Read Cycle | H | H | X | X | X | X |
| Read Cycle | H | L | H | H | H | H |
| Write Cycle / Byte1 only | H | L | L | H | H | H |
| Write Cycle / All Bytes | H | L | L | L | L | L |
| Write Cycle / All Bytes | L | X | X | X | X | X |

Note : (1) X = "don't care".

(2) Any one or more bytes may be written, using $\overline{\text{BWE}}$ and $\overline{\text{BW1}}$ through $\overline{\text{BW4}}$.

■ Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit | |
|-----------|--|-------------------|-------------------------------|---|
| Vcc, VccQ | Supply Voltage | -0.5 to 4.6 | V | |
| VTERM | Terminal Voltage with Respect to GND | CLK | -0.5 to Vcc+2.4 (Max. 6.0) | V |
| | | All Other Pins | -0.5 to Vcc+0.5 (Max. 4.6) | V |
| TOPR | Operating Temperature | 0 to 70 | °C | |
| TSTG | Storage Temperature | -55 to 150 | °C | |
| PD | Power Dissipation | 1.0 | W | |

NOTICE

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ Recommended Operating Conditions
Recommended DC Operating Conditions (TOPR = 0 to 70°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note | |
|-----------|--------------------|----------------|------|------|-------------------------|------|--|
| Vcc, VccQ | Supply Voltage | 3.1 | 3.3 | 3.6 | V | | |
| GND, GNDQ | Supply Voltage | 0 | 0 | 0 | V | | |
| VIH | Input High Voltage | I/O1 -I/O32 | 2.0 | | VccQ + 0.3 | V | |
| | | CLK | 2.0 | | Vcc + 2.4 (Max. 5.5) | V | |
| | | All Other Pins | 2.0 | | Vcc + 0.3 | V | |
| VIL | Input Low Voltage | -0.3 | | 0.8 | V | 1 | |

Note : (1) VIL(Min.) = -2.0V for pulse width less than 10ns.


■ Capacitance

(TOPR = 25°C, f = 1.0MHz)

| Symbol | Parameter | Condition | Max. | Unit |
|--------|--------------------|-----------|------|------|
| CIN | Input Capacitance | VIN = 0V | 6 | pF |
| COU | Output Capacitance | VOUT = 0V | 8 | pF |

Note : These parameters are sampled and not 100% tested.

■ DC Electrical Characteristics

 Power Supply Currents⁽¹⁾

(VCC = 3.3V + 0.3V/ - 0.2V, TOPR = 0 to 70°C)

| Symbol | Parameter | 66MHz | Unit | Note |
|--------|--|-------|------|------|
| ICC | Operating Supply Current Device selected, VIN ≤ VIL or ≥ VIH, I(I/O) = 0 | 185 | mA | |
| ISB | Standby Supply Current Device deselected, VIN ≤ VIL or ≥ VIH (0MHz) | 20 | mA | 2 |
| ISB1 | Standby Supply Current Device deselected, VIN ≤ 0.2V or ≥ VCC - 0.2V VIN(I/O) ≥ VCCQ - 0.2V or ≤ 0.2V (0MHz) | 2 | mA | 2 |
| ISB2 | Standby Supply Current Device deselected, VIN ≤ VIL or ≥ VIH | 50 | mA | |
| ISB3 | Sleep Mode Supply Current ZZ ≥ VCC - 0.2V | 2 | mA | |

Note : (1) All values are the maximum guaranteed values.

(2) All Inputs Static.

DC Characteristics

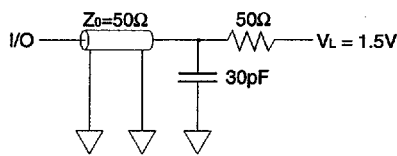
(VCC = 3.3V + 0.3V/ - 0.2V, TOPR = 0 to 70°C)

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|--------|--------------------------------------|------------------------------------|------|------|------|
| ILI | Input Leakage Current ⁽¹⁾ | VIN = GND to VCC | -2 | 2 | μA |
| ILO | Output Leakage Current | VOUT = GND to VCC, Output Disabled | -2 | 2 | μA |
| VOL | Output Low Voltage | IOL = 8mA | - | 0.4 | V |
| VOH | Output High Voltage | IOH = -5mA | 2.4 | - | V |

 Note : (1) MODE, \overline{FT} and ZZ pins are internally biased and exhibit an input leakage current of ± 400μA.

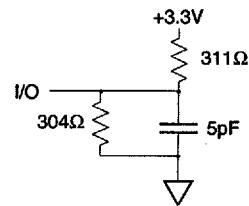

■ AC Test Conditions

| | |
|---------------------------------|--------------------|
| Input pulse levels | GND to 3.0V |
| Input pulse rise and fall times | 1.5ns |
| Input timing reference levels | 1.5V |
| Output timing reference levels | 1.5V |
| Output load | See Figure 1 and 2 |



(Including scope and jig)

Figure 1. Output Load Equivalent



(Including scope and jig)

 Figure 2. Output Load Equivalent
 (for tDC1, tOLZ, tOHZ, tCZ)


■ AC Electrical Characteristics

Read and Write Cycle

(VCC = 3.3V + 0.3V/ - 0.2V, TOPR = 0 to 70°C)

| Parameter | Symbol | | 66MHz | | Unit |
|-----------------------------|---------------------|------------------|-------|-------|------|
| | Standard | Alternative | Min. | Max. | |
| Cycle Time | t _{KHKH} | t _{CYC} | 15.0 | | ns |
| Clock Access Time | t _{KHQV} | t _{CD} | | 7.0 | ns |
| OE Enable to Output Valid | t _{GLQV} | t _{OE} | | 5.0 | ns |
| Clock High to Output Active | t _{KHQX1} | t _{DC1} | 0.0 | | ns |
| Clock High to Output Change | t _{KHQX2} | t _{DC2} | 2.0 | | ns |
| OE Enable to Output Active | t _{GLQX} | t _{OLZ} | 0.0 | | ns |
| OE Disable to Output High-Z | t _{GHQZ} | t _{OHZ} | | 5.0 | ns |
| Clock High to Output High-Z | t _{KHQZ} | t _{CZ} | 2.0 | 15.0 | ns |
| Clock High Pulse Width | t _{KHKL} | t _{CH} | 5.0 | | ns |
| Clock Low Pulse Width | t _{KLKH} | t _{CL} | 5.0 | | ns |
| Setup Times : Address | t _{AVKH} | t _{AS} | 2.5 | | ns |
| Address Status | t _{ADSVKH} | t _{SS} | 2.5 | | ns |
| Data In | t _{DVKH} | t _{DS} | 2.5 | | ns |
| Write Enable | t _{WVKH} | t _{WS} | 2.5 | | ns |
| Address Advance | t _{ADVVKH} | | 2.5 | | ns |
| Chip Enable | t _{EVKH} | | 2.5 | | ns |
| Hold Times : Address | t _{KHAX} | t _{AH} | 0.5 | | ns |
| Address Status | t _{KHADSX} | t _{SH} | 0.5 | | ns |
| Data In | t _{KHDX} | t _{DH} | 0.5 | | ns |
| Write Enable | t _{KHWX} | t _{WH} | 0.5 | | ns |
| Address Advance | t _{KHADVX} | | 0.5 | | ns |
| Chip Enable | t _{KHEX} | | 0.5 | | ns |
| ZZ Standby Time | t _{ZZS} | | | 100.0 | ns |
| ZZ Recovery Time | t _{ZZREC} | | 100.0 | | ns |

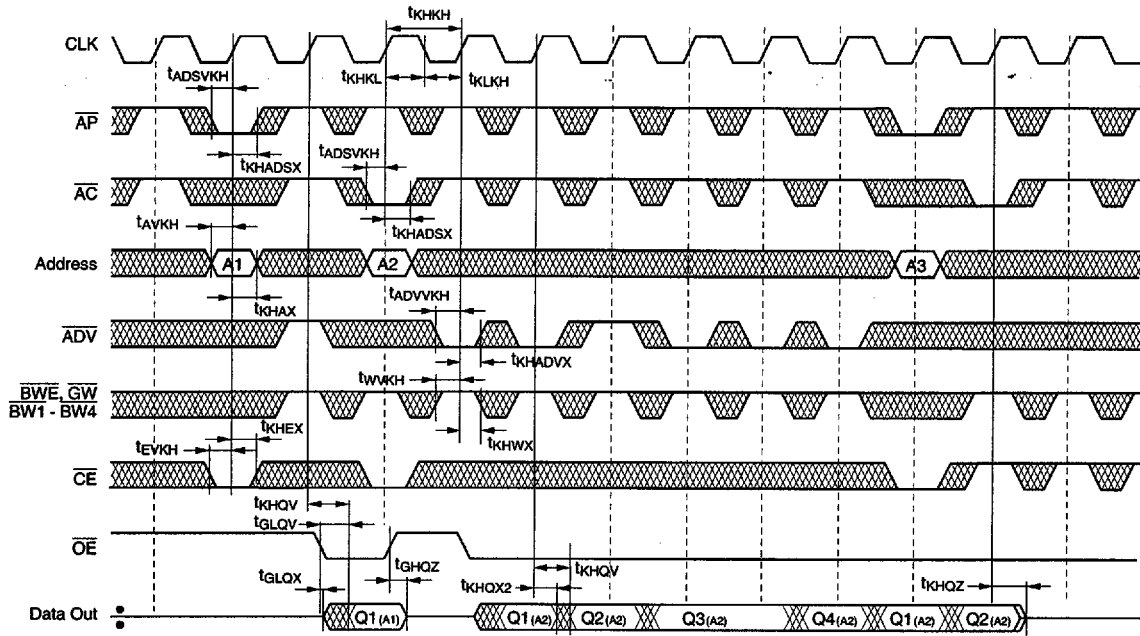
 Note : (1) t_{DC1}, t_{OLZ}, t_{OHZ} and t_{CZ} are sampled and not 100% tested.

(2) ZZ may be asserted at any time but must meet the required standby and recovery times.



■ AC Timing Waveforms

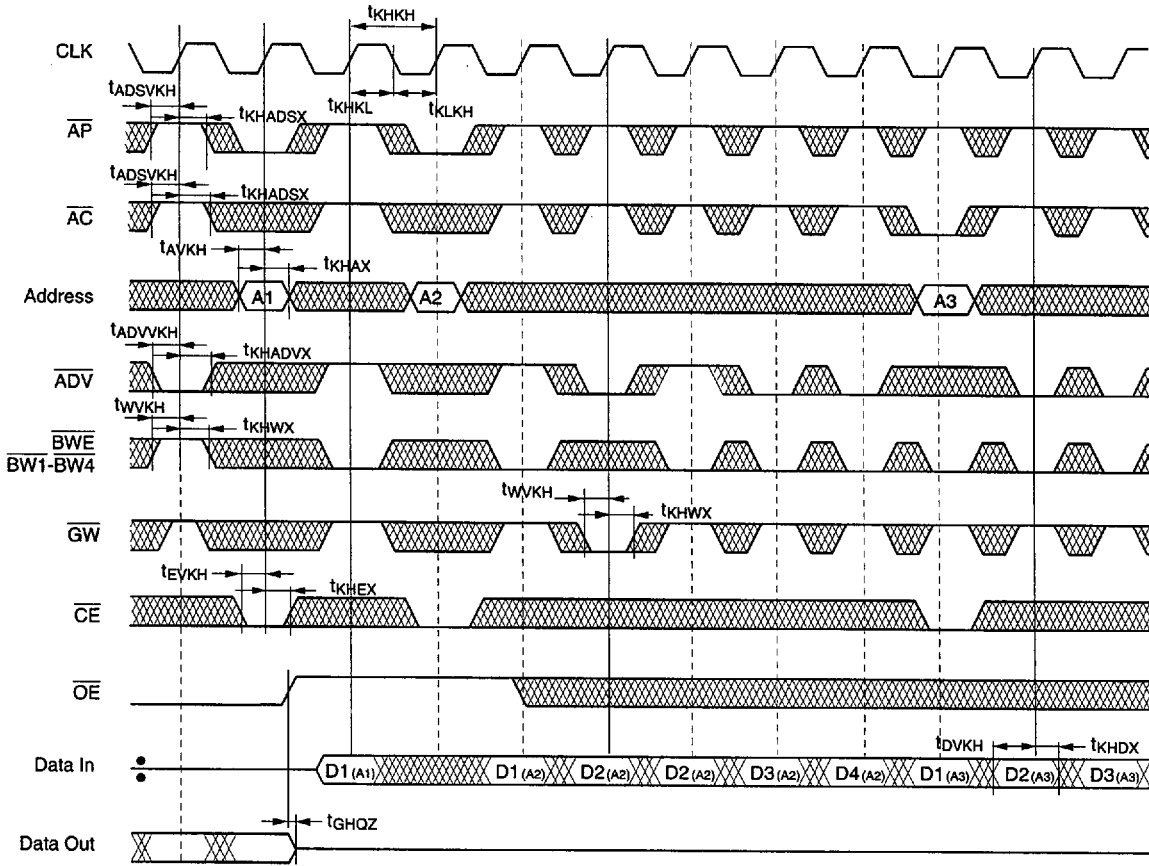
Read Cycle



- Note : (1) $Q_n(A2)$ refers to output from address A2. Q1 - Q4 refers to outputs according to burst sequence.
 (2) $\overline{CE2}$ and CE2 have the same timing as \overline{CE} . In this timing, when \overline{CE} is Low, $\overline{CE2}$ is Low and CE2 is High. When \overline{CE} is High, $\overline{CE2}$ is High and CE2 is Low.

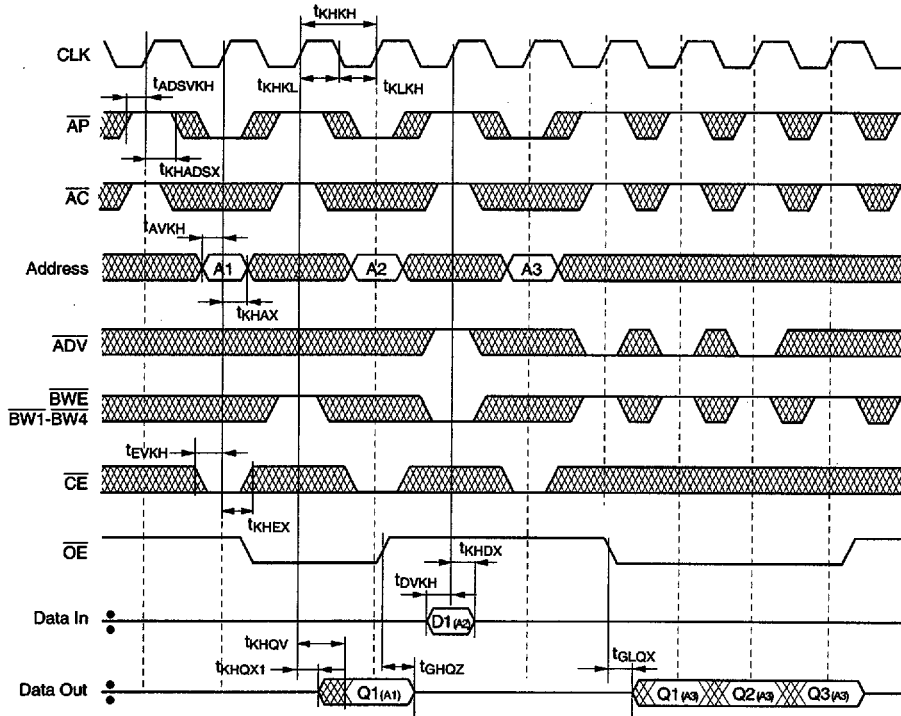


Write Cycle



- Note : (1) $\overline{CE2}$ and $CE2$ have the same timing as \overline{CE} . In this timing, when \overline{CE} is Low, $\overline{CE2}$ is Low and $CE2$ is High. When \overline{CE} is High, $\overline{CE2}$ is High and $CE2$ is Low.
- (2) \overline{BWE} is Low when any one or more Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ and $\overline{BW4}$) are Low in this diagram.

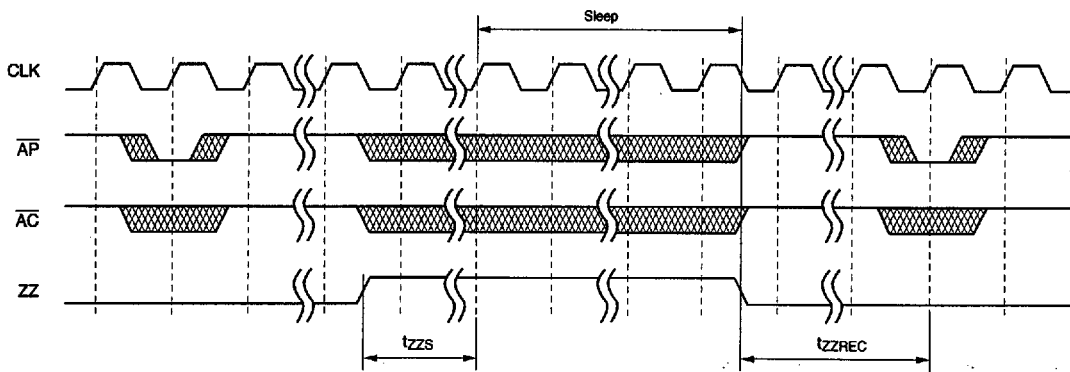
Read/Write Cycle



Note : (1) $\overline{CE2}$ and CE2 have the same timing as \overline{CE} . In this timing, when \overline{CE} is Low, $\overline{CE2}$ is Low and CE2 is High. When \overline{CE} is High, $\overline{CE2}$ is High and CE2 is Low.

(2) \overline{GW} is High in this diagram.

Sleep Mode Cycle



Note : (1) Data retention is guaranteed when ZZ is asserted and clock remains active.

(2) \overline{AC} and \overline{AP} must not be asserted for a least 100ns after leaving ZZ state.

(3) Do not assert ZZ during a write operation.

(4) \overline{AP} and \overline{AC} must be high at the rising edge of CLK when the transition of ZZ from High to Low or Low to High occurs.



■ Ordering Information

N343532L Δ Δ - X □

Package Speed Function

N 5V tolerant Clock pin/Sleep mode/Flow Through

7 ns

QF QFP

TQ TQFP

| PART NO. | Access Time (ns) | Clock Frequency (MHz) | Operating Current (mA) | Package |
|---------------|---------------------|--------------------------|---------------------------|-------------|
| N343532LQF-7N | 7 | 66 | 185 | 100Pin QFP |
| N343532LTQ-7N | 7 | 66 | 185 | 100Pin TQFP |