Independent Clock HOTLink II™ Serializer and Reclocking Deserializer

Features

- **Single channel video serializer plus single channel video reclocking deserializer**
  - **195- to 1500-Mbps serial data signaling rate**
  - **Simultaneous operation at different signaling rates**
- **Second-generation HOTLink® technology**
- **Compliant to SMPTE 292M and SMPTE 259M video standards**
- **Supports reception of either 1.485 or 1.485/1.001 Gbps data rate with the same training clock**
- **Internal phase-locked loops (PLLs) with no external PLL components**
- **Supports half-rate and full-rate clocking**
- **Selectable differential PECL-compatible serial inputs**
  - **Internal DC-restoration**
- **Redundant differential PECL-compatible serial outputs**
  - **No external bias resistors required**
  - **Internal source termination**
  - **Signaling-rate controlled edge-rates**
- **Synchronous LVTTL parallel interface**
- **JTAG boundary scan**
- **Built-In Self-Test (BIST) for at-speed link testing**
- **Link Quality Indicator**
  - **Analog signal detect**
  - **Digital signal detect**
- **Low-power 1.8W @ 3.3V typical**
- **Single 3.3V supply**
- **Thermally enhanced BGA**
- **0.25µ BiCMOS technology**

Functional Description

The CYV15G0104TRB Independent Clock HOTLink II™ Serializer and Reclocking Deserializer is a point-to-point or point-to-multipoint communications building block enabling transfer of data over a variety of high-speed serial links including SMPTE 292M and SMPTE 259M video applications. It supports signaling rates in the range of 195 to 1500 Mbps per serial link. The transmit and receive channels are independent and can operate simultaneously at different rates. The transmit channel accepts 10-bit parallel characters in an Input Register and converts them to serial data. The receive channel accepts serial data and converts it to 10-bit parallel characters and presents these characters to an Output Register. The received serial data can also be reclocked and retransmitted through the reclocker serial outputs. *Figure 1* illustrates typical connections between independent video co-processors and corresponding CYV15G0104TRB chips.

The CYV15G0104TRB satisfies the SMPTE 259M and SMPTE 292M compliance as per SMPTE EG34-1999 Pathological Test Requirements.

As a second-generation HOTLink device, the CYV15G0104TRB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data and BIST) with other HOTLink devices. The transmit (TX) channel of the CYV15G0104TRB HOTLink II device accepts scrambled 10-bit transmission characters. These characters are serialized and output from dual Positive ECL (PECL) compatible differential transmission-line drivers at a bit-rate of either 10- or 20-times the input reference clock for that channel.

The receive (RX) channel of the CYV15G0104TRB HOTLink II device accepts a serial bit-stream from one of two selectable PECL-compatible differential line receivers, and using a completely integrated Clock and Data Recovery PLL, recovers the timing information necessary for data reconstruction. The recovered bit-stream is reclocked and retransmitted through the reclocker serial outputs. Also, the recovered serial data is deserialized and presented to the destination host system.

The transmit and receive channels contain an independent BIST pattern generator and checker, respectively. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit and receive section, and across the interconnecting links.

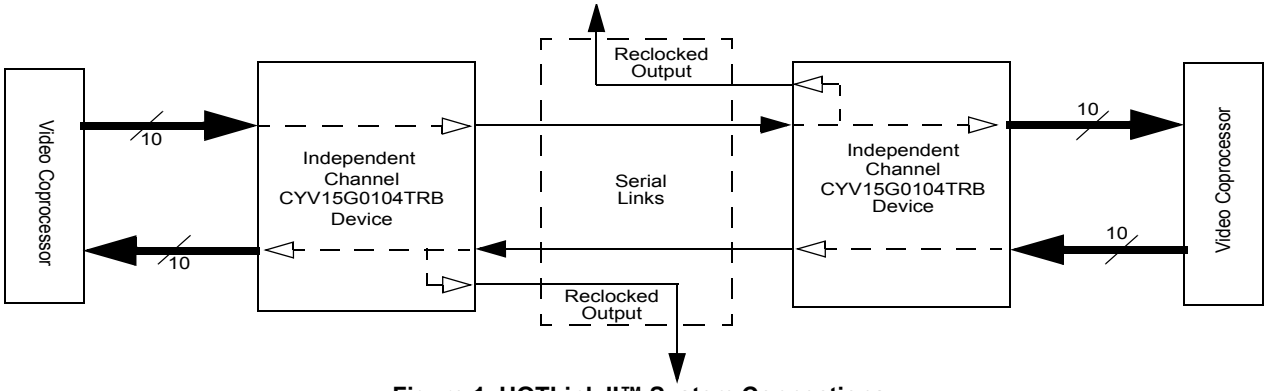
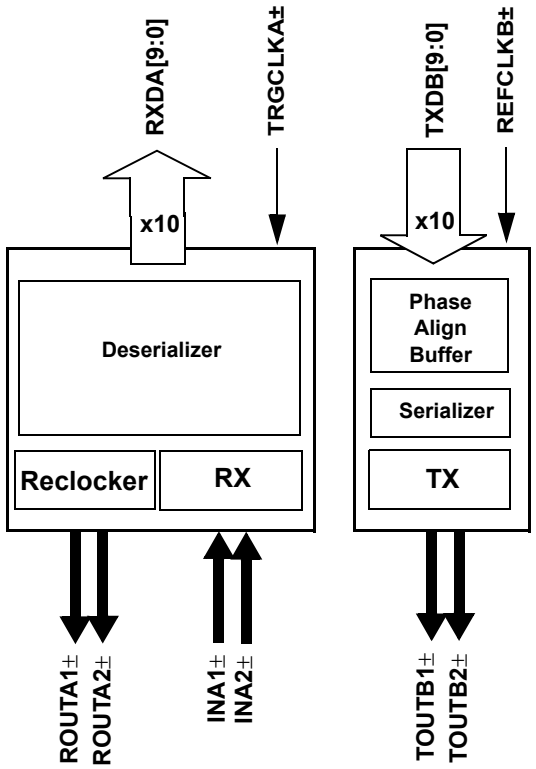


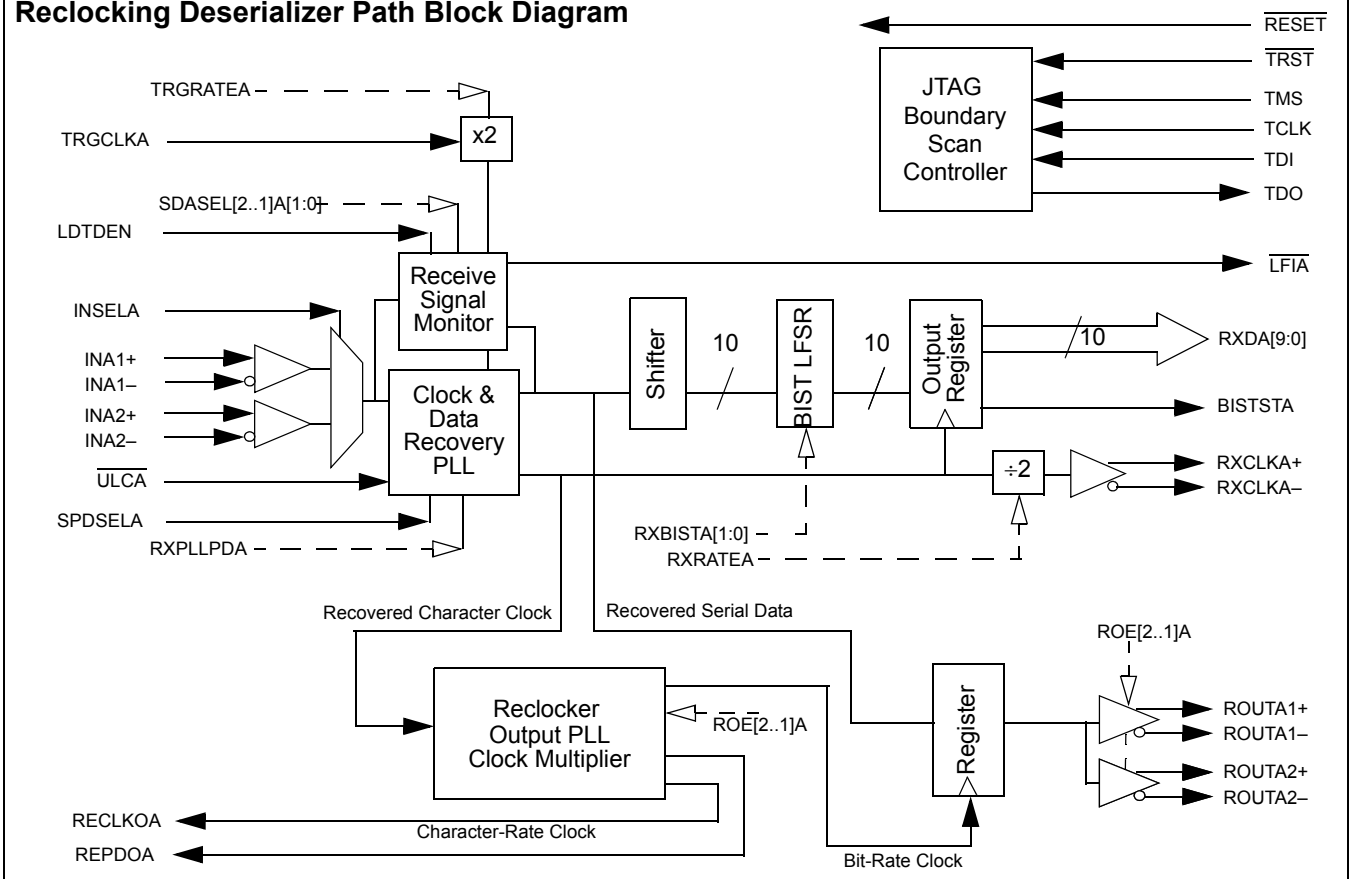
Figure 1. HOTLink II™ System Connections

The CYV15G0104TRB is ideal for SMPTE applications where different data rates and serial interface standards are necessary for each channel. Some applications include multi-format routers, switchers, format converters, SDI monitors, cameras, and camera control units.

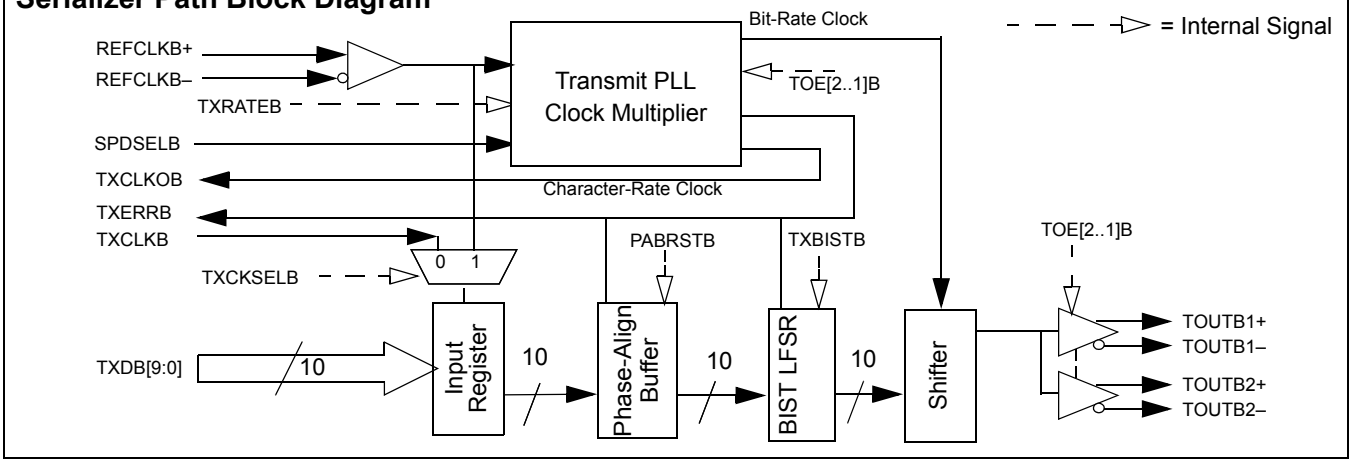
CYV15G0104TRB Serializer and Reclocking Deserializer Logic Block Diagram



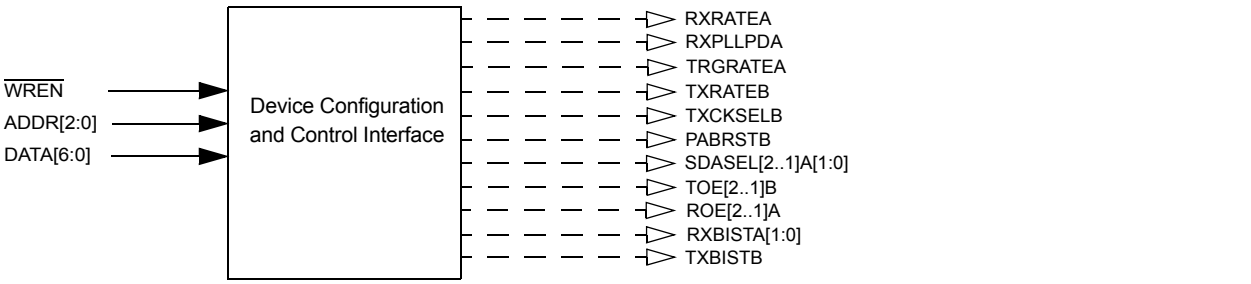
Reclocking Deserializer Path Block Diagram



Serializer Path Block Diagram



Device Configuration and Control Block Diagram



Pin Configuration (Top View)[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	NC	NC	NC	V_{CC}	NC	TOUT B1–	GND	GND	TOUT B2–	IN A1–	ROUT A1–	GND	IN A2–	ROUT A2–	V_{CC}	V_{CC}	NC	V_{CC}	NC
B	V_{CC}	NC	V_{CC}	NC	V_{CC}	V_{CC}	TOUT B1+	GND	NC	TOUT B2+	IN A1+	ROUT A1+	GND	IN A2+	ROUT A2+	V_{CC}	NC	NC	NC	NC
C	TDI	TMS	V_{CC}	V_{CC}	V_{CC}	NC	NC	GND	DATA [6]	DATA [4]	DATA [2]	DATA [0]	GND	NC	SPD SELB	V_{CC}	LDTD EN	$\overline{TRST}$	GND	TDO
D	TCLK	$\overline{RESET}$	V_{CC}	INSELA	V_{CC}	$\overline{ULCA}$	NC	GND	DATA [5]	DATA [3]	DATA [1]	GND	GND	GND	NC	V_{CC}	NC	V_{CC}	SCAN EN2	TMEN3
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	NC	NC	V_{CC}	NC													V_{CC}	NC	NC	NC
G	GND	$\overline{WREN}$	GND	GND													NC	NC	SPD SELA	NC
H	GND	GND	GND	GND													GND	GND	GND	GND
J	GND	GND	GND	GND													NC	NC	NC	NC
K	NC	NC	GND	GND													NC	NC	NC	NC
L	NC	NC	NC	GND													NC	NC	NC	GND
M	NC	NC	NC	NC													NC	NC	NC	GND
N	GND	GND	GND	GND													GND	GND	GND	GND
P	NC	NC	NC	NC													GND	GND	GND	GND
R	NC	NC	NC	NC													V_{CC}	V_{CC}	V_{CC}	V_{CC}
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	TX DB[0]	TX DB[1]	TX DB[2]	TX DB[9]	V_{CC}	NC	NC	GND	GND	ADDR [0]	REF CLKB–	GND	GND	GND	V_{CC}	V_{CC}	RX DA[4]	V_{CC}	BIST STA	RX DA[0]
V	TX DB[3]	TX DB[4]	TX DB[8]	NC	V_{CC}	NC	NC	GND	NC	GND	REF CLKB+	RE CLKOA	GND	GND	V_{CC}	V_{CC}	RX DA[9]	RX DA[5]	RX DA[2]	RX DA[1]
W	TX DB[5]	TX DB[7]	NC	NC	V_{CC}	NC	NC	GND	ADDR [2]	ADDR [1]	RX CLKA+	REPDO A	GND	GND	V_{CC}	V_{CC}	$\overline{LFIA}$	TRG CLKA+	RX DA[6]	RX DA[3]
Y	TX DB[6]	TX CLKB	NC	NC	V_{CC}	NC	NC	GND	TX CLKOB	NC	GND	RX CLKA–	GND	GND	V_{CC}	V_{CC}	TX ERRB	TRG CLKA–	RX DA[8]	RX DA[7]

1. NC = Do not connect.

Pin Configuration (Bottom View)[1]

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	V_{CC}	NC	V_{CC}	V_{CC}	ROUT A2–	IN A2–	GND	ROUT A1–	IN A1–	TOUT B2–	GND	GND	TOUT B1–	NC	V_{CC}	NC	NC	NC	NC
B	NC	NC	NC	NC	V_{CC}	ROUT A2+	IN A2+	GND	ROUT A1+	IN A1+	TOUT B2+	NC	GND	TOUT B1+	V_{CC}	V_{CC}	NC	V_{CC}	NC	V_{CC}
C	TDO	GND	$\overline{TRST}$	LDTD EN	V_{CC}	SPD SELB	NC	GND	DATA [0]	DATA [2]	DATA [4]	DATA [6]	GND	NC	NC	V_{CC}	V_{CC}	V_{CC}	TMS	TDI
D	TMEN3	SCAN EN2	V_{CC}	NC	V_{CC}	NC	GND	GND	GND	DATA [1]	DATA [3]	DATA [5]	GND	NC	$\overline{ULCA}$	V_{CC}	INSELA	V_{CC}	$\overline{RESET}$	TCLK
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	NC	NC	NC	V_{CC}													NC	V_{CC}	NC	NC
G	NC	SPD SELA	NC	NC													GND	GND	$\overline{WREN}$	GND
H	GND	GND	GND	GND													GND	GND	GND	GND
J	NC	NC	NC	NC													GND	GND	GND	GND
K	NC	NC	NC	NC													GND	GND	NC	NC
L	GND	NC	NC	NC													GND	NC	NC	NC
M	GND	NC	NC	NC													NC	NC	NC	NC
N	GND	GND	GND	GND													GND	GND	GND	GND
P	GND	GND	GND	GND													NC	NC	NC	NC
R	V_{CC}	V_{CC}	V_{CC}	V_{CC}													NC	NC	NC	NC
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	RX DA[0]	BIST STA	V_{CC}	RX DA[4]	V_{CC}	V_{CC}	GND	GND	GND	REF CLKB–	ADDR [0]	GND	GND	NC	NC	V_{CC}	TX DB[9]	TX DB[2]	TX DB[1]	TX DB[0]
V	RX DA[1]	RX DA[2]	RX DA[5]	RX DA[9]	V_{CC}	V_{CC}	GND	GND	RE CLKOA	REF CLKB+	GND	NC	GND	NC	NC	V_{CC}	NC	TX DB[8]	TX DB[4]	TX DB[3]
W	RX DA[3]	RX DA[6]	TRG CLKA+	$\overline{LFIA}$	V_{CC}	V_{CC}	GND	GND	REPDO A	RX CLKA+	ADDR [1]	ADDR [2]	GND	NC	NC	V_{CC}	NC	NC	TX DB[7]	TX DB[5]
Y	RX DA[7]	RX DA[8]	TRG CLKA–	TX ERRB	V_{CC}	V_{CC}	GND	GND	RX CLKA–	GND	NC	TX CLKOB	GND	NC	NC	V_{CC}	NC	NC	TX CLKB	TX DB[6]

Pin Definitions
CYV15G0104TRB HOTLink II Serializer and Reclocking Deserializer

Name	I/O Characteristics	Signal Description
Transmit Path Data and Status Signals		
TXDB[9:0]	LVTTL Input, synchronous, sampled by TXCLKB↑ or REFCLKB↑[2]	**Transmit Data Inputs**. TXDB[9:0] data inputs are captured on the rising edge of the transmit interface clock. The transmit interface clock is selected by the TXCKSELB latch via the device configuration interface.
TXERRB	LVTTL Output, synchronous to REFCLKB↑ [3], asynchronous to transmit channel enable / disable, asynchronous to loss or return of REFCLKB±	**Transmit Path Error**. TXERRB is asserted HIGH to indicate detection of a transmit Phase-Align Buffer underflow or overflow. If an underflow or overflow condition is detected, TXERRB, is asserted HIGH and remains asserted until the transmit Phase-Align Buffer is re-centered with the PABRSTB latch via the device configuration interface. When TXBISTB = 0, the BIST progress is presented on the TXERRB output. The TXERRB signal pulses HIGH for one transmit-character clock period to indicate a pass through the BIST sequence once every 511 character times. TXERRB is also asserted HIGH, when any of the following conditions is true: • The TXPLL is powered down. This occurs when TOE2B and TOE1B are both disabled by setting TOE2B = 0 and TOE1B = 0. • The absence of the REFCLKB± signal.
Transmit Path Clock Signals		
REFCLKB±	Differential LVPECL or single-ended LVTTL input clock	**Reference Clock**. REFCLKB± clock inputs are used as the timing reference for the transmit PLL. This input clock may also be selected to clock the transmit parallel interface. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLKB input, and leave the alternate REFCLKB input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs.
TXCLKB	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clock**. When configuration latch TXCKSELB = 0, the associated TXCLKB input is selected as the character-rate input clock for the TXDB[9:0] input. In this mode, the TXCLKB input must be frequency-coherent to its TXCLKOB output clock, but may be offset in phase by any amount. Once initialized, TXCLKB is allowed to drift in phase by as much as ±180 degrees. If the input phase of TXCLKB drifts beyond the handling capacity of the Phase Align Buffer, TXERRB is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of TXCLKB relative to REFCLKB± is initialized when the configuration latch PABRSTB is written as 0. When TXERRB is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured.
TXCLKOB	LVTTL Output	**Transmit Clock Output**. TXCLKOB output clock is synthesized by the transmit PLL and operates synchronous to the internal transmit character clock. TXCLKOB operates at either the same frequency as REFCLKB± (TXRATEB = 0), or at twice the frequency of REFCLKB± (TXRATEB = 1). The transmit clock outputs have no fixed phase relationship to REFCLKB±.
Receive Path Data and Status Signals		
RXDA[9:0]	LVTTL Output, synchronous to the RXCLKA ± output	**Parallel Data Output**. RXDA[9:0] parallel data outputs change relative to the receive interface clock. If RXCLKA± is a full-rate clock, the RXCLKA± clock outputs are complementary clocks operating at the character rate. The RXDA[9:0] outputs for the associated receive channels follow rising edge of RXCLKA+ or falling edge of RXCLKA–. If RXCLKA± is a half-rate clock, the RXCLKA± clock outputs are complementary clocks operating at half the character rate. The RXDA[9:0] outputs for the associated receive channels follow both the falling and rising edges of the associated RXCLKA± clock outputs. When BIST is enabled on the receive channel, the BIST status is presented on the RXDA[1:0] and BISTSTA outputs. See *Table 6* for each status reported by the BIST state machine. Also, while BIST is enabled, the RXDA[9:2] outputs should be ignored.

Notes:
2. When REFCLKB± is configured for half-rate operation, these inputs are sampled relative to both the rising and falling edges of the associated REFCLKB±.
3. When REFCLKB± is configured for half-rate operation, this output is presented relative to both the rising and falling edges of the associated REFCLKB±.

Pin Definitions (continued)
CYV15G0104TRB HOTLink II Serializer and Reclocking Deserializer

Name	I/O Characteristics	Signal Description
BISTSTA	LVTTL Output, synchronous to the RXCLKA ± output	**BIST Status Output.** When RXBISTA[1:0] = 10, BISTSTA (along with RXDA[1:0]) displays the status of the BIST reception. See *Table 6* for the BIST status reported for each combination of BISTSTA and RXDA[1:0]. When RXBISTA[1:0] ≠ 10, BISTSTA should be ignored.
REPDOA	Asynchronous to reclocker output channel enable / disable	**Reclocker Powered Down Status Output.** REPDOA is asserted HIGH, when the reclocker output logic is powered down. This occurs when ROE2A and ROE1A are both disabled by setting ROE2A = 0 and ROE1A = 0.
Receive Path Clock Signals		
TRGCLKA±	Differential LVPECL or single-ended LVTTL input clock	**CDR PLL Training Clock**. TRGCLKA± clock inputs are used as the reference source for the frequency detector (Range Controller) of the receive PLL to reduce PLL acquisition time. In the presence of valid serial data, the recovered clock output of the receive CDR PLL (RXCLKA±) has no frequency or phase relationship with TRGCLKA±. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement TRGCLKA input, and leave the alternate TRGCLKA input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs.
RXCLKA±	LVTTL Output Clock	**Receive Clock Output**. RXCLKA± is the receive interface clock used to control timing of the RXDA[9:0] parallel outputs. These true and complement clocks are used to control timing of data output transfers. These clocks are output continuously at either the half-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATEA.
RECLKOA	LVTTL Output	**Reclocker Clock Output**. RECLKOA output clock is synthesized by the reclocker output PLL and operates synchronous to the internal recovered character clock. RECLKOA operates at either the same frequency as RXCLKA± (RXRATEA = 0), or at twice the frequency of RXCLKA± (RXRATEA = 1).The reclocker clock outputs have no fixed phase relationship to RXCLKA±.
Device Control Signals		
$\overline{\text{RESET}}$	LVTTL Input, asynchronous, internal pull-up	**Asynchronous Device Reset**. $\overline{\text{RESET}}$ initializes all state machines, counters, and configuration latches in the device to a known state. $\overline{\text{RESET}}$ must be asserted LOW for a minimum pulse width. When the reset is removed, all state machines, counters and configuration latches are at an initial state. See *Table 4* for the initialize values of the device configuration latches.
LDTDEN	LVTTL Input, internal pull-up	**Level Detect Transition Density Enable**. When LDTDEN is HIGH, the Signal Level Detector, Range Controller, and Transition Density Detector are all enabled to determine if the RXPLL tracks TRGCLKA± or the selected input serial data stream. If the Signal Level Detector, Range Controller, or Transition Density Detector are out of their respective limits while LDTDEN is HIGH, the RXPLL locks to TRGCLKA± until such a time they become valid. SDASEL[2..1]A[1:0] is used to configure the trip level of the Signal Level Detector. The Transition Density Detector limit is one transition in every 60 consecutive bits. When LDTDEN is LOW, only the Range Controller is used to determine if the RXPLL tracks TRGCLKA± or the selected input serial data stream. it is recommended to set LDTDEN = HIGH.
$\overline{\text{ULCA}}$	LVTTL Input, internal pull-up	**Use Local Clock**. When $\overline{\text{ULCA}}$ is LOW, the RXPLL is forced to lock to TRGCLKA± instead of the received serial data stream. While $\overline{\text{ULCA}}$ is LOW, the link fault indicator LFIA is LOW indicating a link fault. When $\overline{\text{ULCA}}$ is HIGH, the RXPLL performs Clock and Data Recovery functions on the input data streams. This function is used in applications in which a stable RXCLKA± is needed. In cases when there is an absence of valid data transitions for a long period of time, or the high-gain differential serial inputs (INA±) are left floating, there may be brief frequency excursions of the RXCLKA± outputs from TRGCLKA±.

Pin Definitions (continued)

CYV15G0104TRB HOTLink II Serializer and Reclocking Deserializer

Name	I/O Characteristics	Signal Description
SPDSELA SPDSELB	3-Level Select[4] static control input	**Serial Rate Select**. The SPDSELA and SPDSELB inputs specify the operating signaling-rate range of the receive and transmit PLL, respectively. LOW = 195 – 400 MBd MID = 400 – 800 MBd HIGH = 800 – 1500 MBd.
INSELA	LVTTL Input, asynchronous	**Receive Input Selector**. The INSELA input determines which external serial bit stream is passed to the receiver's Clock and Data Recovery circuit. When INSELA is HIGH, the Primary Differential Serial Data Input, INA1±, is selected for the receive channel. When INSELA is LOW, the Secondary Differential Serial Data Input, INA2±, is selected for the receive channel.
$\overline{\text{LFIA}}$	LVTTL Output, asynchronous	**Link Fault Indication Output**. $\overline{\text{LFIA}}$ is an output status indicator signal. $\overline{\text{LFIA}}$ is the logical OR of six internal conditions. $\overline{\text{LFIA}}$ is asserted LOW when any of the following conditions is true: • Received serial data rate outside expected range • Analog amplitude below expected levels • Transition density lower than expected • Receive channel disabled • $\overline{\text{ULCA}}$ is LOW • Absence of TRGCLKA±.
Device Configuration and Control Bus Signals		
$\overline{\text{WREN}}$	LVTTL input, asynchronous, internal pull-up	**Control Write Enable**. The $\overline{\text{WREN}}$ input writes the values of the DATA[6:0] bus into the latch specified by the address location on the ADDR[2:0] bus.[5]
ADDR[2:0]	LVTTL input asynchronous, internal pull-up	**Control Addressing Bus**. The ADDR[2:0] bus is the input address bus used to configure the device. The $\overline{\text{WREN}}$ input writes the values of the DATA[6:0] bus into the latch specified by the address location on the ADDR[2:0] bus.[5] *Table 4* lists the configuration latches within the device, and the initialization value of the latches upon the assertion of RESET. *Table 5* shows how the latches are mapped in the device.
DATA[6:0]	LVTTL input asynchronous, internal pull-up	**Control Data Bus**. The DATA[6:0] bus is the input data bus used to configure the device. The $\overline{\text{WREN}}$ input writes the values of the DATA[6:0] bus into the latch specified by address location on the ADDR[2:0] bus.[5] *Table 4* lists the configuration latches within the device, and the initialization value of the latches upon the assertion of RESET. *Table 5* shows how the latches are mapped in the device.
Internal Device Configuration Latches		
RXRATEA	Internal Latch[6]	**Receive Clock Rate Select**.
SDASEL[2..1]A[1:0]	Internal Latch[6]	**Signal Detect Amplitude Select**.
TXCKSELB	Internal Latch[6]	**Transmit Clock Select**.
TXRATEB	Internal Latch[6]	**Transmit PLL Clock Rate Select**.
TRGRATEA	Internal Latch[6]	**Reclocker Output PLL Clock Rate Select**.
RXPLLPDA	Internal Latch[6]	**Receive Channel Power Control**.
RXBISTA[1:0]	Internal Latch[6]	**Receive Bist Disabled**.
TXBISTB	Internal Latch[6]	**Transmit Bist Disabled**.
TOE2B	Internal Latch[6]	**Transmitter Differential Serial Output Driver 2 Enable**.
TOE1B	Internal Latch[6]	**Transmitter Differential Serial Output Driver 1 Enable**.

Notes:

4. 3-Level Select inputs are used for static configuration. These are ternary inputs that make use of logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). The MID level is usually implemented by not connecting the input (left floating), which allows it to self bias to the proper level.
5. See *Device Configuration and Control Interface* for detailed information on the operation of the Configuration Interface.
6. See *Device Configuration and Control Interface* for detailed information on the internal latches.

Pin Definitions (continued)

CYV15G0104TRB HOTLink II Serializer and Reclocking Deserializer

Name	I/O Characteristics	Signal Description
ROE2A	Internal Latch[6]	**Reclocker Differential Serial Output Driver 2 Enable**.
ROE1A	Internal Latch[6]	**Reclocker Differential Serial Output Driver 1 Enable**.
PABRSTB	Internal Latch[6]	**Transmit Clock Phase Alignment Buffer Reset**.
Factory Test Modes		
SCANEN2	LVTTL input, internal pull-down	**Factory Test 2.** SCANEN2 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
TMEN3	LVTTL input, internal pull-down	**Factory Test 3**. TMEN3 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
Analog I/O		
TOUTB1±	CML Differential Output	**Transmitter Primary Differential Serial Data Output**. The transmitter TOUTB1± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
TOUTB2±	CML Differential Output	**Transmitter Secondary Differential Serial Data Output**. The transmitter TOUTB2± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
ROUTA1±	CML Differential Output	**Reclocker Primary Differential Serial Data Output**. The reclocker ROUTA1± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
ROUTA2±	CML Differential Output	**Reclocker Secondary Differential Serial Data Output**. The reclocker ROUTA2± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
INA1±	Differential Input	**Primary Differential Serial Data Input**. The INA1± input accepts the serial data stream for deserialization. The INA1± serial stream is passed to the receive CDR circuit to extract the data content when INSELA = HIGH.
INA2±	Differential Input	**Secondary Differential Serial Data Input**. The INA2± input accepts the serial data stream for deserialization. The INA2± serial stream is passed to the receiver CDR circuit to extract the data content when INSELA = LOW.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**.
TDO	3-State LVTTL Output	**Test Data Out**. JTAG data output buffer. High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
$\overline{\text{TRST}}$	LVTTL Input, internal pull-up	**JTAG reset signal**. When asserted (LOW), this input asynchronously resets the JTAG test access port controller.
Power		
V_{CC}		**+3.3V Power**.
GND		**Signal and Power Ground for all internal circuits**.

CYV15G0104TRB HOTLink II Operation

The CYV15G0104TRB is a highly configurable, independent clocking device designed to support reliable transfer of large quantities of digital video data, using high-speed serial links from multiple sources to multiple destinations.

CYV15G0104TRB Transmit Data Path

Input Register

The parallel input bus TXDB[9:0] can be clocked in using TXCLKB (TXCKSELB = 0) or REFCLKB (TXCKSELB = 1).

Phase-Align Buffer

Data from the Input Register is passed to the Phase-Align Buffer, when the TXDB[9:0] input register is clocked using TXCLKBA (TXCKSELB = 0) or when REFCLKB is a half-rate clock (TXCKSELB = 1 and TXRATEB = 1). When the TXDB[9:0] input register is clocked using REFCLKB± (TXCKSELA = 1) and REFCLKB± is a full-rate clock (TXRATEB = 0), the associated Phase Alignment Buffer in the transmit path is bypassed. These buffers are used to absorb clock phase differences between the TXCLKB input clock and the internal character clock for that channel.

Once initialized, TXCLKB is allowed to drift in phase as much as ±180 degrees. If the input phase of TXCLKB drifts beyond the handling capacity of the Phase Align Buffer, TXERRB is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of TXCLKB relative to its internal character rate clock is initialized when the configuration latch PABRSTB is written as 0. When the associated TXERRB is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured.

If the phase offset, between the initialized location of the input clock and REFCLKB, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on that channel's TXERRB output. This output indicates an error continuously until the Phase-Align Buffer for that channel is reset. While the error remains active, the transmitter for that channel outputs a continuous "1001111000" character to indicate to the remote receiver that an error condition is present in the link.

Transmit BIST

The transmit channel contains an internal pattern generator that can be used to validate both the link and device operation. This generator is enabled by the TXBISTB latch via the device configuration interface. When enabled, a register in the transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Receiver(s).

A device reset ($\overline{\text{RESET}}$ sampled LOW) presets the BIST Enable Latches to disable BIST on all channels.

All data present at the TXDB[9:0] inputs are ignored when BIST is active on that channel.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLKB± input, and that clock is multiplied by 10 or 20 (as selected by TXRATEB) to generate a bit-rate clock for use by the transmit shifter. It also provides a character-rate clock used by the transmit paths, and outputs this character rate clock as TXCLKOB.

The clock multiplier PLL can accept a REFCLKB± input between 19.5 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYV15G0104TRB clock multiplier (TXRATEB) and by the level on the SPDSELB input.

SPDSELB is a 3-level select[4] input that selects one of three operating ranges for the serial data outputs of the transmit channel. The operating serial signaling-rate and allowable range of REFCLKB± frequencies are listed in *Table 1*.

Table 1. Operating Speed Settings

SPDSELB	TXRATEB	REFCLKB± Frequency (MHz)	Signaling Rate (Mbps)
LOW	1	reserved	195 – 400
	0	19.5 – 40	
MID (Open)	1	20 – 40	400 – 800
	0	40 – 80	
HIGH	1	40 – 75	800 – 1500
	0	80 – 150	

The REFCLKB± inputs are differential inputs with each input internally biased to 1.4V. If the REFCLKB+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point. When driven by a single-ended TTL, LVTTL, or LVCMOS clock source, connect the clock source to either the true or complement REFCLKB input, and leave the alternate REFCLKB input open (floating).

When both the REFCLKB+ and REFCLKB– inputs are connected, the clock source must be a differential clock. This can either be a differential LVPECL clock that is DC-or AC-coupled or a differential LVTTL or LVCMOS clock.

By connecting the REFCLKB– input to an external voltage source, it is possible to adjust the reference point of the REFCLKB+ input for alternate logic levels. When doing so, it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

Transmit Serial Output Drivers

The serial output interface drivers use differential Current Mode Logic (CML) drivers to provide source-matched drivers for 50Ω transmission lines. These drivers accept data from the transmit shifter. These drivers have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

Transmit Channels Enabled

Each driver can be enabled or disabled separately via the device configuration interface.

When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both transmit serial drivers are in this disabled state, the transmitter internal logic for that channel is also powered down. A device reset ($\overline{\text{RESET}}$ sampled LOW) disables all output drivers.

Note. When the disabled transmit channel (i.e., both outputs disabled) is re-enabled:

- the data on the transmit serial outputs may not meet all timing specifications for up to 250 μs
- the state of the phase-align buffer cannot be guaranteed, and a phase-align reset is required if the phase-align buffer is used

CYV15G0104TRB Receive Data Path

Serial Line Receivers

Two differential Line Receivers, INA1± and INA2±, are available on the receive channel for accepting serial data streams. The active Serial Line Receiver is selected using the INSELA input. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

Signal Detect/Link Fault

Each selected Line Receiver (i.e., that routed to the clock and data recovery PLL) is simultaneously monitored for

- analog amplitude above amplitude level selected by SDASELA
- transition density above the specified limit
- range controls report the received data stream inside normal frequency range (±1500 ppm[24])
- receive channel enabled
- Presence of reference clock
- ULCA is not asserted.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFIA (Link Fault Indicator) output associated with each receive channel, which changes synchronous to the receive interface clock.

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with highly attenuated signals, or in high-noise environments. The analog amplitude level detection is set by the SDASELA latch via device configuration interface. The SDASELA latch sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 2*. This control input affects the analog monitors for all receive channels. The Analog Signal Detect monitors are active for the Line Receiver as selected by the INSELA input.

Table 2. Analog Amplitude Detect Valid Signal Levels[7]

SDASE-LA	Typical Signal with Peak Amplitudes Above
00	Analog Signal Detector is disabled
01	140 mV p-p differential
10	280 mV p-p differential
11	420 mV p-p differential

Transition Density

The Transition Detection logic checks for the absence of transitions spanning greater than six transmission characters

(60 bits). If no transitions are present in the data received, the Detection logic for that channel asserts LFIA.

Range Controls

The CDR circuit includes logic to monitor the frequency of the PLL Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been "missing."
- when the incoming data stream is outside the acceptable signaling rate range.

To perform this function, the frequency of the RXPLL VCO is periodically compared to the frequency of the TRGCLKA± input. If the VCO is running at a frequency beyond ±1500ppm[24] as defined by the TRGCLKA± frequency, it is periodically forced to the correct frequency (as defined by TRGCLKA±, SPDSELA, and TRGRATEA) and then released in an attempt to lock to the input data stream.

The sampling and relock period of the Range Control is calculated as follows: RANGE_CONTROL_ SAMPLING_PERIOD = (RECOVERED BYTE CLOCK PERIOD) * (4096).

During the time that the Range Control forces the RXPLL VCO to track TRGCLKA±, the LFIA output is asserted LOW. After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIA should be HIGH.

The operating serial signaling-rate and allowable range of TRGCLKA± frequencies are listed in *Table 3*.

Table 3. Operating Speed Settings

SPDSELA	TRGRATEA	TRGCLKA± Frequency (MHz)	Signaling Rate (Mbps)
LOW	1	reserved	195 – 400
	0	19.5 – 40	
MID (Open)	1	20 – 40	400 – 800
	0	40 – 80	
HIGH	1	40 – 75	800 – 1500
	0	80 – 150	

Receive Channel Enabled

The receive channel can be enabled or disabled through the RXPLLPDA input latch as controlled by the device configuration interface. When RXPLLPDA = 0, the CDR PLL and analog circuitry of the channel are disabled. Any disabled channel indicates a constant link fault condition on the LFIA output. When RXPLLPDA = 1, the CDR PLL and receive channel are enabled to receive a serial stream.

Note:

7. The peak amplitudes listed in this table are for typical waveforms that have generally 3 – 4 transitions for every ten bits. In a worse case environment the signals may have a sine-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table above by approximately 100 mV.

Note. When the disabled receive channel is reenabled, the status of the LFIA output and data on the parallel outputs for the associated channel may be indeterminate for up to 2 ms.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from the received serial stream is performed by a separate CDR block within the receive channel. The clock extraction function is performed by an integrated PLL that tracks the frequency of the transitions in the incoming bit stream and aligns the phase of the internal bit-rate clock to the transitions in the selected serial data stream.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) training clock from the TRGCLKA± input. This TRGCLKA± input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency (rather than a harmonic of the bit-rate)
- reduce PLL acquisition time
- limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR attempts to recover a data stream from it. If the signaling rate of the recovered data stream is outside the limits set by the range control monitors, the CDR tracks TRGCLKA± instead of the data stream. Once the CDR output (RXCLKA±) frequency returns back close to the TRGCLKA± frequency, the CDR input is switched back to the input data stream. If no data is present at the selected line receiver, this switching behavior may result in brief RXCLKA± frequency excursions from TRGCLKA±. However, the validity of the input data stream is indicated by the LFIA output. The frequency of TRGCLKA± is required to be within ±1500ppm[24] of the frequency of the clock that drives the REFCLKB± input of the *remote* transmitter to ensure a lock to the incoming data stream. This large ppm tolerance allows the CDR PLL to reliably receive a 1.485 or 1.485/1.001 Gbps SMPTE HD-SDI data stream with a constant TRGCLK frequency.

For systems using multiple or redundant connections, the LFIA output can be used to select an alternate data stream. When an LFIA indication is detected, external logic can toggle selection of the INA1± and INA2± input through the INSELA input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream.

Reclocker

The receive channel performs a reclocker function on the incoming serial data. To do this, the Clock and Data Recovery PLL first recovers the clock from the data. The data is retimed by the recovered clock and then passed to an output register. Also, the recovered character clock from the receive PLL is passed to the reclocker output PLL which generates the bit clock that is used to clock the retimed data into the output register. This data stream is then transmitted through the differential serial outputs.

Reclocker Serial Output Drivers

The serial output interface drivers use differential Current Mode Logic (CML) drivers to provide source-matched drivers for 50Ω transmission lines. These drivers accept data from the reclocker output register in the reclocker channel. These drivers have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

Reclocker Output Channels Enabled

Each driver can be enabled or disabled separately via the device configuration interface.

When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both reclocker serial drivers are in this disabled state, the internal reclocker logic is also powered down. The deserialization logic and parallel outputs will remain enabled. A device reset (RESET sampled LOW) disables all output drivers.

Note. When the disabled reclocker function (i.e., both outputs disabled) is re-enabled, the data on the reclocker serial outputs may not meet all timing specifications for up to 250 μs.

Output Bus

The receive channel presents a 10-bit data signal (and a BIST status signal when RXBISTA[1:0] = 10).

Receive BIST Operation

The receiver channel contains an internal pattern checker that can be used to validate both device and link operation. These pattern checkers are enabled by the RXBISTA[1:0] latch via the device configuration interface. When enabled, a register in the receive channel becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the Receiver checks each character from the deserializer with each character generated by the LFSR and indicates compare errors and BIST status at the RXDA[1:0] and BISTSTA bits of the Output Register.

The BIST status bus {BISTSTA, RXDA[0], RXDA[1]} indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress.

The specific status reported by the BIST state machine is listed in *Table 6*. These same codes are reported on the receive status outputs.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to look for the start of the BIST sequence again.

A device reset (RESET sampled LOW) presets the BIST Enable Latches to disable BIST on all channels.

BIST Status State Machine

When a receive path is enabled to look for and compare the received data stream with the BIST pattern, the {BISTSTA, RXDA[1:0]} bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in *Figure 2* and *Table 6*. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine

is forced to the WAIT_FOR_BIST state where it monitors the receive path for the first character of the next BIST sequence.

Power Control

The CYV15G0104TRB supports user control of the powered up or down state of each transmit and receive channel. The receive channels are controlled by the RXPLLPDA latch via the device configuration interface. When RXPLLPDA = 0, the receive PLL and analog circuitry of the channel is disabled. The transmit channel is controlled by the TOE1B and the TOE2B latches via the device configuration interface. The reclocker function is controlled by the ROE1A and the ROE2A latches via the device configuration interface. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. When the reclocker serial drivers are disabled, the reclocker function will be disabled, but the deserialization logic and parallel outputs will remain enabled.

Device Reset State

When the CYV15G0104TRB is reset by assertion of $\overline{\text{RESET}}$, all state machines, counters, and configuration latches in the device are initialized to a reset state. See *Table 4* for the initialize values of the configuration latches.

Following a device reset, it is necessary to enable the transmit and receive channels used for normal operation. This can be done by sequencing the appropriate values on the device configuration interface.[5]

Device Configuration and Control Interface

The CYV15G0104TRB is highly configurable via the configuration interface. The configuration interface allows the transmitter and reclocker to be configured independently. *Table 4* lists the configuration latches within the device including the initialization value of the latches upon the assertion of $\overline{\text{RESET}}$. *Table 5* shows how the latches are mapped in the device. Each row in the *Table 5* maps to a 7-bit latch bank. There are 6 such write-only latch banks. When $\overline{\text{WREN}}$ = 0, the logic value in the DATA[6:0] is latched to the latch bank specified by the values in ADDR[2:0]. The second column of *Table 5* specifies the channels associated with the corresponding latch bank. For example, the first three latch banks (0,1 and 2) consist of configuration bits for the reclocker channel A.

Latch Types

There are two types of latch banks: static (S) and dynamic (D). Each channel is configured by 2 static and 1 dynamic latch banks. The S type contain those settings that normally do not change for a given application, whereas the D type controls the settings that could change during the application's lifetime. The first and second rows of each channel (address numbers 0, 1, 5, and 6) are the static control latches. The third row of latches for each channel (address numbers 2 and 7) are the dynamic control latches that are associated with enabling dynamic functions within the device. Address numbers 3 and 4 are internal test registers.

Static Latch Values

There are some latches in the table that have a static value (i.e. 1, 0, or X). The latches that have a ‘1’ or ‘0’ must be configured with their corresponding value each time that their associated latch bank is configured. The latches that have an ‘X’ are don’t cares and can be configured with any value.

Table 4. Device Configuration and Control Latch Descriptions

RXRATEA	**Receive Clock Rate Select**. The initialization value of the RXRATEA latch = 1. RXRATEA is used to select the rate of the RXCLKA± clock output. When RXRATEA = 1, the RXCLKA± clock outputs are complementary clocks that follow the recovered clock operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKA+ and RXCLKA–. When RXRATEA = 0, the RXCLKA± clock outputs are complementary clocks that follow the recovered clock operating at the character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKA+ or falling edge of RXCLKA–.
SDASEL1A[1:0]	**Primary Serial Data Input Signal Detector Amplitude Select**. The initialization value of the SDASEL1A[1:0] latch = 10. SDASEL1A[1:0] selects the trip point for the detection of a valid signal for the INA1± Primary Differential Serial Data Inputs. When SDASEL1A[1:0] = 00, the Analog Signal Detector is disabled. When SDASEL1A[1:0] = 01, the typical p-p differential voltage threshold level is 140mV. When SDASEL1A[1:0] = 10, the typical p-p differential voltage threshold level is 280mV. When SDASEL1A[1:0] = 11, the typical p-p differential voltage threshold level is 420mV.
SDASEL2A[1:0]	**Secondary Serial Data Input Signal Detector Amplitude Select**. The initialization value of the SDASEL2A[1:0] latch = 10. SDASEL2A[1:0] selects the trip point for the detection of a valid signal for the INA2± Secondary Differential Serial Data Inputs. When SDASEL2A[1:0] = 00, the Analog Signal Detector is disabled When SDASEL2A[1:0] = 01, the typical p-p differential voltage threshold level is 140mV. When SDASEL2A[1:0] = 10, the typical p-p differential voltage threshold level is 280mV. When SDASEL2A[1:0] = 11, the typical p-p differential voltage threshold level is 420mV.

Table 4. Device Configuration and Control Latch Descriptions (continued)

TRGRATEA	**Training Clock Rate Select**. The initialization value of the TRGRATEA latch = 0. TRGRATEA is used to select the clock multiplier for the training clock input to the CDR PLL. When TRGRATEA = 0, the TRGCLKA± input is not multiplied before it is passed to the CDR PLL. When TRGRATEA = 1, the TRGCLKA± input is multiplied by 2 before it is passed to the CDR PLL. TRGRATEA = 1 and SPDSELA = LOW is an invalid state and this combination is reserved.
RXPLLPDA	**Receive Channel Enable**. The initialization value of the RXPLLPDA latch = 0. RXPLLPDA selects if the receive channel is enabled or powered-down. When RXPLLPDA = 0, the receive PLL and analog circuitry are powered-down. When RXPLLPDA = 1, the receive PLL and analog circuitry are enabled.
RXBISTA[1:0]	**Receive Bist Disable / SMPTE Receive Enable**. The initialization value of the RXBISTA[1:0] latch = 11. For SMPTE data reception, RXBISTA[1:0] should not remain in this initialization state (11). RXBISTA[1:0] selects if receive BIST is disabled or enabled and sets the device for SMPTE data reception. When RXBISTA[1:0] = 01, the receiver BIST function is disabled and the device is set to receive SMPTE data. When RXBISTA[1:0] = 10, the receive BIST function is enabled and the device is set to receive BIST data. RXBISTA[1:0] = 00 and RXBISTA[1:0] = 11 are invalid states.
ROE2A	**Reclocker Secondary Differential Serial Data Output Driver Enable**. The initialization value of the ROE2A latch = 0. ROE2A selects if the ROUTA2± secondary differential output drivers are enabled or disabled. When ROE2A = 1, the associated serial data output driver is enabled allowing the reclocked data to be transmitted. When ROE2A = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the reclocker logic is also powered down. A device reset (RESET sampled LOW) disables all output drivers.
ROE1A	**Reclocker Primary Differential Serial Data Output Driver Enable**. The initialization value of the ROE1A latch = 0. ROE1A selects if the ROUTA1± primary differential output drivers are enabled or disabled. When ROE1A = 1, the associated serial data output driver is enabled allowing the reclocked data to be transmitted. When ROE1A = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the reclocker logic is also powered down. A device reset (RESET sampled LOW) disables all output drivers.
TXCKSELB	**Transmit Clock Select**. The initialization value of the TXCKSELB latch = 1. TXCKSELB selects the clock source used to write data into the Transmit Input Register. When TXCKSELB = 1, the input register TXDB[9:0] is clocked by REFCLKB↑. In this mode, the phase alignment buffer in the transmit path is bypassed. When TXCKSELB = 0, TXCLKB↑ is used to clock in the input register TXDB[9:0].
TXRATEB	**Transmit PLL Clock Rate Select**. The initialization value of the TXRATEB latch = 0. TXRATEB is used to select the clock multiplier for the Transmit PLL. When TXRATEB = 0, the transmit PLL multiples the REFCLKB± input by 10 to generate the serial bit-rate clock. When TXRATEB = 0, the TXCLKOB output clocks are full-rate clocks and follow the frequency and duty cycle of the REFCLKB± input. When TXRATEB = 1, the Transmit PLL multiplies the REFCLKB± input by 20 to generate the serial bit-rate clock. When TXRATEB = 1, the TXCLKOB output clocks are twice the frequency rate of the REFCLKB± input. When TXCKSELB = 1 and TXRATEB = 1, the Transmit Data Inputs are captured using both the rising and falling edges of REFCLKB. TXRATEB = 1 and SPDSELB = LOW, is an invalid state and this combination is reserved.
TXBISTB	**Transmit Bist Disable**. The initialization value of the TXBISTB latch = 1. TXBISTB selects if the transmit BIST is disabled or enabled. When TXBISTB = 1, the transmit BIST function is disabled. When TXBISTB = 0, the transmit BIST function is enabled.
TOE2B	**Secondary Differential Serial Data Output Driver Enable**. The initialization value of the TOE2B latch = 0. TOE2B selects if the TOUTB2± secondary differential output drivers are enabled or disabled. When TOE2B = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When TOE2B = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.
TOE1B	**Primary Differential Serial Data Output Driver Enable**. The initialization value of the TOE1B latch = 0. TOE1B selects if the TOUTB1± primary differential output drivers are enabled or disabled. When TOE1B = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When TOE1B = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.

Table 4. Device Configuration and Control Latch Descriptions (continued)

PABRSTB	**Transmit Clock Phase Alignment Buffer Reset**. The initialization value of the PABRSTB latch = 1. The PABRSTB is used to re-center the Transmit Phase Align Buffer. When the configuration latch PABRSTB is written as a 0, the phase of the TXCLKB input clock relative to REFCLKB+/- is initialized. PABRSTB is an asynchronous input, but is sampled by each TXCLKB↑ to synchronize it to the internal clock domain. PABRSTB is a self clearing latch. This eliminates the requirement of writing a 1 to complete the initialization of the Phase Alignment Buffer.

Device Configuration Strategy

The following is a series of ordered events needed to load the configuration latches on a per channel basis:

1. Pulse $\overline{\text{RESET}}$ Low after device power-up. This operation resets both channels.
2. Set the static latch banks for the target channel.
3. Set the dynamic bank of latches for the target channel. Enable the Receive PLL and/or transmit channel. If the receiver is enabled, set the device for SMPTE data reception (RXBISTA[1:0] = 01) or BIST data reception (RXBISTA[1:0] = 10).
4. Reset the Phase Alignment Buffer. [Optional if phase align buffer is bypassed.]

Table 5. Device Control Latch Configuration Table

ADDR	Channel	Type	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Reset Value
0 (000b)	A	S	1	0	X	X	0	0	RXRATEA	1011111
1 (001b)	A	S	SDASEL2A[1]	SDASEL2A[0]	SDASEL1A[1]	SDASEL1A[0]	X	X	TRGRATEA	1010110
2 (010b)	A	D	RXBISTA[1]	RXPLLPDA	RXBISTA[0]	X	ROE2A	ROE1A	X	1011001
3 (011b)			INTERNAL TEST REGISTERS							
4 (100b)			DO NOT WRITE TO THESE ADDRESSES							
5 (101b)	B	S	X	X	X	X	X	0	RXRATE D	1011111
6 (110b)	B	S	X	X	X	X	0	TXCKSELB	TXRATEB	1010110
7 (111b)	B	D	X	0	X	TXBISTB	TOE2B	TOE1B	PABRSTB	1011001

JTAG Support

The CYV15G0104TRB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, boundary scan, and bypass are supported. This capability is present only on the LVTTL inputs and outputs, the TRGCLKA± input, and the REFCLKB± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

3-Level Select Inputs

Each 3-Level select inputs reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11 respectively

JTAG ID

The JTAG device ID for the CYV15G0104TRB is '0C811069'x.

Table 6. Receive BIST Status Bits

{BISTSTA, RXDA[0], RXDA[1]}	Description Receive BIST Status (Receive BIST = Enabled)
000, 001	**BIST Data Compare**. Character compared correctly.
010	**BIST Last Good**. Last Character of BIST sequence detected and valid.
011	Reserved.
100	**BIST Last Bad**. Last Character of BIST sequence detected invalid.
101	**BIST Start**. Receive BIST is enabled on this channel, but character compares have not yet commenced. This also indicates a PLL Out of Lock condition.
110	**BIST Error**. While comparing characters, a mismatch was found in one or more of the character bits.
111	**BIST Wait**. The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

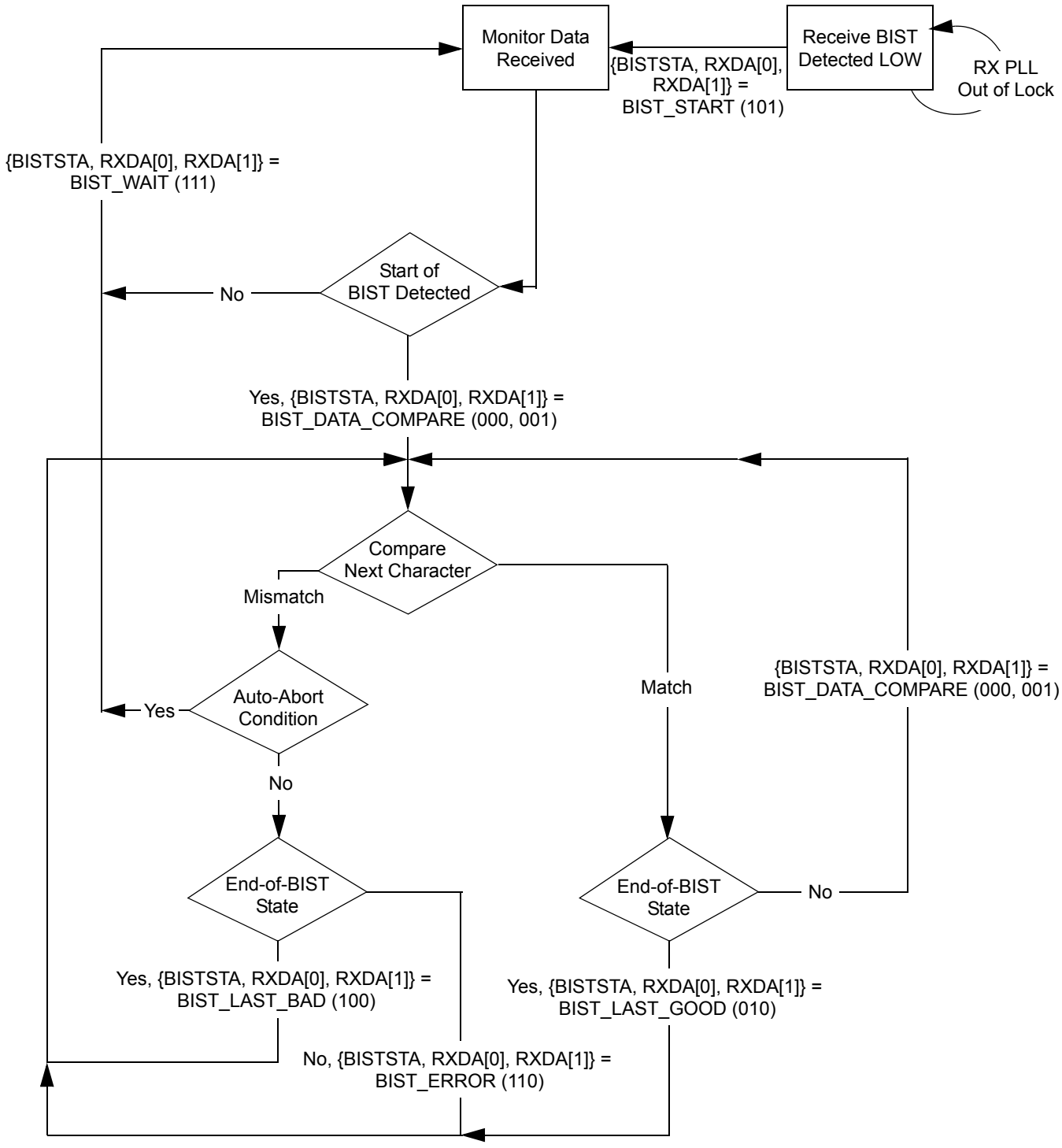


Figure 2. Receive BIST State Machine

Maximum Ratings

(Above which the useful life may be impaired. User guidelines only, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State .....–0.5V to V_{CC} + 0.5V

Output Current into LVTTL Outputs (LOW).....60 mA

DC Input Voltage.....–0.5V to V_{CC} + 0.5V

Static Discharge Voltage.....> 2000 V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Power-up Requirements

The CYV15G0104TRB requires one power-supply. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%

CYV15G0104TRB DC Electrical Characteristics

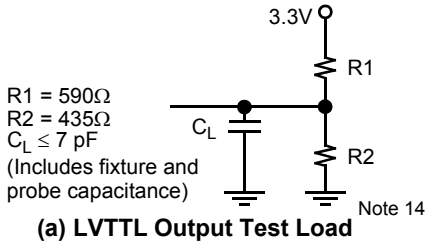
Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL-compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = – 4 mA, V_{CC} = Min.	2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.		0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[8], V_{CC} = 3.3V	–20	–100	mA
I_{OZL}	High-Z Output Leakage Current	V_{OUT} = 0V, V_{CC}	–20	20	µA
LVTTL-compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLKB Input, V_{IN} = V_{CC}		1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	REFCLKB Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLKB±					
V_{DIFF}[9]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	V_{CC}/2	V
V_{COMREF}[10]	Common Mode Range		1.0	V_{CC} – 1.2V	V
3-Level Inputs					
V_{IHH}	Three-Level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-Level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW current	V_{IN} = GND		–200	µA
Differential CML Serial Outputs: OUTA1±, OUTA2±, OUTB1±, OUTB2±, OUTC1±, OUTC2±, OUTD1±, OUTD2±					
V_{OHC}	Output HIGH Voltage (V_{cc} Referenced)	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V

8. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
9. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
10. The common mode range defines the allowable range of REFCLKB+ and REFCLKB– when REFCLKB+ = REFCLKB–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

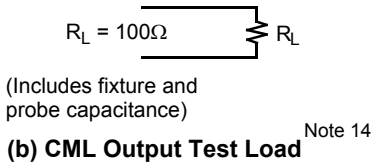
CYV15G0104TRB DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OLC}	Output LOW Voltage (V_{CC} Referenced)	100Ω differential load		V_{CC} – 1.4	V_{CC} – 0.7	V
		150Ω differential load		V_{CC} – 1.4	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load		450	900	mV
		150Ω differential load		560	1000	mV
Differential Serial Line Receiver Inputs: INA1±, INA2±						
V_{DIFFs}[9]	Input Differential Voltage |(IN+) – (IN–)|			100	1200	mV
V_{IHE}	Highest Input HIGH Voltage				V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage			V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}$ Max.			1350	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}$ Min.		–700		µA
VI_{COM}[11]	Common Mode input range	((V_{CC} – 2.0V)+0.5)min, (V_{CC} – 0.5V) max.		+1.25	+3.1	V
Power Supply				**Typ.**	**Max.**	
I_{CC}[12,13]	Max Power Supply Current	REFCLKB = MAX	Commercial	585	690	mA
I_{CC}[12,13]	Typical Power Supply Current	REFCLKB = 125 MHz	Commercial	560	660	mA

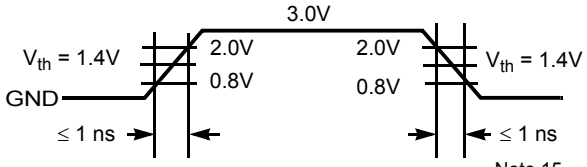
AC Test Loads and Waveforms



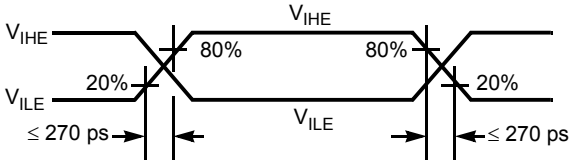
(a) LVTTL Output Test Load



(b) CML Output Test Load



(c) LVTTL Input Test Waveform



(d) CML/LVPECL Input Test Waveform

CYV15G0104TRB AC Electrical Characteristics

Parameter	Description	Min.	Max	Unit
CYV15G0104TRB Transmitter LVTTL Switching Characteristics Over the Operating Range				
f_{TS}	TXCLKB Clock Cycle Frequency	19.5	150	MHz
t_{TXCLK}	TXCLKB Period=1/f_{TS}	6.66	51.28	ns
t_{TXCLKH}[16]	TXCLKB HIGH Time	2.2		ns
t_{TXCLKL}[16]	TXCLKB LOW Time	2.2		ns

Notes:

11. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
12. Maximum I_{CC} is measured with V_{CC} = MAX,T_A = 25°C, with all channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern, and outputs unloaded.
13. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, T_A = 25°C,with all channels enabled and one Serial Line Driver per channel sending a continuous alternating 01 pattern. The redundant outputs on each channel are powered down and the parallel outputs are unloaded.
14. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
15. The LVTTL switching threshold is 1.4V. All timing references are made relative to where the signal edges cross the threshold voltage.
16. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.

CYV15G0104TRB AC Electrical Characteristics (continued)

Parameter	Description	Min.	Max	Unit
t_{TXCLKR} [16, 17, 18, 19]	TXCLKB Rise Time	0.2	1.7	ns
t_{TXCLKF} [16, 17, 18, 19]	TXCLKB Fall Time	0.2	1.7	ns
t_{TXDS}	Transmit Data Set-up Time to TXCLKB↑ (TXCKSELB = 0)	2.2		ns
t_{TXDH}	Transmit Data Hold Time from TXCLKB↑ (TXCKSELB = 0)	0.8		ns
f_{TOS}	TXCLKOB Clock Frequency = 1x or 2x REFCLKB Frequency	19.5	150	MHz
t_{TXCLKO}	TXCLKOB Period=1/f_{TOS}	6.66	51.28	ns
$t_{TXCLKOD}$	TXCLKOB Duty Cycle centered at 60% HIGH time	-1.9	0	ns
CYV15G0104TRB Receiver LVTTL Switching Characteristics Over the Operating Range				
f_{RS}	RXCLKA± Clock Output Frequency	9.75	150	MHz
t_{RXCLKP}	RXCLKA± Period = 1/f_{RS}	6.66	102.56	ns
t_{RXCLKD}	RXCLKA± Duty Cycle Centered at 50% (Full Rate and Half Rate)	–1.0	+1.0	ns
t_{RXCLKR} [16]	RXCLKA± Rise Time	0.3	1.2	ns
t_{RXCLKF} [16]	RXCLKA± Fall Time	0.3	1.2	ns
t_{RXDv-} [20]	Status and Data Valid Time to RXCLKA± (RXRATEA = 0) (Full Rate)	5UI–1.8 [21]		ns
	Status and Data Valid Time to RXCLKA± (RXRATEA = 1) (Half Rate)	5UI–1.3 [21]		ns
t_{RXDv+} [20]	Status and Data Valid Time to RXCLKA± (RXRATEA = 0)	5UI–1.7 [21]		ns
	Status and Data Valid Time to RXCLKA± (RXRATEA = 1)	5UI–2.1 [21]		ns
f_{ROS}	RECLKOA Clock Frequency	19.5	150	MHz
t_{RECLKO}	RECLKOA Period=1/f_{ROS}	6.66	51.28	ns
$t_{RECLKOD}$	RECLKOA Duty Cycle centered at 60% HIGH time	-1.9	0	ns
CYV15G0104TRB REFCLKB Switching Characteristics Over the Operating Range				
f_{REF}	REFCLKB Clock Frequency	19.5	150	MHz
t_{REFCLK}	REFCLKB Period = 1/f_{REF}	6.6	51.28	ns
t_{REFH}	REFCLKB HIGH Time (TXRATEB = 1)(Half Rate)	5.9		ns
	REFCLKB HIGH Time (TXRATEB = 0)(Full Rate)	2.9 [16]		ns
t_{REFL}	REFCLKB LOW Time (TXRATEB = 1)(Half Rate)	5.9		ns
	REFCLKB LOW Time (TXRATEB = 0)(Full Rate)	2.9 [16]		ns
t_{REFD} [22]	REFCLKB Duty Cycle	30	70	%
t_{REFR} [16, 17, 18, 19]	REFCLKB Rise Time (20%–80%)		2	ns
t_{REFF} [16, 17, 18, 19]	REFCLKB Fall Time (20%–80%)		2	ns
t_{TREFDS}	Transmit Data Set-up Time to REFCLKB - Full Rate (TXRATEB = 0, TXCKSELB = 1)	2.2		ns
	Transmit Data Set-up Time to REFCLKB - Half Rate (TXRATEB = 1, TXCKSELB = 1)	1.9		ns
t_{TREFDH}	Transmit Data Hold Time from REFCLKB - Full Rate (TXRATEB= 0, TXCKSELB = 1)	0.8		ns
	Transmit Data Hold Time from REFCLKB - Half Rate (TXRATEB = 1, TXCKSELB = 1)	1.5		ns

Notes:
17. The ratio of rise time to falling time must not vary by greater than 2:1.
18. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
19. All transmit AC timing parameters measured with 1ns typical rise time and fall time.
20. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.
21. Receiver UI (Unit Interval) is calculated as 1/(f_{TRG} * 20) (when TRGRATEA = 1) or 1/(f_{TRG} * 10) (when TRGRATEA = 0). In an operating link this is equivalent to t_B.
22. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLKB± duty cycle cannot be as large as 30%–70%.

CYV15G0104TRB AC Electrical Characteristics (continued)

Parameter	Description	Min.	Max	Unit
CYV15G0104TRB TRGCLKA Switching Characteristics Over the Operating Range				
f_{TRG}	TRGCLKA Clock Frequency	19.5	150	MHz
t_{REFCLK}	TRGCLKA Period = $1/f_{TRG}$	6.6	51.28	ns
t_{TRGH}	TRGCLKA HIGH Time (TRGRATEA = 1)(Half Rate)	5.9		ns
	TRGCLKA HIGH Time (TRGRATEA = 0)(Full Rate)	2.9[16]		ns
t_{TRGL}	TRGCLKA LOW Time (TRGRATEA = 1)(Half Rate)	5.9		ns
	TRGCLKA LOW Time (TRGRATEA = 0)(Full Rate)	2.9[16]		ns
t_{TRGD}[23]	TRGCLKA Duty Cycle	30	70	%
t_{TRGR}[16, 17, 18]	TRGCLKA Rise Time (20%–80%)		2	ns
t_{TRGF}[16, 17, 18]	TRGCLKA Fall Time (20%–80%)		2	ns
t_{TRGRX}[24]	TRGCLKA Frequency Referenced to Received Clock Frequency	–0.15	+0.15	%
CYV15G0104TRB Bus Configuration Write Timing Characteristics Over the Operating Range				
t_{DATAH}	Bus Configuration Data Hold	0		ns
t_{DATAS}	Bus Configuration Data Setup	10		ns
t_{WRENP}	Bus Configuration WREN Pulse Width	10		ns
CYV15G0104TRB JTAG Test Clock Characteristics Over the Operating Range				
f_{TCLK}	JTAG Test Clock Frequency		20	MHz
t_{TCLK}	JTAG Test Clock Period	50		ns
CYV15G0104TRB Device RESET Characteristics Over the Operating Range				
t_{RST}	Device RESET Pulse Width	30		ns

CYV15G0104TRB Transmitter and Reclocker Serial Output Characteristics Over the Operating Range

Parameter	Description	Condition	Min.	Max.	Unit
t_B	Bit Time		660	5128	ps
t_{RISE}[16]	CML Output Rise Time 20–80% (CML Test Load)	SPDSELx = HIGH	50	270	ps
		SPDSELx= MID	100	500	ps
		SPDSELx =LOW	180	1000	ps
t_{FALL}[16]	CML Output Fall Time 80–20% (CML Test Load)	SPDSELx = HIGH	50	270	ps
		SPDSELx = MID	100	500	ps
		SPDSELx =LOW	180	1000	ps

PLL Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
CYV15G0104TRB Transmitter Output PLL Characteristics						
$t_{JTGENSD}$[16, 25]	Transmit Jitter Generation - SD Data Rate	REFCLKB = 27 MHz		200		ps
$t_{JTGENHD}$[16, 25]	Transmit Jitter Generation - HD Data Rate	REFCLKB = 148.5 MHz		76		ps
t_{TXLOCK}	Transmit PLL lock to REFCLKB±				200	µs

Notes:

23. The duty cycle specification is a simultaneous condition with the t_{TRGH} and t_{TRGL} parameters. This means that at faster character rates the TRGCLKA± duty cycle cannot be as large as 30%–70%.
24. TRGCLKA± has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. TRGCLKA± must be within ±1500 PPM (±0.15%) of the transmitter PLL reference (REFCLK±) frequency. Although transmitting to a HOTLink II receiver channel necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard.
25. While sending BIST data at the corresponding data rate, after 10,000 histogram hits, time referenced to REFCLKB± input.
26. Receiver input stream is BIST data from the transmit channel. This data is reclocked and output to a wide-bandwidth digital sampling oscilloscope. The measurement was recorded after 10,000 histogram hits, time referenced to REFCLKB± of the transmit channel.

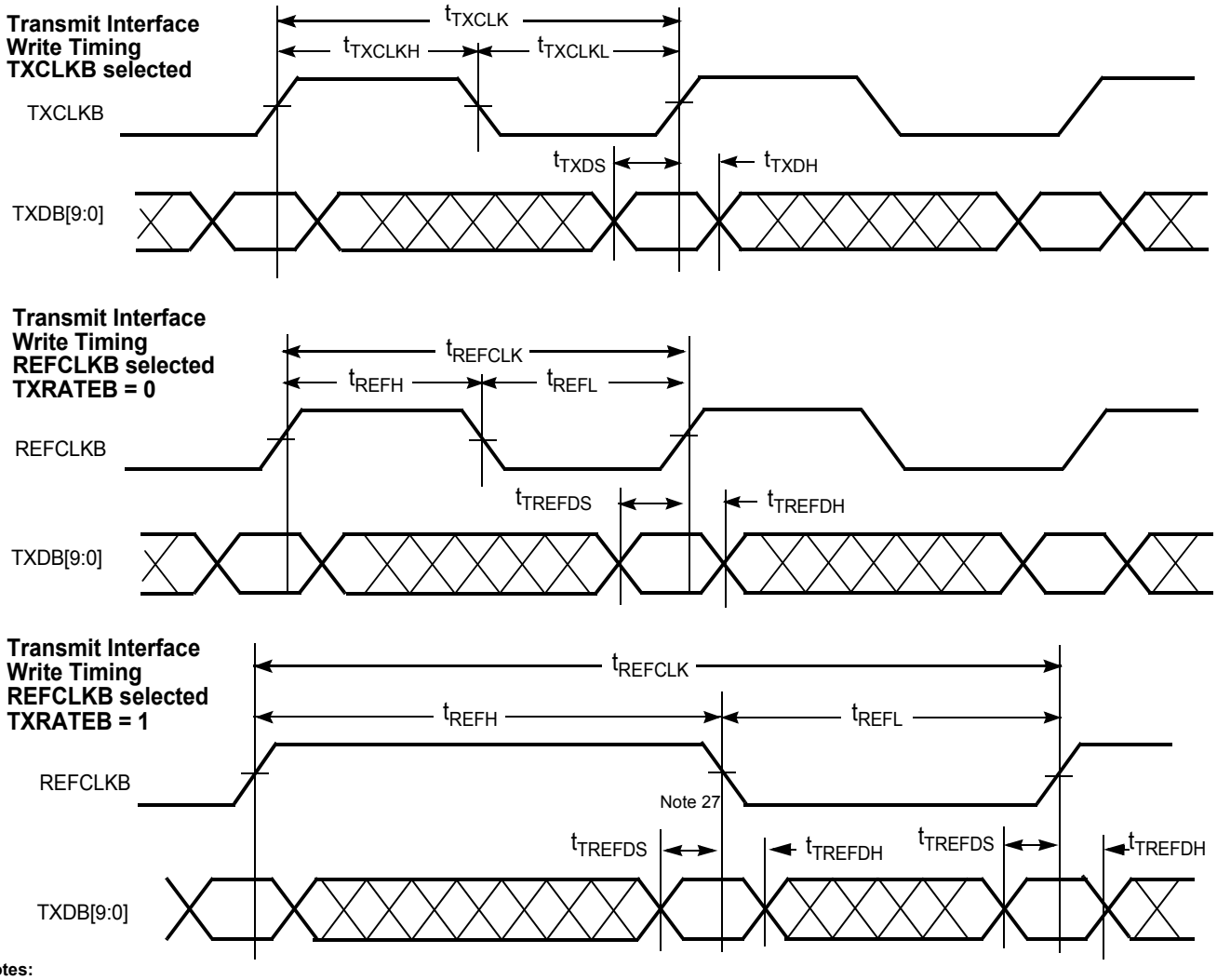
PLL Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
CYV15G0104TRB Reclocker Output PLL Characteristics						
$t_{JRGENSD}$ [16, 26]	Reclocker Jitter Generation - SD Data Rate	TRGCLKA = 27 MHz		133		ps
$t_{JRGENHD}$ [16, 26]	Reclocker Jitter Generation - HD Data Rate	TRGCLKA = 148.5 MHz		107		ps
CYV15G0104TRB Receive PLL Characteristics Over the Operating Range						
t_{RXLOCK}	Receive PLL lock to input data stream (cold start)				376k	UI
	Receive PLL lock to input data stream				376k	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate				46	UI

Capacitance [16]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	4	pF

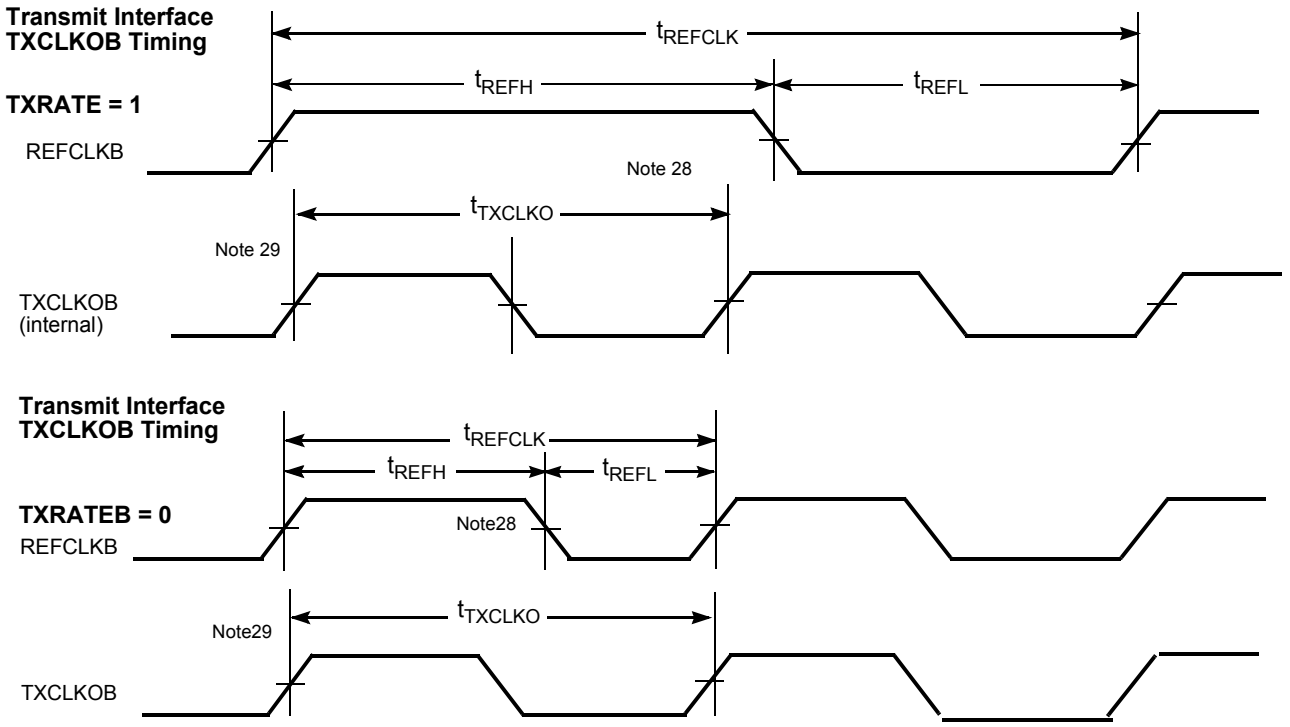
CYV15G0104TRB HOTLink II Transmitter Switching Waveforms



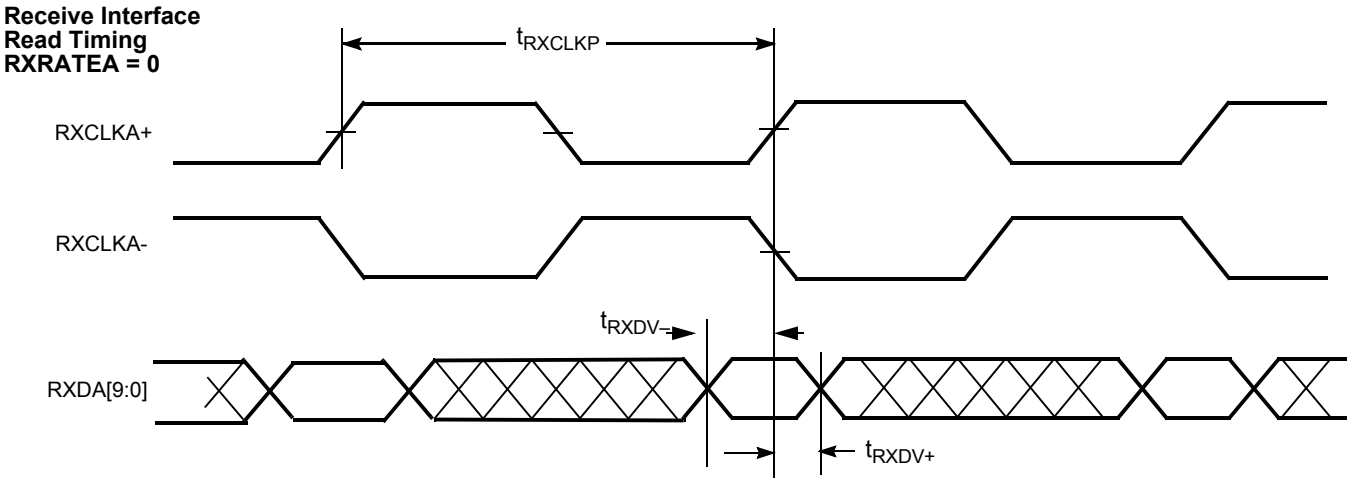
Notes:

27. When REFCLKB± is configured for half-rate operation (TXRATEB = 1) and data is captured using REFCLKB instead of a TXCLKB clock. Data is captured using both the rising and falling edges of REFCLKB.

CYV15G0104TRB HOTLink II Transmitter Switching Waveforms (continued)



Switching Waveforms for the CYV15G0104TRB HOTLink II Receiver

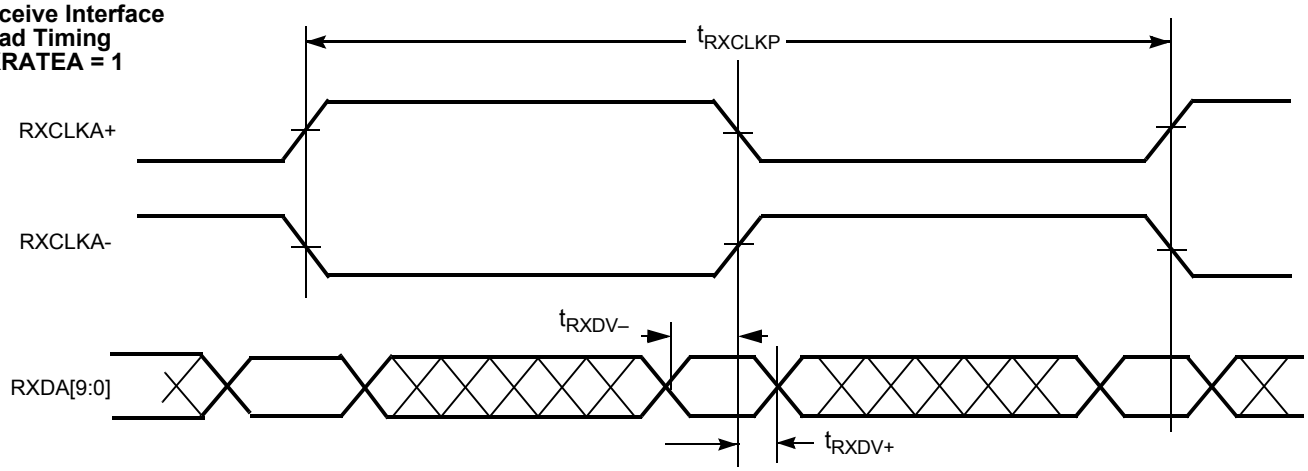


Notes:

28. The TXCLKOB output remains at the character rate regardless of the state of TXRATEB and does not follow the duty cycle of REFCLKB±.
29. The rising edge of TXCLKOB output has no direct phase relationship to the REFCLKB± input.

Switching Waveforms for the CYV15G0104TRB HOTLink II Receiver

Receive Interface Read Timing RXRATEA = 1



Bus Configuration Write Timing

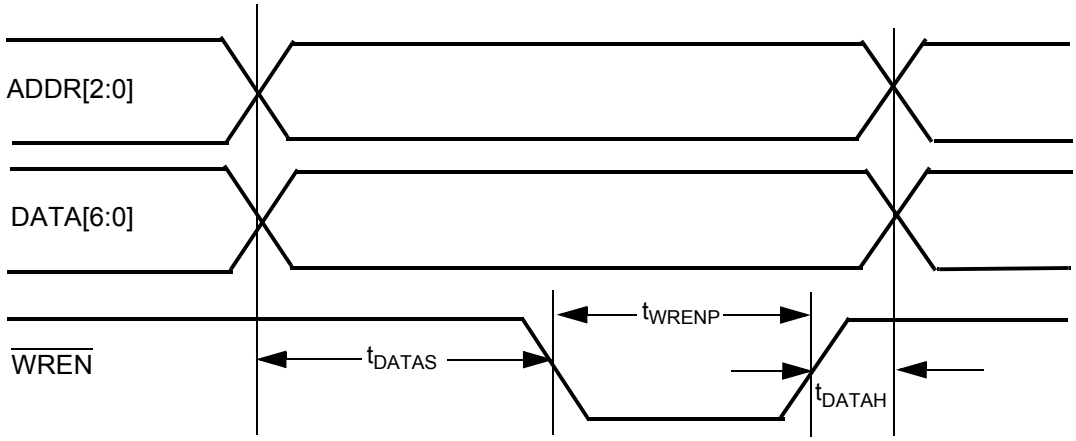


Table 7. Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A01	NC	NO CONNECT	C07	NC	NO CONNECT	F17	VCC	POWER
A02	NC	NO CONNECT	C08	GND	GROUND	F18	NC	NO CONNECT
A03	NC	NO CONNECT	C09	DATA[6]	LVTTL IN PU	F19	NC	NO CONNECT
A04	NC	NO CONNECT	C10	DATA[4]	LVTTL IN PU	F20	NC	NO CONNECT
A05	VCC	POWER	C11	DATA[2]	LVTTL IN PU	G01	GND	GROUND
A06	NC	NO CONNECT	C12	DATA[0]	LVTTL IN PU	G02	$\overline{\text{WREN}}$	LVTTL IN PU
A07	TOUTB1–	CML OUT	C13	GND	GROUND	G03	GND	GROUND
A08	GND	GROUND	C14	NC	NO CONNECT	G04	GND	GROUND
A09	GND	GROUND	C15	SPDSELB	3-LEVEL SEL	G17	NC	NO CONNECT
A10	TOUTB2–	CML OUT	C16	VCC	POWER	G18	NC	NO CONNECT
A11	INA1–	CML IN	C17	LDTDEN	LVTTL IN PU	G19	SPDSELA	3-LEVEL SEL
A12	ROUTA1–	CML OUT	C18	$\overline{\text{TRST}}$	LVTTL IN PU	G20	NC	NO CONNECT
A13	GND	GROUND	C19	GND	GROUND	H01	GND	GROUND
A14	INA2–	CML IN	C20	TDO	LVTTL 3-S OUT	H02	GND	GROUND
A15	ROUTA2–	CML OUT	D01	TCLK	LVTTL IN PD	H03	GND	GROUND
A16	VCC	POWER	D02	$\overline{\text{RESET}}$	LVTTL IN PU	H04	GND	GROUND
A17	VCC	POWER	D03	VCC	POWER	H17	GND	GROUND
A18	NC	NO CONNECT	D04	INSELA	LVTTL IN	H18	GND	GROUND
A19	VCC	POWER	D05	VCC	POWER	H19	GND	GROUND
A20	NC	NO CONNECT	D06	$\overline{\text{ULCA}}$	LVTTL IN PU	H20	GND	GROUND
B01	VCC	POWER	D07	NC	NO CONNECT	J01	GND	GROUND
B02	NC	NO CONNECT	D08	GND	GROUND	J02	GND	GROUND
B03	VCC	POWER	D09	DATA[5]	LVTTL IN PU	J03	GND	GROUND
B04	NC	NO CONNECT	D10	DATA[3]	LVTTL IN PU	J04	GND	GROUND
B05	VCC	POWER	D11	DATA[1]	LVTTL IN PU	J17	NC	NO CONNECT
B06	VCC	POWER	D12	GND	GROUND	J18	NC	NO CONNECT
B07	TOUTB1+	CML OUT	D13	GND	GROUND	J19	NC	NO CONNECT
B08	GND	GROUND	D14	GND	GROUND	J20	NC	NO CONNECT
B09	NC	NO CONNECT	D15	NC	NO CONNECT	K01	NC	NO CONNECT
B10	TOUTB2+	CML OUT	D16	VCC	POWER	K02	NC	NO CONNECT
B11	INA1+	CML IN	D17	NC	NO CONNECT	K03	GND	GROUND
B12	ROUTA1+	CML OUT	D18	VCC	POWER	K04	GND	GROUND
B13	GND	GROUND	D19	SCANEN2	LVTTL IN PD	K17	NC	NO CONNECT
B14	INA2+	CML IN	D20	TMEN3	LVTTL IN PD	K18	NC	NO CONNECT
B15	ROUTA2+	CML OUT	E01	VCC	POWER	K19	NC	NO CONNECT
B16	VCC	POWER	E02	VCC	POWER	K20	NC	NO CONNECT
B17	NC	NO CONNECT	E03	VCC	POWER	L01	NC	NO CONNECT
B18	NC	NO CONNECT	E04	VCC	POWER	L02	NC	NO CONNECT
B19	NC	NO CONNECT	E17	VCC	POWER	L03	NC	NO CONNECT
B20	NC	NO CONNECT	E18	VCC	POWER	L04	GND	GROUND
C01	TDI	LVTTL IN PU	E19	VCC	POWER	L17	NC	NO CONNECT
C02	TMS	LVTTL IN PU	E20	VCC	POWER	L18	NC	NO CONNECT
C03	VCC	POWER	F01	NC	NO CONNECT	L19	NC	NO CONNECT

Table 7. Package Coordinate Signal Allocation (continued)

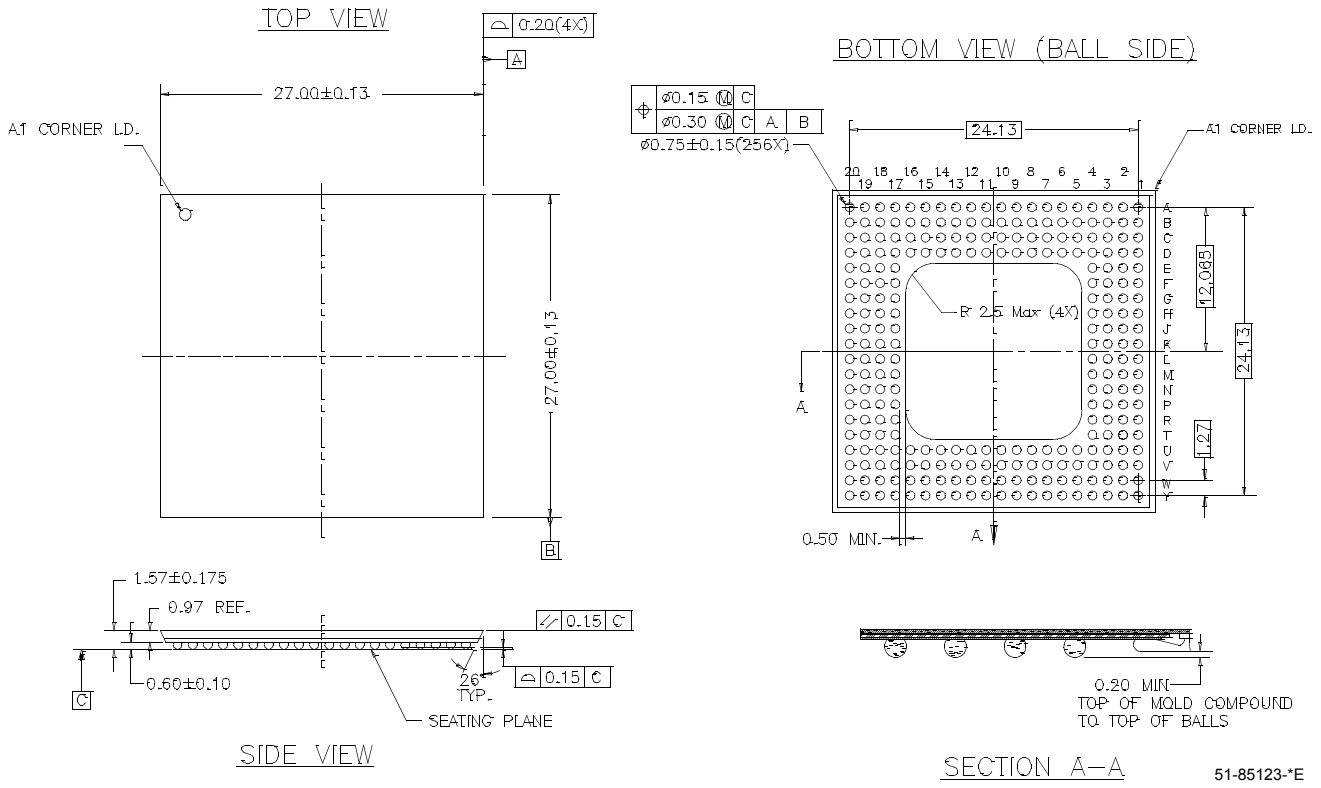
Ball ID	Signal Name	Signal Type
C04	VCC	POWER
C05	VCC	POWER
C06	NC	NO CONNECT
M03	NC	NO CONNECT
M04	NC	NO CONNECT
M17	NC	NO CONNECT
M18	NC	NO CONNECT
M19	NC	NO CONNECT
M20	GND	GROUND
N01	GND	GROUND
N02	GND	GROUND
N03	GND	GROUND
N04	GND	GROUND
N17	GND	GROUND
N18	GND	GROUND
N19	GND	GROUND
N20	GND	GROUND
P01	NC	NO CONNECT
P02	NC	NO CONNECT
P03	NC	NO CONNECT
P04	NC	NO CONNECT
P17	GND	GROUND
P18	GND	GROUND
P19	GND	GROUND
P20	GND	GROUND
R01	NC	NO CONNECT
R02	NC	NO CONNECT
R03	NC	NO CONNECT
R04	NC	NO CONNECT
R17	VCC	POWER
R18	VCC	POWER
R19	VCC	POWER
R20	VCC	POWER
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	TXDB[0]	LVTTL IN
U02	TXDB[1]	LVTTL IN
F02	NC	NO CONNECT
F03	VCC	POWER
F04	NC	NO CONNECT
U03	TXDB[2]	LVTTL IN
U04	TXDB[9]	LVTTL IN
U05	VCC	POWER
U06	NC	NO CONNECT
U07	NC	NO CONNECT
U08	GND	GROUND
U09	GND	GROUND
U10	ADDR [0]	LVTTL IN PU
U11	REFCLKB–	PECL IN
U12	GND	GROUND
U13	GND	GROUND
U14	GND	GROUND
U15	VCC	POWER
U16	VCC	POWER
U17	RXDA[4]	LVTTL OUT
U18	VCC	POWER
U19	BISTSTA	LVTTL OUT
U20	RXDA[0]	LVTTL OUT
V01	TXDB[3]	LVTTL IN
V02	TXDB[4]	LVTTL IN
V03	TXDB[8]	LVTTL IN
V04	NC	NO CONNECT
V05	VCC	POWER
V06	NC	NO CONNECT
V07	NC	NO CONNECT
V08	GND	GROUND
V09	NC	NO CONNECT
V10	GND	GROUND
V11	REFCLKB+	PECL IN
V12	RECLKOA	LVTTL OUT
V13	GND	GROUND
V14	GND	GROUND
V15	VCC	POWER
V16	VCC	POWER
V17	RXDA[9]	LVTTL OUT
V18	RXDA[5]	LVTTL OUT
V19	RXDA[2]	LVTTL OUT
V20	RXDA[1]	LVTTL OUT
W01	TXDB[5]	LVTTL IN
W02	TXDB[7]	LVTTL IN
L20	GND	GROUND
M01	NC	NO CONNECT
M02	NC	NO CONNECT
W03	NC	NO CONNECT
W04	NC	NO CONNECT
W05	VCC	POWER
W06	NC	NO CONNECT
W07	NC	NO CONNECT
W08	GND	GROUND
W09	ADDR [2]	LVTTL IN PU
W10	ADDR [1]	LVTTL IN PU
W11	RXCLKA+	LVTTL OUT
W12	REPDOA	LVTTL OUT
W13	GND	GROUND
W14	GND	GROUND
W15	VCC	POWER
W16	VCC	POWER
W17	$\overline{\text{LFIA}}$	LVTTL OUT
W18	TRGCLKA+	PECL IN
W19	RXDA[6]	LVTTL OUT
W20	RXDA[3]	LVTTL OUT
Y01	TXDB[6]	LVTTL IN
Y02	TXCLKB	LVTTL IN PD
Y03	NC	NO CONNECT
Y04	NC	NO CONNECT
Y05	VCC	POWER
Y06	NC	NO CONNECT
Y07	NC	NO CONNECT
Y08	GND	GROUND
Y09	TXCLKOB	LVTTL OUT
Y10	NC	NO CONNECT
Y11	GND	GROUND
Y12	RXCLKA–	LVTTL OUT
Y13	GND	GROUND
Y14	GND	GROUND
Y15	VCC	POWER
Y16	VCC	POWER
Y17	TXERRB	LVTTL OUT
Y18	TRGCLKA–	PECL IN
Y19	RXDA[8]	LVTTL OUT
Y20	RXDA[7]	LVTTL OUT

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYV15G0104TRB-BGC	BL256	256-Ball Thermally Enhanced Ball Grid Array	Commercial

Package Diagram

256-Lead L2 Ball Grid Array (27 x 27 x 1.57 mm) BL256



Document History Page

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REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**			FRE	New Data Sheet