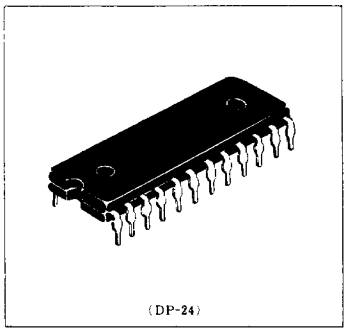
2048-word×8-bit High Speed Static CMOS RAM

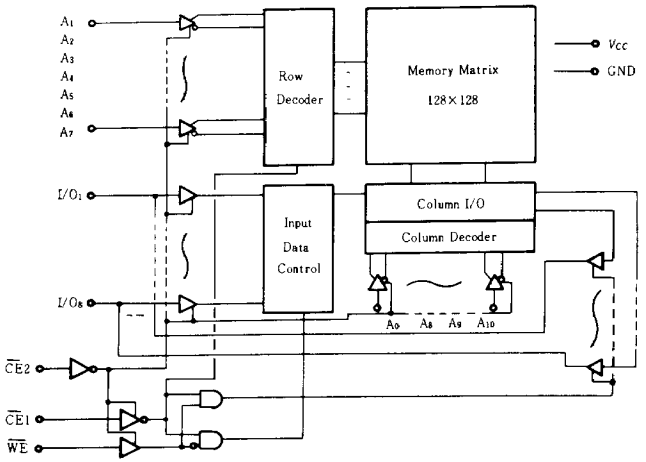
■FEATURES

- Single 5V Supply and High Density 24 Pin Package.
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

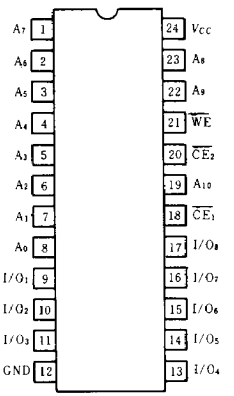


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse width 50ns : −1.0V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to+70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−1.0*	—	0.8	V

* Pulse Width : 50ns, DC : $V_{IL_{min}}$ = −0.3V.

■DC AND OPERATING CHARACTERISTICS (Ta=0°C to +70°C, V_{CC} = 5V±10%, GND = 0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN} = GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1} = V_{IH}$ or $\overline{CE_2} = V_{IH}$ $V_{I/O}$ = GND to V_{CC}	—	—	2	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE_1} = \overline{CE_2} = V_{IL}$, $I_{I/O}$ = 0mA	—	35	70	mA
Average Operating Current	I_{CC1}	Min cycle, duty = 100% $\overline{CE_1} = V_{IL}$, $\overline{CE_2} = V_{IL}$	—	35	70	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE_1} \geqq V_{CC}-0.2V$ $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	—	2	50	μA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE_2} \geqq V_{CC}-0.2V$	—	2	50	μA
Output low Voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC} = 5.0V, Ta = + 25°C
2) * : $V_{IL_{min}}$ = −0.3V

■CAPACITANCE (Ta=25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	5	7	pF

Note : 1) This parameter is sampled and not 100% tested.

■AC. CHARACTERISTICS (Ta=0°C to +70°C, V_{CC} = 5V±10% unless otherwise noted)

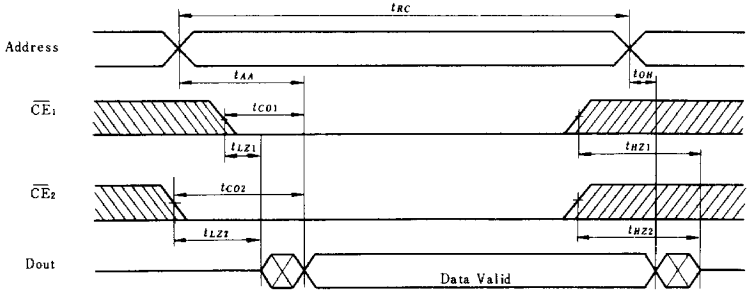
●AC TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels ... 1.5V
Output Load ..... 1 TTL Gate and C_L = 100pF (Including Scope & Jig)

●READ CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1, 2)

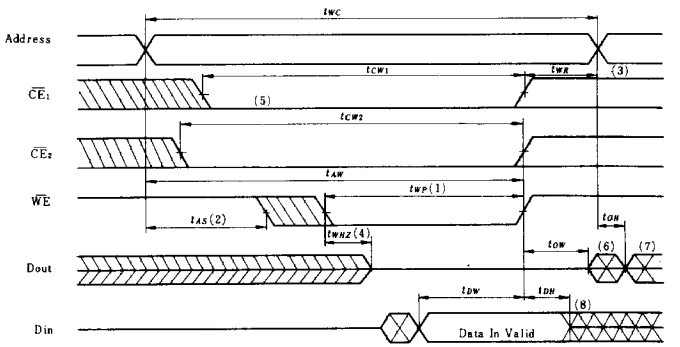


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. When $\overline{CE}_1$ and $\overline{CE}_2$ are low, the address input must not be in the high impedance state.

● WRITE CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE



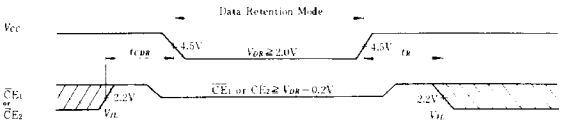
NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end/of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CE_1} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
V_{CC} for Data Retention	V_{DR2}	$\overline{CE_2} \geq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	$V_{CC}=3.0V$, $\overline{CE_1} \geq 2.8V$, $V_{IN} \geq 2.8V$ or $V_{IN} \leq 0.2V$	—	—	30*	μA
Data Retention Current	I_{CCDR2}	$V_{CC}=3.0V$, $\overline{CE_2} \geq V_{CC}-0.2V$	—	—	30*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

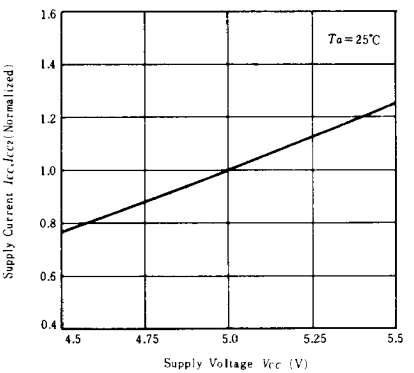
* 10μA max at Ta=0°C to +40°C, V_{IL} min=−0.3V
** t_{RC}=Read Cycle Time

●LOW V_{CC} DATA RETENTION WAVEFORM

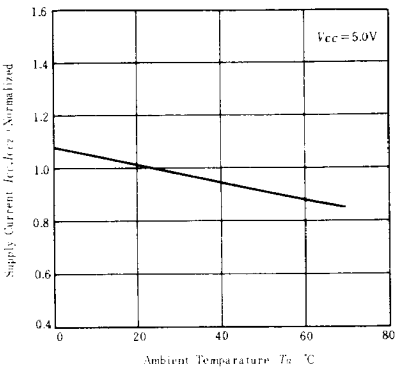


NOTE: 1. $\overline{CE_2}$ controls Address buffer, $\overline{WE}$ buffer, $\overline{CE_1}$ buffer and D_{IN} buffer. If $\overline{CE_2}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_1}$, $D_{I/O}$) can be in the high impedance state. If $\overline{CE_1}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{DE_2}$, $D_{I/O}$) must be $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$.

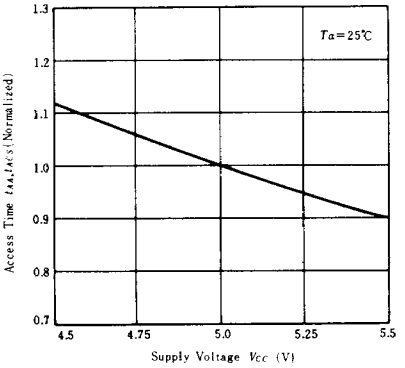
SUPPLY CURRENT vs. SUPPLY VOLTAGE



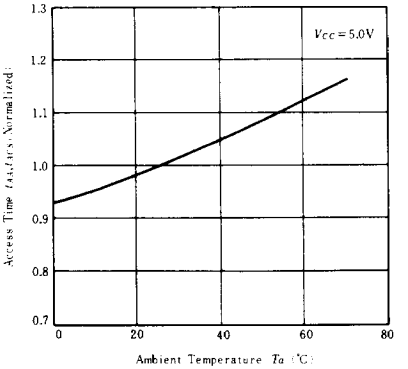
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



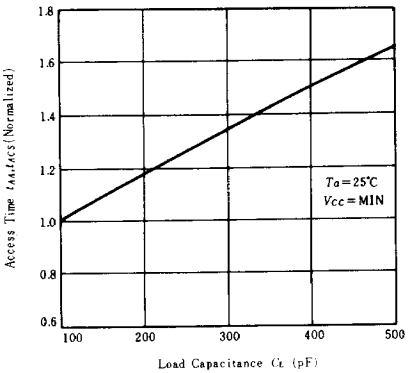
ACCESS TIME vs. SUPPLY VOLTAGE



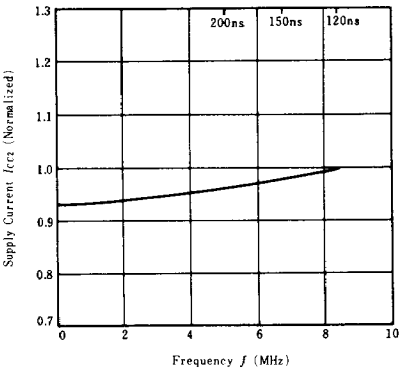
ACCESS TIME vs. AMBIENT TEMPERATURE



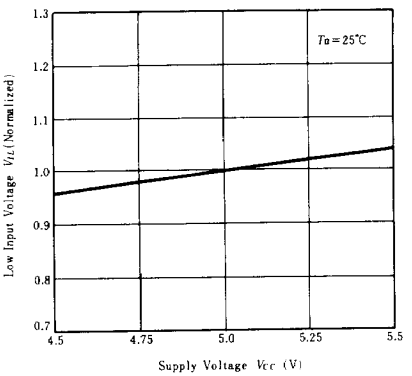
ACCESS TIME vs. LOAD CAPACITANCE



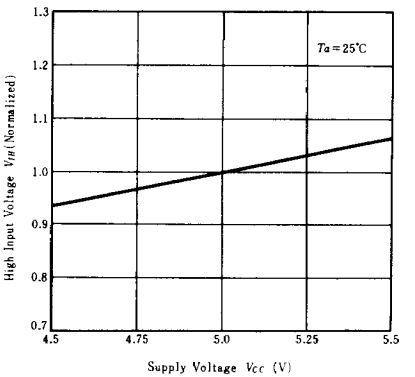
SUPPLY CURRENT vs. FREQUENCY



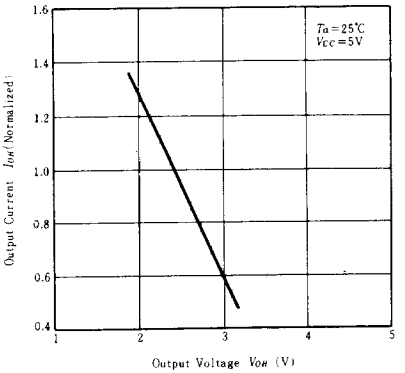
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



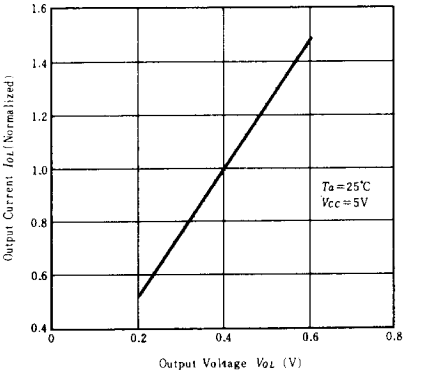
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



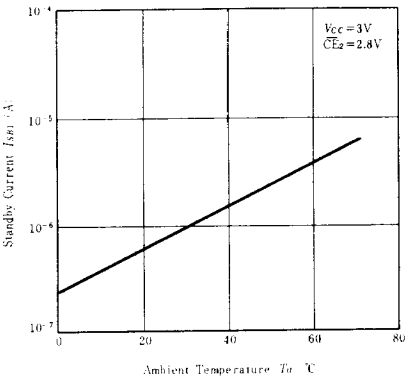
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



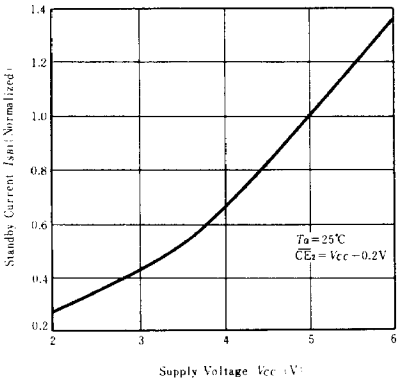
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



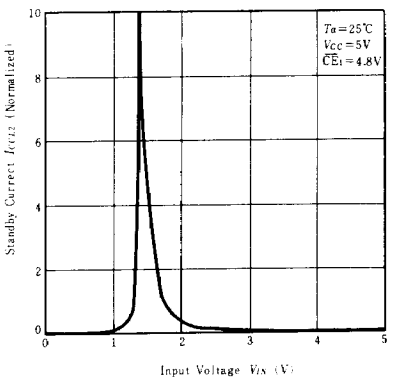
STAND-BY CURRENT vs. AMBIENT TEMPERATURE



STAND-BY CURRENT vs. SUPPLY VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE