MCP79400/MCP79401/MCP79402

I²C™ Real-Time Clock/Calendar with SRAM, Unique ID and Battery Switchover

Device Selection Table

Part Number	SRAM (Bytes)	Unique ID
MCP79400	64	Blank
MCP79401	64	EUI-48™
MCP79402	64	EUI-64™

Features:

- Real-Time Clock/Calendar (RTCC), Battery Backed:
  - Hours, Minutes, Seconds, Day of Week, Day, Month and Year
  - Dual alarm with single output
- On-Chip Digital Trimming/Calibration:
  - Range -127 to +127 ppm
  - Resolution 1 ppm
- Programmable Open-Drain Output Control:
  - CLKOUT with 4 selectable frequencies
  - Alarm output
- 64 Bytes SRAM, Battery Backed
- 64-Bit Unique ID:
  - User or factory programmable
  - Protected EEPROM
  - EUI-48™ or EUI-64™ MAC address
  - Custom ID programming
- Automatic V_{CC} Switchover to V_{BAT} Backup Supply
- Power-Fail Time-Stamp for Battery Switchover
- Low-Power CMOS Technology:
  - Dynamic Current: 400 μA max read
  - Dynamic Current: 400 μA max SRAM
  - Battery Backup Current: <700nA @ 1.8V
- 100 kHz and 400 kHz Compatibility
- ESD Protection >4,000V
- 1 Million Erase/Write Cycles for Unique ID
- Packages include 8-Lead SOIC, TSSOP, 2x3 TDFN, MSOP
- Pb-Free and RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C

Description:

The MCP7940X series of low-power Real-Time Clocks (RTC) uses digital timing compensation for an accurate clock/calendar, a programmable output control for versatility, a power sense circuit that automatically switches to the backup supply, and nonvolatile memory for data storage. Using a low-cost 32.768 kHz crystal, it tracks time using several internal registers. For communication, the MCP7940X uses the I²C™ bus.

The clock/calendar automatically adjusts for months with fewer than 31 days, including corrections for leap years. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator and settable alarm(s) to the second, minute, hour, day of the week, date or month. Using the programmable CLKOUT, frequencies of 32.768, 8.192 and 4.096 kHz and 1 Hz can be generated from the external crystal.

Along with the battery-backed SRAM memory, a 64-bit protected EEPROM space is available for a unique ID or MAC address to be programmed at the factory or by the end user.

The device is fully accessible through the serial interface while V_{CC} is between 1.8V and 5.5V, but can operate down to 1.3V for timekeeping and SRAM retention only.

The RTC series of devices are available in the standard 8-lead SOIC, TSSOP, MSOP and 2x3 TDFN packages.

Package Types

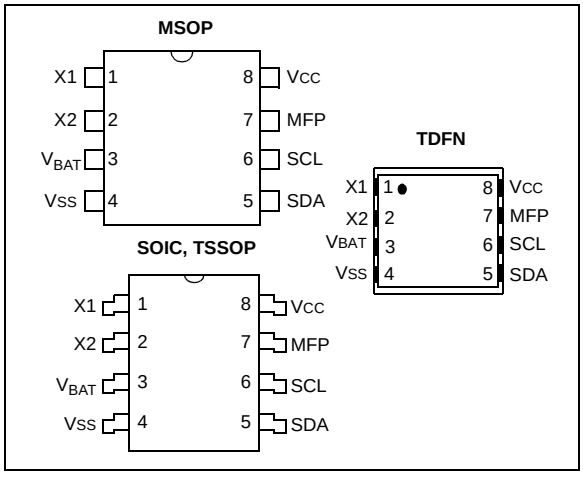
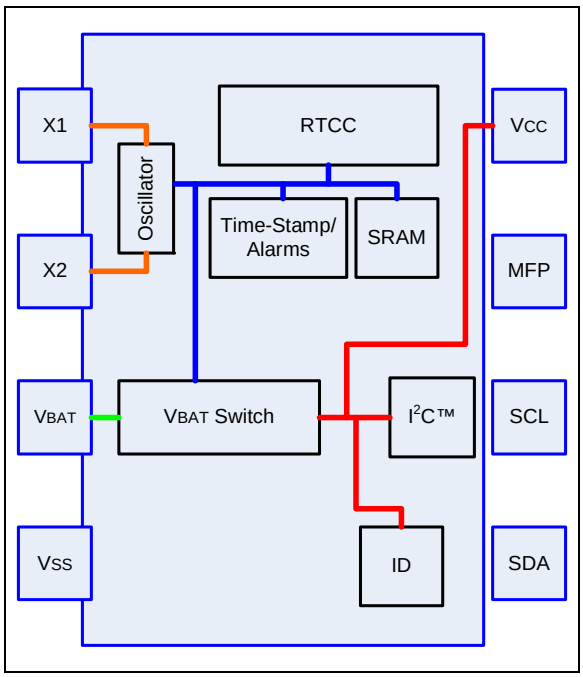


FIGURE 1-1: TYPICAL OPERATING CIRCUIT



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
	—	SCL, SDA pins	—		—	—	—
D1	VIH	High-level input voltage	0.7 VCC		—	V	—
D2	VIL	Low-level input voltage	—		0.3 VCC 0.2 VCC	V	VCC = 2.5V to 5.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC		—	V	**(Note 1)**
D4	VOL	Low-level output voltage (MFP, SDA)	—		0.40	V	IOL = 3.0 ma @ VCC = 4.5V IOL = 2.1 ma @ VCC = 2.5V
D5	ILI	Input leakage current	—		±1	µA	VIN = VSS or VCC
D6	ILO	Output leakage current	—		±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin capacitance (SDA, SCL and MFP)	—		10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, f = 400 kHz
D8	ICC Read	Operating current ID	—		400	µA	VCC = 5.5V, SCL = 400 kHz
	ICC Write		—		3	mA	VCC = 5.5V
D9	ICC Read	Operating current SRAM	—		300	µA	VCC = 5.5V, SCL = 400 kHz
	ICC Write		—		400	µA	VCC = 5.5V, SCL = 400 kHz
D10	ICCS	Standby current **(Note 2)**	—		5	µA	VCC = 5.5V, SCL = SDA = VCC
D11	IBAT	VBAT Standby Current **(Note 2)**	—	700	—	nA	VBAT = 1.8V @ 25°C
D12	VTRIP	VBAT Change Over	1.3		1.7	V	1.5V typical at TAMB = 25°C
D13	VCCFT	VCC Fall Time **(Note 1)**	300		—	µs	From VTRIP (max) to VTRIP (min)
D14	VCCRT	VCC Rise Time **(Note 1)**	0		—	µs	From VTRIP (min) to VTRIP (max)
D15	VBAT	VBAT Voltage Range **(Note 1)**	1.3		5.5	V	—

Note 1: This parameter is periodically sampled and not 100% tested.

2: Standby with oscillator running

TABLE 1-2: AC CHARACTERISTICS

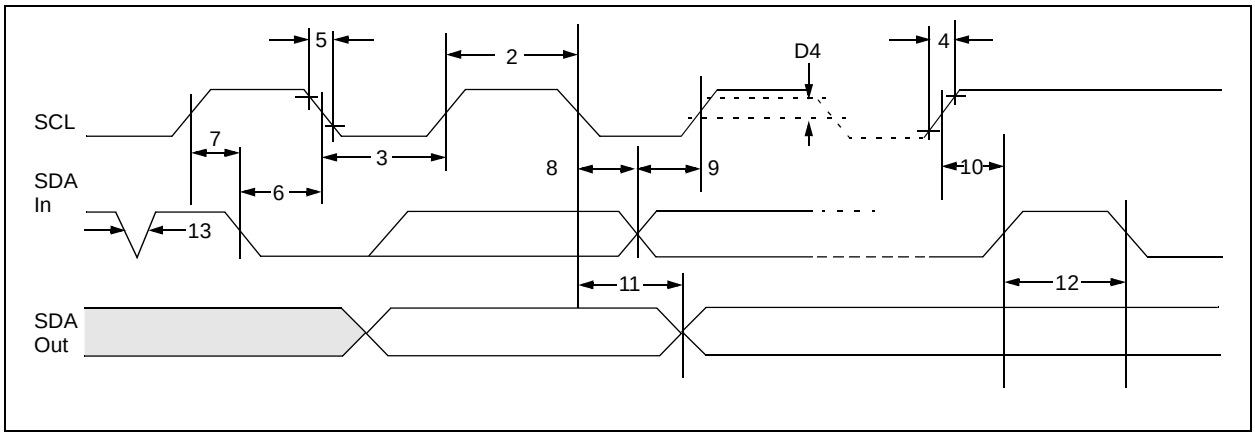
AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): V_{CC} = +1.8V to 5.5V T_A = -40°C to +85°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— —	100 400	kHz	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
2	T_{HIGH}	Clock high time	4000 600	— —	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
3	T_{LOW}	Clock low time	4700 1300	— —	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
4	T_R	SDA and SCL rise time **(Note 1)**	— —	1000 300	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
5	T_F	SDA and SCL fall time **(Note 1)**	— —	1000 300	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
6	$T_{HD:STA}$	Start condition hold time	4000 600	— —	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
7	$T_{SU:STA}$	Start condition setup time	4700 600	— —	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
8	$T_{HD:DAT}$	Data input hold time	0	—	ns	
9	$T_{SU:DAT}$	Data input setup time	250 100	— —	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
10	$T_{SU:STO}$	Stop condition setup time	4000 600	— —	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
11	T_{AA}	Output valid from clock	— —	3500 900	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
12	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	4700 1300	— —	ns	1.8V ≤ V_{CC} < 2.5V 2.5V ≤ V_{CC} ≤ 5.5V
13	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	50	ns	**(Note 1 and Note 2)**
14	T_{WC}	Write cycle time (byte or page)	—	5	ms	—
15	—	Endurance	1M	—	cycles	25°C, V_{CC} = 5.5V Page mode **(Note 3)**

Note 1: Not 100% tested.

2: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

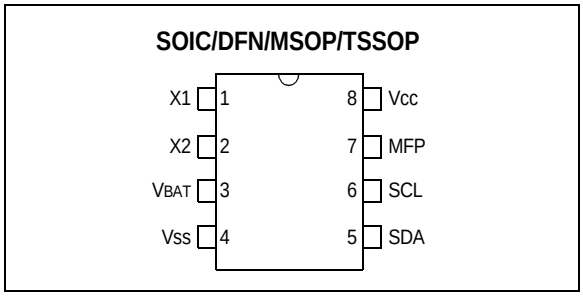
FIGURE 1-2: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

FIGURE 2-1: DEVICE PINOUTS



2.1 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typically 10 kΩ for 100 kHz, 2 kΩ for 400 kHz). For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.2 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

TABLE 2-1: PIN DESCRIPTIONS

Pin Name	Pin Function
Vss	Ground
SDA	Bidirectional Serial Data
SCL	Serial Clock
X1	Xtal Input, External Oscillator Input
X2	Xtal Output
VBAT	Battery Backup Input (3V Typ)
MFP	Multi Function Pin
Vcc	+1.8V to +5.5V Power Supply

3.0 I²C BUS CHARACTERISTICS

3.1 I²C Interface

The MCP7940X supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the Start and Stop conditions, while the MCP7940X works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.1.1 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1.1.1 Bus not Busy (A)

Both data and clock lines remain high.

3.1.1.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.1.1.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

3.1.1.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

3.1.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The MCP7940X does not generate any Acknowledge bits while an internal Unique ID programming cycle is in progress, but the user may still access the SRAM and RTCC registers.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (MCP7940X) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

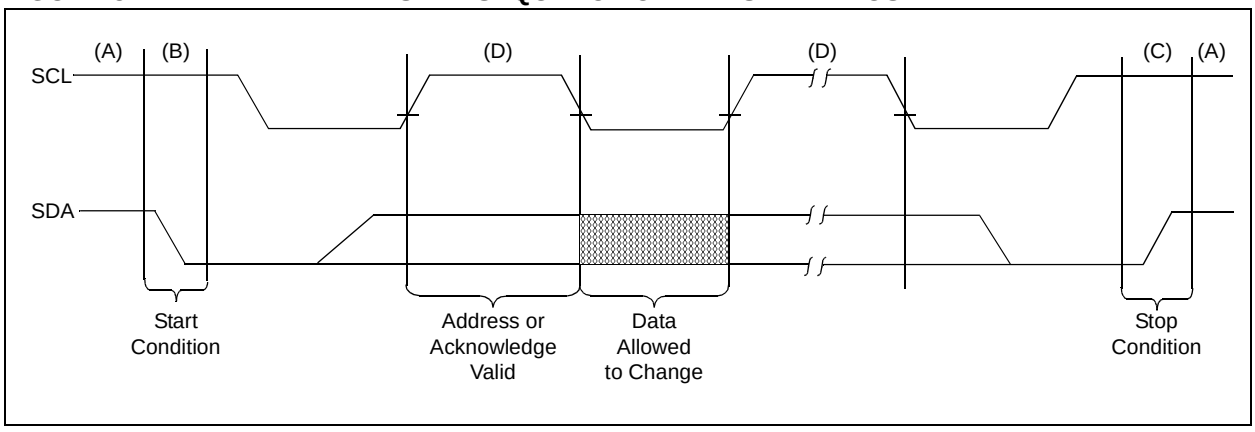
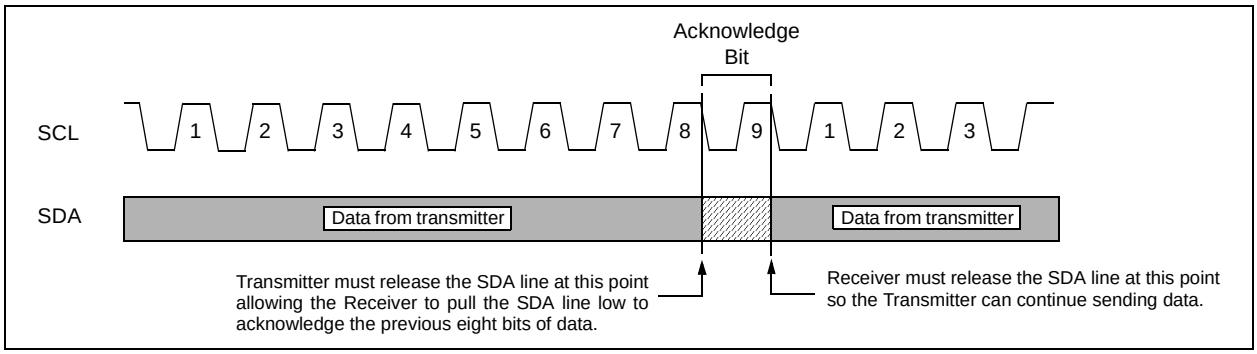


FIGURE 3-2: ACKNOWLEDGE TIMING



3.1.2 DEVICE ADDRESSING AND OPERATION

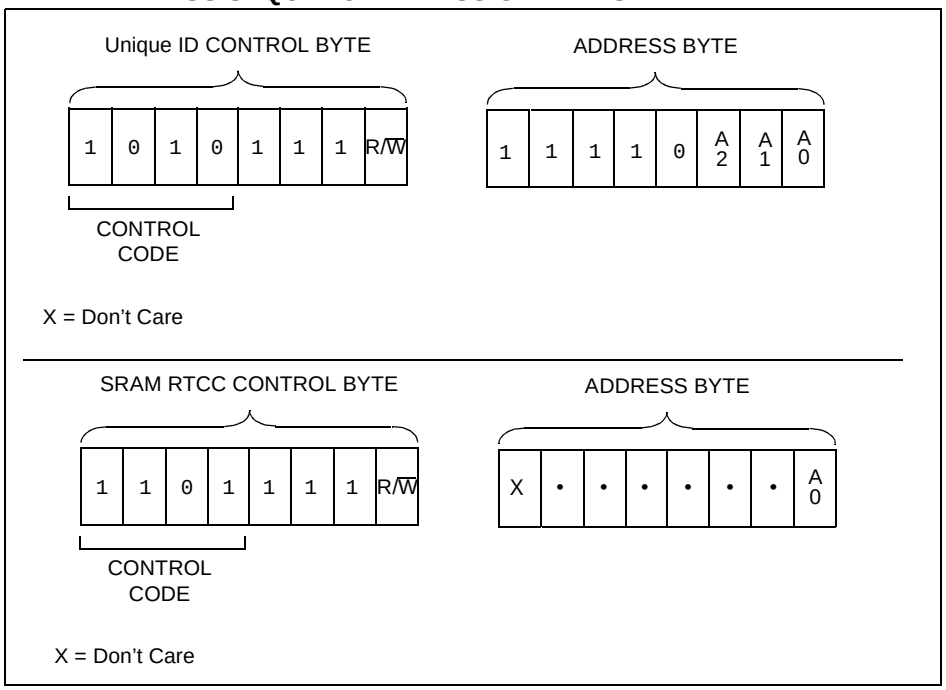
A control byte is the first byte received following the Start condition from the master device (Figure 3-2). The control byte consists of a control code; for the MCP7940X this is set as '1010111' for read and write operations for the Unique ID after the correct unlock sequence.

The control byte for accessing the SRAM and RTCC registers are set to '1101111'. The RTCC registers and the SRAM share the same address space.

The last bit of the control byte defines the operation to be performed. When set to a '1' a read operation is selected, and when set to a '0' a write operation is selected. The next byte received defines the address of the data byte (Figure 3-3). The upper address bits are transferred first, followed by the Least Significant bits (LSb).

Following the Start condition, the MCP7940X monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving an '1010111' or '1101111' code, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the MCP7940X will select a read or write operation.

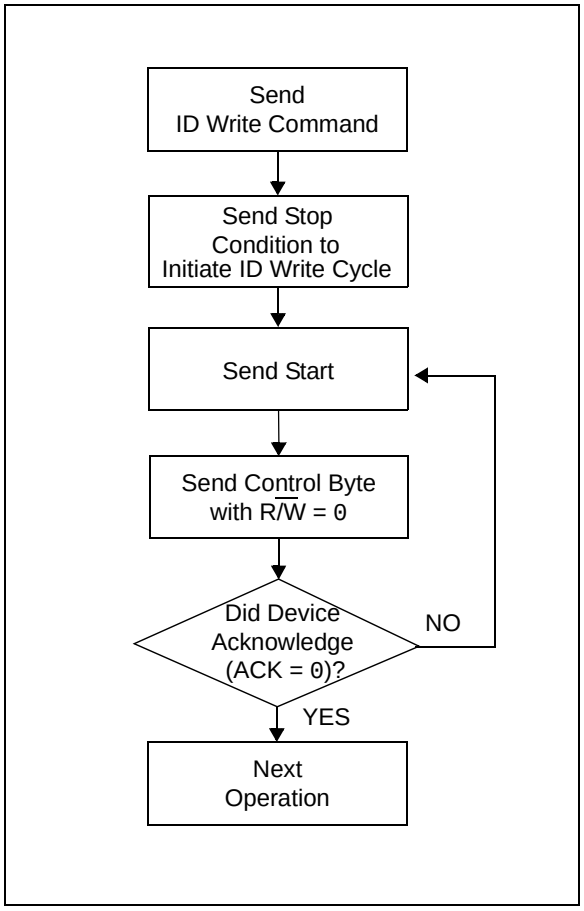
FIGURE 3-3: ADDRESS SEQUENCE BIT ASSIGNMENTS



3.1.3 ACKNOWLEDGE POLLING

Since the device will not acknowledge a Unique ID command during an ID write cycle, this can be used to determine when the cycle is complete. This feature can be used to maximize bus throughput. Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next Read or Write command. See Figure 3-4 for the flow diagram.

FIGURE 3-4: ACKNOWLEDGE POLLING FLOW



4.0 RTCC FUNCTIONALITY

The MCP7940X family is a highly integrated RTCC. On-board time and date counters are driven from a low-power oscillator to maintain the time and date. An integrated VCC switch enables the device to maintain the time and date and also the contents of the SRAM during a VCC power failure.

4.1 RTCC MEMORY MAP

The RTCC registers are contained in addresses 0x00h-0x1fh. 64 bytes of user-accessable SRAM are located in the address range 0x20-0x5f. The SRAM memory is a separate block from the RTCC control and Configuration registers. All SRAM locations are battery-backed-up during a VCC power fail. Unused locations are not accessible, MCP7940X will noACK after the address byte if the address is out of range. The shaded areas are not implemented and read as '0'. No error checking is provided when loading time and date registers.

- Addresses 0x00h-0x06h are the RTCC Time and Date registers. These are read/write registers. Care must be taken when writing to these registers while the oscillator is running.
- Incorrect data can appear in the Time and Date registers if a write is attempted during the timeframe where these internal registers are being incremented. The user can minimize the likelihood of data corruption by insuring that any writes to the Time and Date registers occur before the contents of the second register reach a value of 0x59H.
- Addresses 0x07h-0x09h are the device Configuration, Calibration and ID Unlock registers.
- Addresses 0x0Ah-0x10h are the Alarm 0 registers. These are used to set up the Alarm 0, the Interrupt polarity and the Alarm 0 compare.
- Addresses 0x11h-0x17h are the same as 0x0Bh-0x11h but are used for Alarm 1.
- Addresses 0x18h-0x1Fh are used for the timestamp feature.

The Memory Map is shown in Table 4-1.

TABLE 4-1: RTCC MEMORY MAP

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range	Reset State
00h	ST	10 Seconds			Seconds				Seconds	00-59	00h
01h		10 Minutes			Minutes				Minutes	00-59	00h
02h		12/$\overline{24}$	10 Hour AM/PM	10 Hour	Hour				Hours	1-12 + AM/PM 00 - 23	00h
03h			OSCON	VBAT	VBATEN	Day			Day	1-7	01h
04h			10 Date		Date				Date	01-31	01h
05h			LP	10 Month	Month				Month	01-12	01h
06h	10 Year				Year				Year	00-99	01h
07h	OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0	Control Reg.		80h
08h	CALIBRATION								Calibration		00h
09h	UNIQUE UNLOCK ID SEQUENCE								Unlock ID		00h
0Ah		10 Seconds			Seconds				Seconds	00-59	00h
0Bh		10 Minutes			Minutes				Minutes	00 - 59	00h
0Ch		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour				Hours	1-12 + AM/PM 00-23	00h
0Dh	ALM0POL	ALM0C2	ALM0C1	ALM0C0	ALM0IF	Day			Day	1-7	01h
0Eh			10 Date		Date				Date	01-31	01h
0Fh				10 Month	Month				Month	01-12	01h
10h	Reserved – Do not use								Reserved		01h
11h		10 Seconds			Seconds				Seconds	00-59	00h
12h		10 Minutes			Minutes				Minutes	00-59	00h
13h		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour				Hours	1-12 + AM/PM 00-23	00h
14h	ALM1POL	ALM1C2	ALM1C1	ALM1C0	ALM1IF	Day			Day	1-7	01h
15h			10 Date		Date				Date	01-31	01h
16h				10 Month	Month				Month	01-12	01h
17h	Reserved – Do not use								Reserved		01h
18h		10 Minutes			Minutes						00h
19h		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour						00h
1Ah			10 Date		Date						00h
1Bh	Day			10 Month	Month						00h

TABLE 4-1: RTCC MEMORY MAP (CONTINUED)

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range	Reset State
1Ch		10 Minutes			Minutes						00h
1Dh		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour						00h
1Eh			10 Date		Date						00h
1Fh	Day			10 Month	Month						00h

4.1.1 RTCC REGISTER ADDRESSES

0x00h – Contains the BCD seconds and 10 seconds. The range is 00 to 59. Bit 7 in this register is used to start or stop the on-board crystal oscillator. Setting this bit to a '1' starts the oscillator and clearing this bit to a '0' stops the on-board oscillator.

0x01h – Contains the BCD minutes and 10 minutes. The range is 00 to 59.

0x02h – Contains the BCD hour in bits 3:0. Bits 5:4 contain either the 10 hour in BCD for 24-hour format or the AM/PM indicator and the 10-hour bit for 12-hour format. Bit 6 determines the hour format. Setting this bit to '0' enables 24-hour format, setting this bit to '1' enables 12-hour format.

0x03h – Contains the BCD day. The range is 1-7. Additional bits are also used for configuration and status.

- Bit 3 is the VBATEN bit. If this bit is set, the internal circuitry is connected to the V_{BAT} pin when V_{CC} fails. If this bit is '0' then the V_{BAT} pin is disconnected and the only current drain on the external battery is the V_{BAT} pin leakage.
- Bit 4 is the V_{BAT} bit. This bit is set by hardware when the V_{CC} fails and the V_{BAT} is used to power the Oscillator and the RTCC registers. This bit is cleared by software. Clearing this bit will also clear all the time-stamp registers.
- Bit 5 is the OSCON bit. This is set and cleared by hardware. If this bit is set, the oscillator is running, if cleared, the oscillator is not running. This bit does not indicate that the oscillator is running at the correct frequency. The RTCC will wait 32 oscillator cycles before the bit is set. The RTCC will wait roughly 32 clock cycles to clear this bit.

0x04h – Contains the BCD date and 10 date. The range is 01-31.

0x05h – Contains the BCD month. Bit 4 contains the 10 month. Bit 5 is the Leap Year bit, which is set during a leap year and is read-only.

0x06h – Contains the BCD year and 10 year. The Range is 00-99.

0x07h – Is the Control register.

- Bit 7 is the OUT bit. This sets the logic level on the MFP when not using this as a square wave output.
- Bit 6 is the SQWE bit. Setting this bit enables the divided output from the crystal oscillator.
- Bits 5:4 determine which alarms are active.
  - 00 – No Alarms are active
  - 01 – Alarm 0 is active
  - 10 – Alarm 1 is active
  - 11 – Both Alarms are active
- Bit 3 is the EXTOSC enable bit. Setting this bit will allow an external 32.768 kHz signal to drive the RTCC registers eliminating the need for an external crystal.
- Bit 2:0 sets the internal divider for the 32.768 kHz oscillator to be driven to the MFP. The duty cycle is 50%. The output is responsive to the Calibration register. The following frequencies are available:
  - 000 – 1 Hz
  - 001 – 4.096 kHz
  - 010 – 8.192 kHz
  - 011 – 32.768 kHz
  - 1xx enables the Cal output function. Cal output appears on MFP if SQWE is set (64 Hz Nominal).

Note: The RTCC counters will continue to increment during the calibration.

0x08h is the Calibration register. This is an 8-bit register that is used to add or subtract clocks from the RTCC counter every minute. The MSB is the sign bit and indicates if the count should be added or subtracted. The remaining 7 bits, with each bit adding or subtracting 2 clocks, give the user the ability to add or subtract up to 254 clocks per minute.

0x09h is the unlock sequence address. To unlock write access to the unique ID area in the EEPROM, a sequence must be written to this address in separate commands. The process is fully detailed in **Section 4.2.1 "Unlock Sequence"**.

0x0Ah-0x0fh and 0x11-0x16h are the Alarm 0 and Alarm 1 registers. The bits are the same as the RTCC bits with the following differences:

Locations 0x10h and 0x17h are reserved and should not be used to allow for future device compatibility.

0x0Dh/0x14h has additional bits for alarm configuration.

- ALMxPOL: This bit specifies the level that the MFP will drive when the alarm is triggered. ALM2POL is a copy of ALM1POL. The default state of the MFP when used for alarms is the inverse of ALM1POL.
- ALMxIF: This is the Alarm Interrupt Fag. This bit is set in hardware if the alarm was triggered. The bit is cleared in software.
- ALMxC2:0: These Configuration bits determine the alarm match. The logic will trigger the alarm based on one of the following match conditions:

  000 – Seconds match

  001 – Minutes match

  010 – Hours match (takes into account 12/24 hour)

  011 – Matches the current day, interrupt at 12.00.00 a.m. Example: 12 midnight on

  100 – Date

  101 – RESERVED

  110 – RESERVED

  111 – Seconds, Minutes, Hour, Day, Date, Month
- The 12/24-hour bits 0xCh.6 and 0x13h.6 are copies of the bit in 0x02h.6. The bits are read-only.

0x18h-0x1Bh are used for the timesaver function. These registers are loaded at the time when VCC fails and the RTCC operates on the VBAT. The VBAT bit is also set at this time. These registers are cleared when the VBAT bit is cleared in software.

0x1Ch-0x1Fh are used for the timesaver function. These registers are loaded at the time when VCC is restored and the RTCC switches to VDD. These registers are cleared when the VBAT bit is cleared in software.

Note:	It is strongly recommended that the timesaver function only be used when the oscillator is running. This will ensure accurate functionality.

4.2 FEATURES

4.2.1 UNLOCK SEQUENCE

The unique ID location is user accessible by using the unlock ID sequence.

The unique ID location is 64-bits (8 bytes) and is stored in EEPROM locations 0xF0 to 0xF7. This location can be read at any time, however, a write is inhibited until unlocked.

To unlock the write access to this location the following sequence must be completed:

- A single write of 0x55h to address 0x09. Stop
- A single write of 0xAAh to address 0x09. Stop

This will allow the unique EEPROM locations to be written.

After the byte or page write to these locations, the write sequence is initiated by the Stop condition. At this time, the ID locations are locked and no further writes are possible to this location unless a complete unlock sequence is repeated.

4.2.2 CALIBRATION

The MCP7940X utilizes digital calibration to correct for inaccuracies of the input clock source (either external or crystal). Calibration is enabled by setting the value of the Calibration register at address 08H. Calibration is achieved by adding or subtracting a number of input clock cycles per minute in order to achieve ppm level adjustments in the internal timing function of the MCP7940X.

The MSB of the Calibration register is the sign bit, with a '1' indicating subtraction and a '0' indicating addition. The remaining seven bits in the register indicate the number of input clock cycles (multiplied by two) that are subtracted or added per minute to the internal timing function.

The internal timing function can be monitored using the MFP open-drain output pin by setting bit [6] (SQWE) and bits [2:0] (RS2, RS1, RS0) of the control register at address 07H. Note that the MFP output waveform is disabled when the MCP7940X is running in VBAT mode. With the SQWE bit set to '1', there are two methods that can be used to observe the internal timing function of the MCP7940X:

A. RS2 BIT SET TO '0'

With the RS2 bit set to '0', the RS1 and RS0 bits enable the following internal timing signals to be output on the MFP pin:

RS2	RS1	RS0	Output Signal
0	0	0	1 Hz
0	0	1	4.096 kHz
0	1	0	8.192 kHz
0	1	1	32.768 kHz

The frequencies listed in the table presume an input clock source of exactly 32.768 kHz. In terms of the equivalent number of input clock cycles, the table becomes:

RS2	RS1	RS0	Output Signal
0	0	0	32768
0	0	1	8
0	1	0	4
0	1	1	1

With regards to the calibration function, the Calibration register setting has no impact upon the MFP output clock signal when bits RS1 and RS0 are set to '11'. The setting of the Calibration register to a non-zero value (i.e., values other than 00H or 80H) enables the calibration function which can be observed on the MFP output pin. The calibration function can be expressed in terms of the number of input clock cycles added/subtracted from the internal timing function.

With bits RS1 and RS0 set to '00', the calibration function can be expressed as:

$$T_{output} = (32768 +/- (2 * CALREG))\ T_{input}$$

where:

T_{output} = clock period of MFP output signal

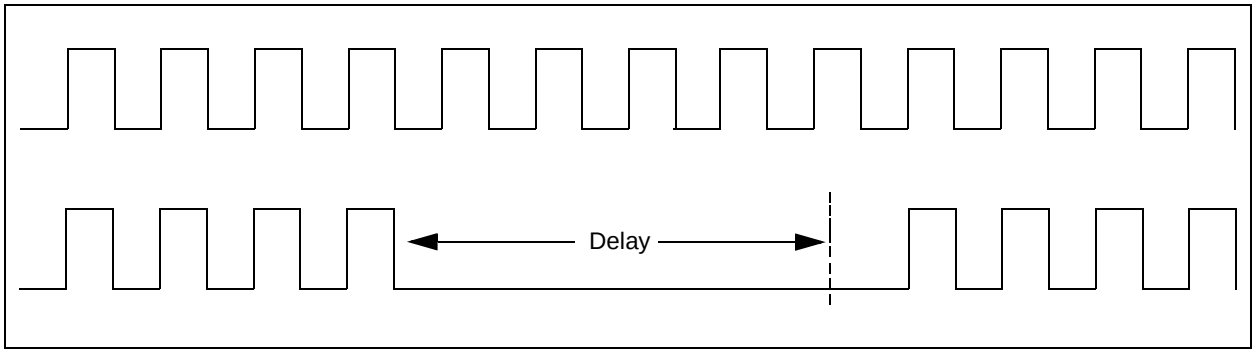
T_{input} = clock period of input signal

CALREG = decimal value of Calibration register setting and the sign is determined by the MSB of Calibration register.

Since the calibration is done once per minute (i.e., when the internal minute counter is incremented), only one cycle in sixty of the MFP output waveform is affected by the calibration setting. Also note that the duty cycle of the MFP output waveform will not necessarily be at 50% when the calibration setting is applied.

With bits RS1 and RS0 set to '01' or '10', the calibration function can not be expressed in terms of the input clock period. In the case where the MSB of the Calibration register is set to '0', the waveform appearing at the MFP output pin will be "delayed", once per minute, by twice the number of input clock cycles defined in the Calibration register. The MFP waveform will appear as:

FIGURE 4-1: RS1 AND RS0 WITH AND WITHOUT CALIBRATION



In the case where the MSB of the Calibration register is set to '1', the MFP output waveforms that appear when bits RS1 and RS0 are set to '01' or '10' are not as responsive to the setting of the Calibration register. For example, when outputting the 4.096 kHz waveform (RS1, RS0 set to '01'), the output waveform is generated using only eight input clock cycles. Consequently, attempting to subtract more than eight input clock cycles from this output does not have a meaningful effect on the resulting waveform. Any effect on the output will appear as a modification in both the frequency and duty cycle of the waveform appearing on the MFP output pin.

B.RS2 BIT SET TO '1'

With the RS2 bit set to '1', the following internal timing signal is output on the MFP pin:

RS2	RS1	RS0	Output Signal
1	x	x	64.0 Hz

The frequency listed in the table presumes an input clock source of exactly 32.768 kHz. In terms of the equivalent number of input clock cycles, the table becomes:

RS2	RS1	RS0	Output Signal
1	x	x	512

Unlike the method previously described, the calibration setting is continuously applied and affects every cycle of the output waveform. This results in the modulation of the frequency of the output waveform based upon the setting of the Calibration register.

Using this setting, the calibration function can be expressed as:

$$T_{output} = (2 * (256 +/- (2 * CALREG))) T_{input}$$

where:

T_{output} = clock period of MFP output signal

T_{input} = clock period of input signal

CALREG = decimal value of the Calibration register setting, and the sign is determined by the MSB of the Calibration register.

Since the calibration is done every cycle, the frequency of the output MFP waveform is constant.

4.2.3 MFP

Pin 7 is a multi-function pin and supports the following functions:

- Use of the OUT bit in the Control register for single bit I/O
- Alarm Outputs – Available in VBAT mode
- FOUT mode – driven from a FOSC divider – Not available in VBAT mode

The internal control logic for the MFP is connected to the switched internal supply bus, this allows operation in VBAT mode. The Alarm Output is the only mode that operates in VBAT mode, other modes are suspended.

4.2.4 VBAT

If the VBAT feature is not being used, the VBAT pin should be connected to GND. A low-value series resistor is recommended between the external battery and the VBAT pin.

The VBAT point is defined as 1.5V typical. When VDD falls below 1.5V the system will continue to operate the RTCC and SRAM using the VBAT supply. The following conditions apply:

TABLE 4-2:

Supply Condition	Read/Write Access	Powered By
VCC < VTRIP, VCC < VBAT	No	VBAT
VCC > VTRIP, VCC < VBAT	Yes	VCC
VCC > VTRIP, VCC > VBAT	Yes	VCC

4.2.5 CRYSTAL SPECS

The MCP7940X has been designed to operate with a standard 32 kHz crystal. Devices with a specified load capacitance of either 12pF or 6pF can be used. The end user should fully validate the chosen crystal across all the expected design parameters of the system to ensure correct operation.

The following crystals have been tested and shown to work with the MCP7940X:

- CM200S 12pF surface mount crystals from Citizen
- ECS-.327 12pF surface mount crystals from ECS INC
- CFS206 12pF leaded crystals from Citizen

This is not a definitive list and all crystals should be tested in the target application across all temperature, voltage and other significant environmental conditions.

4.2.6 POWER-FAIL TIME-STAMP

The MCP7940X family of RTCC devices feature a power-fail time-stamp feature. This feature will save the time at which V_{CC} crosses the V_{TRIP} voltage. To use this feature, a V_{BAT} supply must be present and the oscillator must also be running.

There are two separate sets of registers that are used to record this information:

- The first set located at 0x18h through 0x1Bh are loaded at the time when V_{CC} fails and the RTCC operates on the V_{BAT}. The V_{BAT} (register 0x03h bit 4) bit is also set at this time.
- The second set of registers, located at 0x1Ch through 0x1Fh, are loaded at the time when V_{CC} is restored and the RTCC switches to V_{CC}.

The power-fail time-stamp registers are cleared when the V_{BAT} bit is cleared in software.

5.0 ON BOARD MEMORY

The MCP7940X has both on-board Unique ID memory and battery-backed SRAM. The SRAM is arranged as 64 x 8 bytes and is retained when the VCC supply is removed, provided the VBAT supply is present and enabled. The Unique ID is nonvolatile memory and does not require the VBAT supply for retention.

5.1 SRAM

FIGURE 5-1: SRAM/RTCC BYTE WRITE

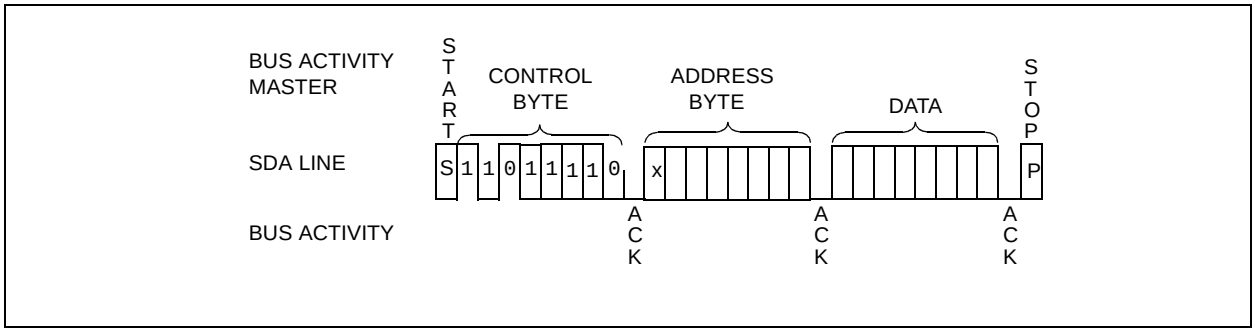
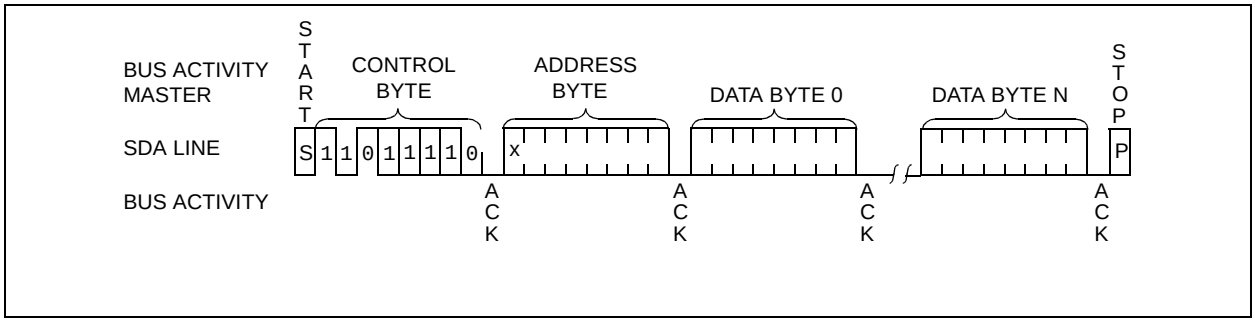


FIGURE 5-2: SRAM/RTCC MULTIPLE BYTE WRITE



The 64 bytes of user SRAM are at location 0x20h and can be accessed during an RTCC update. Upon POR the SRAM will be in an undefined state.

Writing to the SRAM and RTCC is accomplished in a similar way to writing to the EEPROM (as described later in this document) with the following considerations:

- There is no page. The entire 64 bytes of SRAM or 32 bytes of RTCC register can be written in one command.
- The SRAM allows an unlimited number of read/write cycles with no cell wear out.
- The RTCC and SRAM are not accessible when the device is running on the external VBAT.
- The RTCC and SRAM are separate blocks. The SRAM array may be accessed during an RTCC update.
- Read and write access is limited to either the RTCC register block or the SRAM array. The Address Pointer will rollover to the start of the addressed block.
- Data written to the RTCC and SRAM are on a per byte basis.

Note: Entering an address past 5F for an SRAM operation will result in the MCP7940X not acknowledging the address.

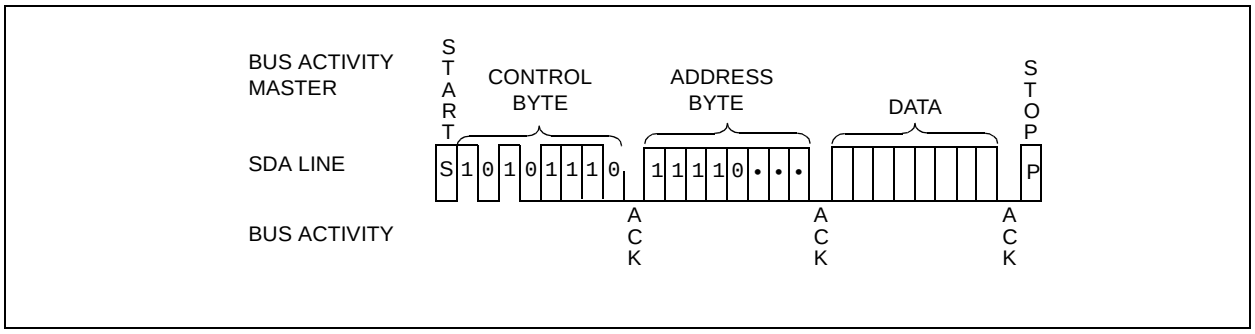
5.2 ID

5.2.1 ID BYTE WRITE

Following the Start condition from the master, the control code and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the MCP7940X. After receiving another Acknowledge signal from the MCP7940X, the master device transmits the data word to be written into the addressed memory location. The MCP7940X acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and, during this time, the MCP7940X does not generate Acknowledge signals for Unique ID Write commands. If an attempt is made to write to an address and the protection is set then the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a Byte Write command, the internal address counter will point to the address location following the one that was just written.

Note:	Addressing undefined ID locations will result in the MCP7940X not acknowledging the address.

FIGURE 5-3: ID BYTE WRITE



5.2.2 READ OPERATION

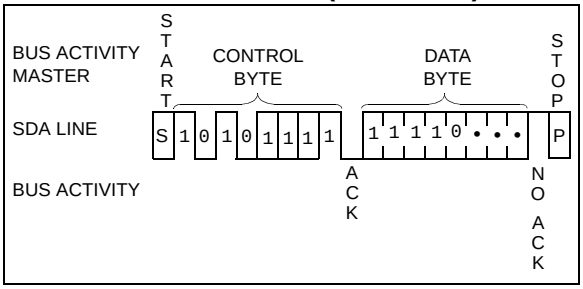
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read, and sequential read. The SRAM array can be read in the same way as the ID using the control byte for the SRAM '1101111' with a valid address.

5.2.2.1 Current Address Read

The MCP7940X contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the MCP7940X issues an Acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the MCP7940X discontinues transmission (Figure 5-5).

FIGURE 5-4: CURRENT ADDRESS READ (ID SHOWN)



5.2.2.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the MCP7940X as part of a write operation (R/$\overline{W}$ bit set to '0'). After the word address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The MCP7940X will then issue an Acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but it does generate a Stop condition which causes the MCP7940X to discontinue transmission (Figure 5-6). After a random read command, the internal address counter will point to the address location following the one that was just read.

5.2.2.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the MCP7940X transmits the first data byte, the master issues an Acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the MCP7940X to transmit the next sequentially addressed 8-bit word (Figure 5-7). Following the final byte transmitted to the master, the master will NOT generate an Acknowledge but will generate a Stop condition. To provide sequential reads, the MCP7940X contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over to the start of the Block.

FIGURE 5-5: RANDOM READ (UNIQUE ID SHOWN)

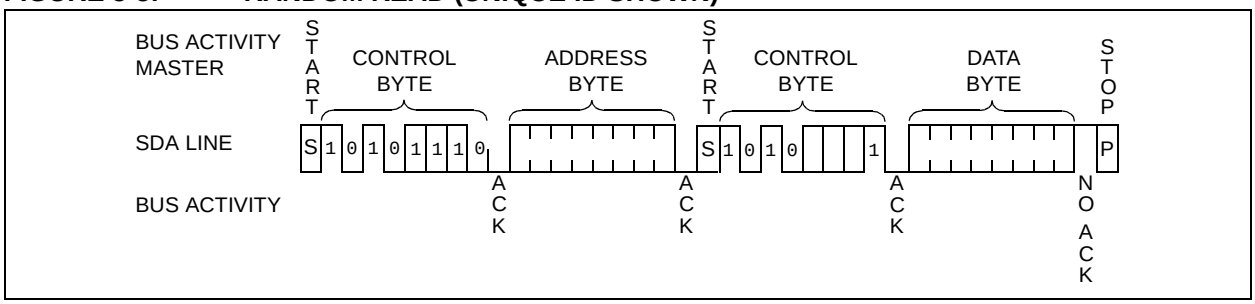
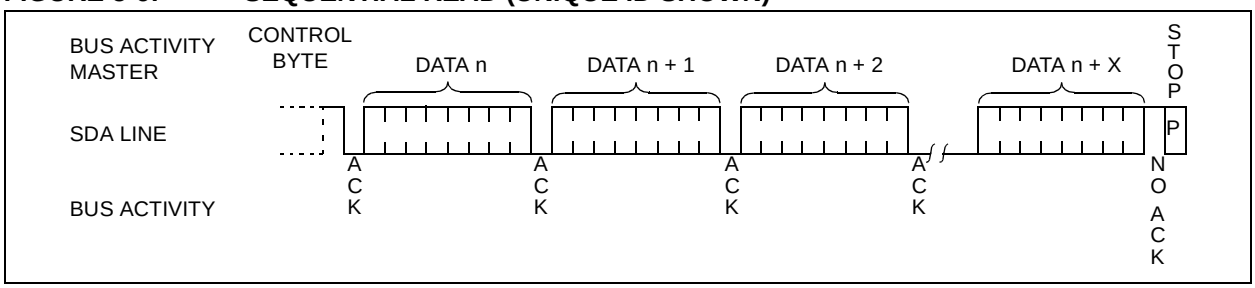


FIGURE 5-6: SEQUENTIAL READ (UNIQUE ID SHOWN)



5.3 Unique ID

The MCP7940X features an additional 64-bit unique ID area.

The unique ID is located at addresses 0xF0 through 0xF7. Reading the unique ID requires the user to simply address these bytes.

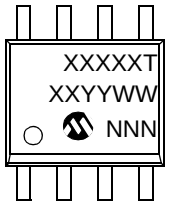
The unique ID area is protected to prevent unintended writes to these locations. The unlock sequence is detailed in **4.2.1 "Unlock Sequence"**.

The unique ID can be factory programmed on some devices to provide a unique IEEE EUI-48 or EUI-64 value. In addition, customer-provided codes can also be programmed.

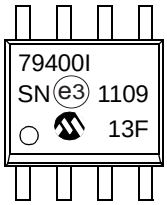
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

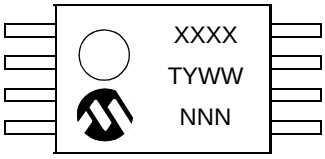
8-Lead SOIC (3.90 mm)



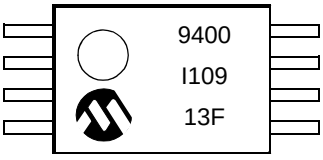
Example:



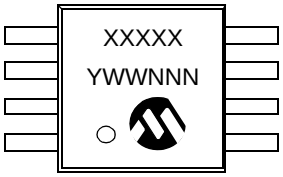
8-Lead TSSOP



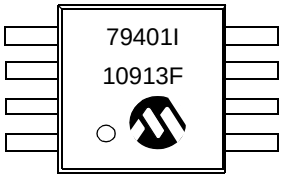
Example:



8-Lead MSOP

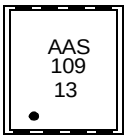


Example:



8-Lead 2x3 TDFN

Example:



Part Number	1st Line Marking Codes		
	TSSOP	MSOP	TDFN
MCP79400	9400	79400T	AAS
MCP79401	9401	79401T	AAT
MCP79402	9402	79402T	AAU

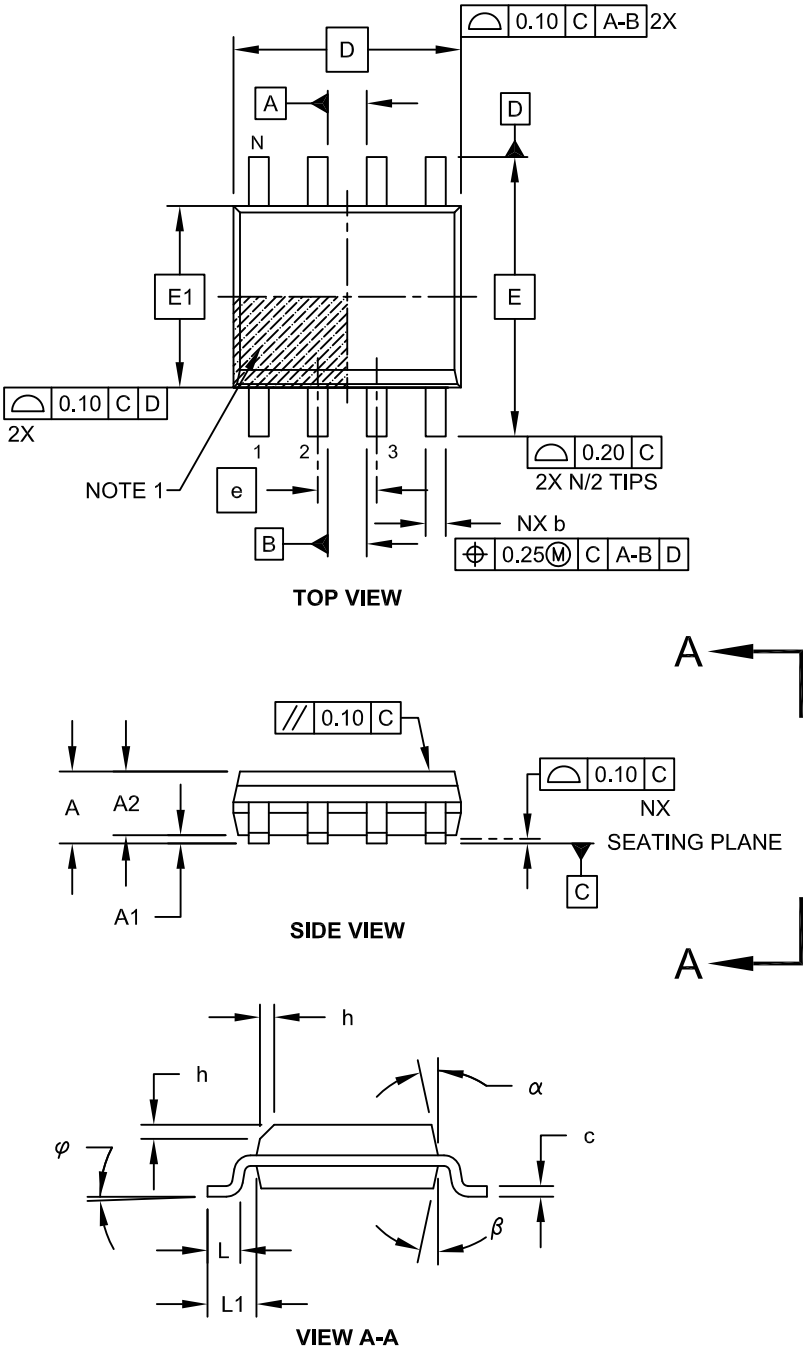
Note: T = Temperature grade
NN = Alphanumeric traceability code

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

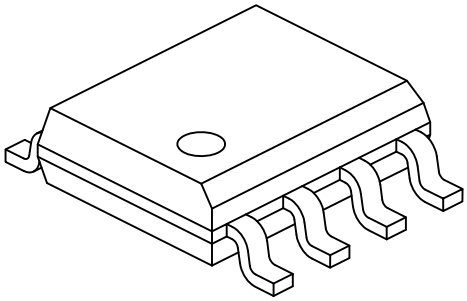
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

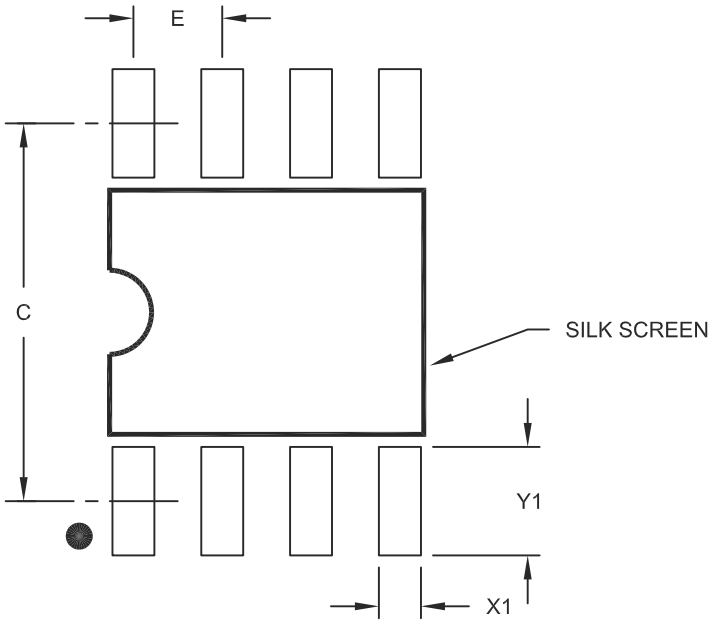
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

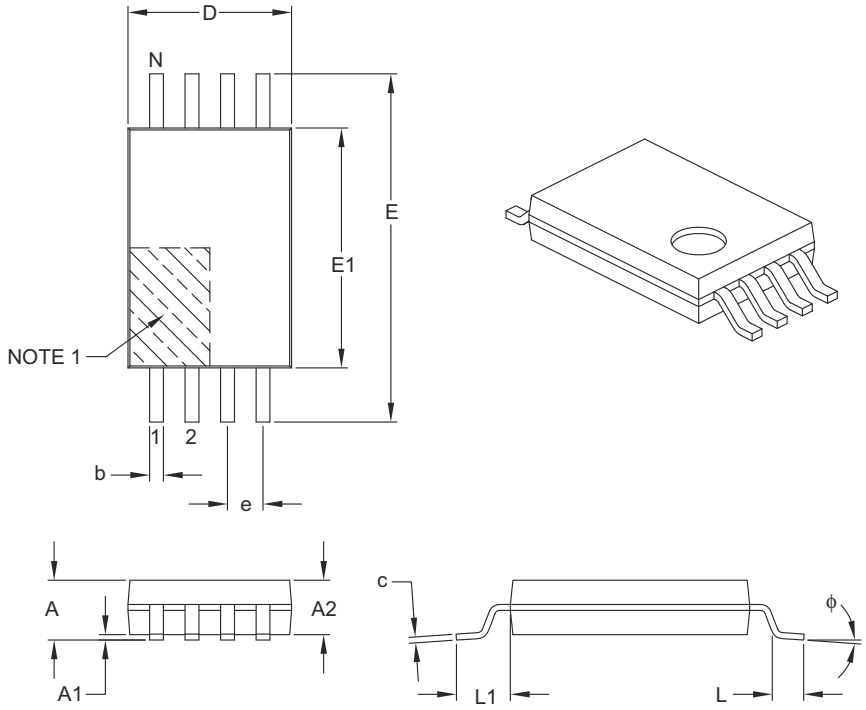
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

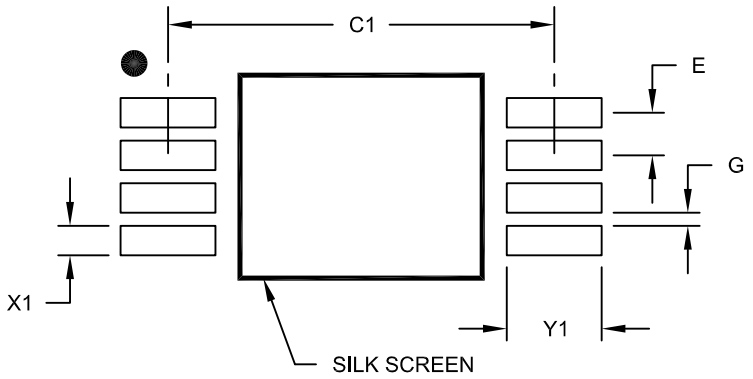
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

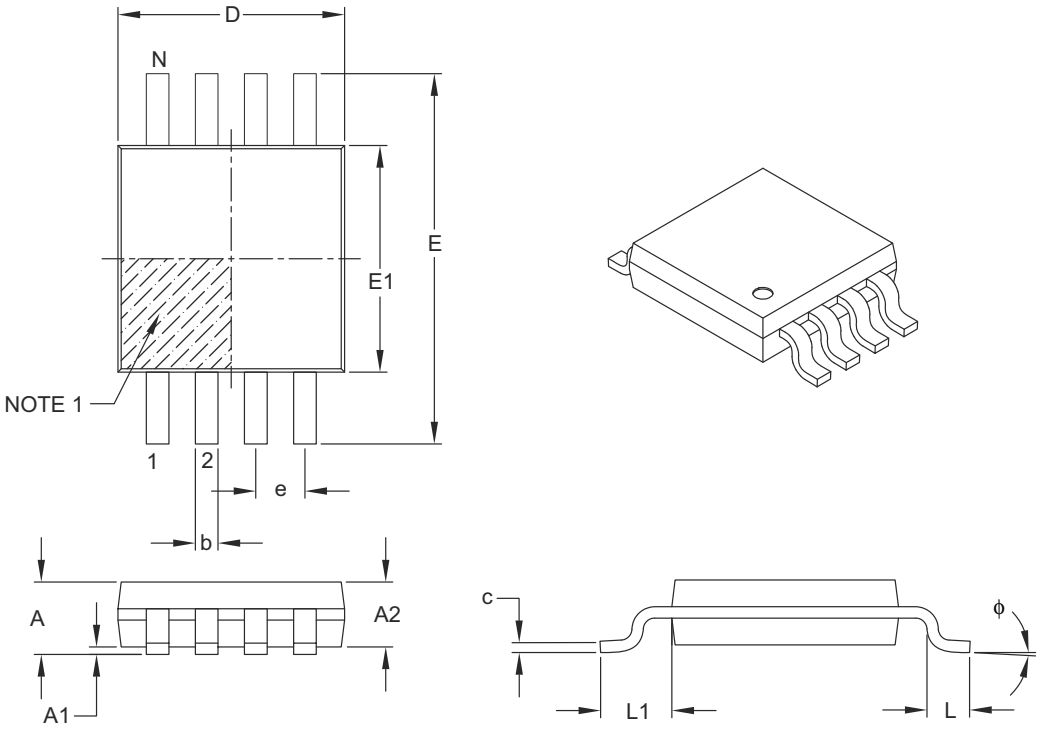
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

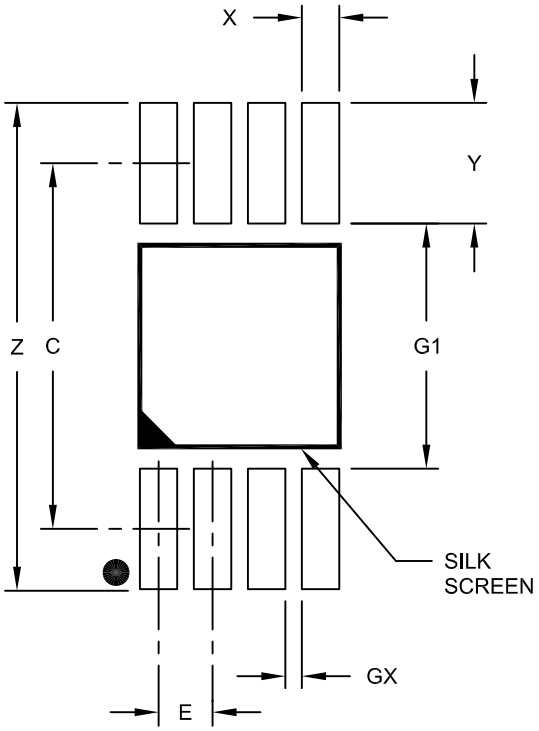
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

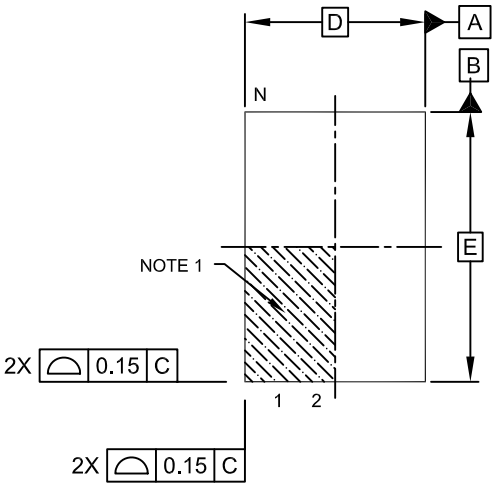
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

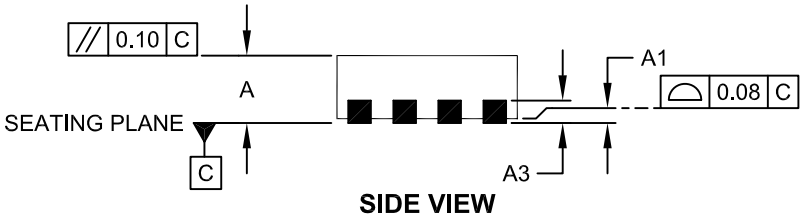
Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

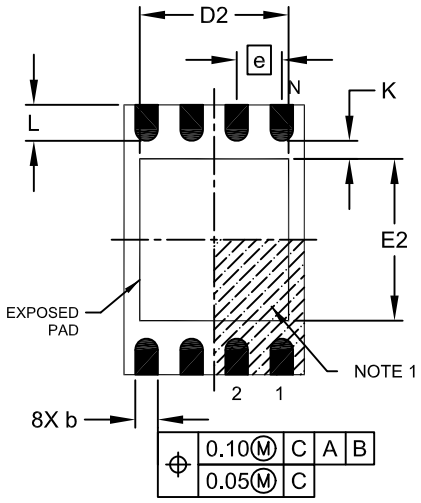
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

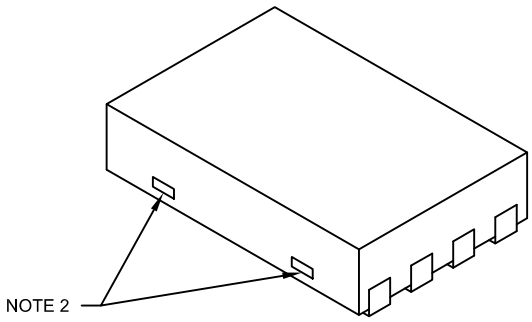


BOTTOM VIEW

Microchip Technology Drawing No. C04-129C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

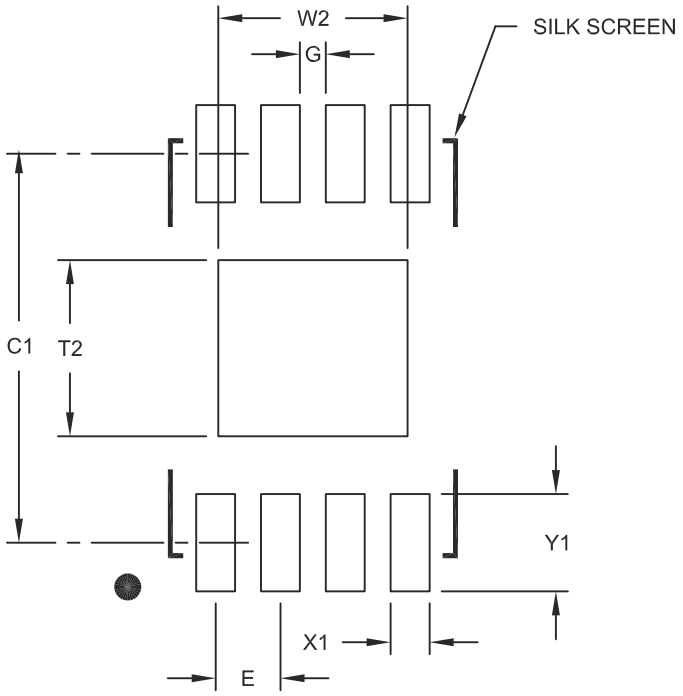
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision A (04/2011)

Original release of this document.

NOTES:

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PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP79400	=	1.8V - 5.5V I²C™ Serial RTCC
	MCP79400T	=	1.8V - 5.5V I²C Serial RTCC (Tape and Ree)
	MCP79401	=	1.8V - 5.5V I²C Serial RTCC, EUI-48™
	MCP79401T	=	1.8V - 5.5V I²C Serial RTCC, EUI-48™ (Tape and Reel)
	MCP79402	=	1.8V - 5.5V I²C Serial RTCC, EUI-64™
	MCP79402T	=	1.8V - 5.5V I²C Serial RTCC, EUI-64™ (Tape and Reel)
Temperature Range:	I	=	-40°C to +85°C
Package:	SN	=	8-Lead Plastic Small Outline (3.90 mm body)
	ST	=	8-Lead Plastic Thin Shrink Small Outline (4.4 mm)
	MS	=	8-Lead Plastic Micro Small Outline
	MNY(1)	=	8-Lead Plastic Dual Flat, No Lead

Note 1: 'Y' indicates a Nickel Palladium Gold (NiPdAu) finish.

Examples:

a) MCP79400-I/SN: Industrial Temperature, SOIC package.

b) MCP79400T-I/SN: Industrial Temperature, SOIC package, Tape and Reel.

c) MCP79400T-I/MNY: Industrial Temperature, TDFN package.

d) MCP79401-I/SN: Industrial Temperature, SOIC package, EUI-48™.

e) MCP79401-I/MS: Industrial Temperature MSOP package, EUI-48™.

f) MCP79402-I/SN: Industrial Temperature, SOIC package, EUI-64™.

g) MCP79402-I/ST: Industrial Temperature, TSSOP package, EUI-64™.

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