

### FEATURES

**Micropower at high voltage (18 V): 18  $\mu$ A typical**

**Single-supply operation: 2.7 V to 18 V**

**Dual-supply operation:  $\pm 1.35$  V to  $\pm 9$  V**

**Low input bias current: 20 pA**

**Gain bandwidth product: 200 kHz**

**Unity-gain stable**

### APPLICATIONS

**Portable medical equipment**

**Current monitors**

**4 mA to 20 mA loop drivers**

**Buffer/level shifting**

**Multipole filters**

**Remote/wireless sensors**

**Low power transimpedance amplifiers**

### GENERAL DESCRIPTION

The AD8546 is a dual, micropower, high impedance, rail-to-rail input/output amplifier optimized for low power and wide operating supply voltage range applications.

The AD8546 operates from 2.7 V up to 18 V with a typical supply current of 18  $\mu$ A. The combination of low supply current, high input impedance, and rail-to-rail input and output makes the AD8546 ideal for dc gain and buffering of sensor front ends or high impedance input sources in wireless or remote sensors or transmitters.

With its low power consumption and rail-to-rail input and output, the AD8546 is ideally suited for a variety of battery-powered, portable applications such as ECGs, pulse monitors, glucose meters, smoke and fire detectors, vibration monitors, and backup battery sensors.

The AD8546 is specified over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and is available in an 8-lead MSOP.

### PIN CONFIGURATION



Figure 1. 8-Lead MSOP

Table 1. Micropower Op Amps<sup>1</sup>

Amplifier	Supply Voltage		
	5 V	12 V to 16 V	36 V
Single	AD8500 ADA4505-1 AD8505 AD8541 AD8603	AD8663	
Dual	AD8502 ADA4505-2 AD8506 AD8542 AD8607	AD8667 OP281	OP295 ADA4062-2
Quad	AD8504 ADA4505-4 AD8508 AD8544 AD8609	AD8669 OP481	OP495 ADA4062-4

<sup>1</sup> See [www.analog.com](http://www.analog.com) for the latest selection of micropower op amps.

#### Rev. 0

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## REVISION HISTORY

1/11—Revision 0: Initial Version

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

$V_{SY} = 2.7\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to }2.7\text{ V}$			3	mV
		$V_{CM} = 0.3\text{ V to }2.4\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			4	mV
		$V_{CM} = 0\text{ V to }2.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			5	mV
		$V_{CM} = 0.3\text{ V to }2.4\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			4	mV
		$V_{CM} = 0\text{ V to }2.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			12.5	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.6	nA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }2.7\text{ V}$	60	75		dB
		$V_{CM} = 0.3\text{ V to }2.4\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	59			dB
		$V_{CM} = 0\text{ V to }2.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	57			dB
		$V_{CM} = 0.3\text{ V to }2.4\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	58			dB
		$V_{CM} = 0\text{ V to }2.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	49			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega; V_O = 0.5\text{ V to }2.2\text{ V}$	92	105		dB
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	75			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	65			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		$\mu\text{V}/^\circ\text{C}$
Input Resistance	$R_{IN}$			10		G $\Omega$
Input Capacitance						
Differential Mode	$C_{INDM}$			3.5		pF
Common Mode	$C_{INCM}$			3.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega\text{ to }V_{CM}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.69			V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega\text{ to }V_{CM}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			10	mV
Short-Circuit Current	$I_{SC}$			$\pm 4$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}; A_V = +1$		20		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to }18\text{ V}$	90	120		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70			dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$		18	22	$\mu\text{A}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			33	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		38		V/ms
Settling Time to 0.1%	$t_S$	$V_{IN} = 1\text{ V step}; R_L = 100\text{ k}\Omega; C_L = 10\text{ pF}$		14		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		170		kHz
Phase Margin	$\Phi_M$	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		69		Degrees
Channel Separation	CS	$f = 10\text{ kHz}; R_L = 1\text{ M}\Omega$		105		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		6		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		60		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		56		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

## ELECTRICAL CHARACTERISTICS—10 V OPERATION

$V_{SY} = 10\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to }10\text{ V}$			3	mV
		$V_{CM} = 0.3\text{ V to }9.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			4.2	mV
		$V_{CM} = 0\text{ V to }10\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			5	mV
		$V_{CM} = 0.3\text{ V to }9.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			8.5	mV
		$V_{CM} = 0\text{ V to }10\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			12.5	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2	15	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.6	nA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }10\text{ V}$	70	88		dB
		$V_{CM} = 0\text{ V to }10\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	70			dB
		$V_{CM} = 0\text{ V to }10\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	60			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega; V_O = 0.5\text{ V to }9.5\text{ V}$	95	115		dB
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	90			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	67			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		$\mu\text{V}/^\circ\text{C}$
Input Resistance	$R_{IN}$			10		G $\Omega$
Input Capacitance						
Differential Mode	$C_{INDM}$			3.5		pF
Common Mode	$C_{INCM}$			3.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega\text{ to }V_{CM}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	9.98			V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega\text{ to }V_{CM}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			20	mV
Short-Circuit Current	$I_{SC}$			$\pm 11$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}; A_V = +1$		15		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to }18\text{ V}$	90	120		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70			dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$		18	22	$\mu\text{A}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			33	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		60		V/ms
Settling Time to 0.1%	$t_s$	$V_{IN} = 1\text{ V step}; R_L = 100\text{ k}\Omega; C_L = 10\text{ pF}$		13		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		200		kHz
Phase Margin	$\Phi_M$	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		60		Degrees
Channel Separation	CS	$f = 10\text{ kHz}; R_L = 1\text{ M}\Omega$		105		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		5		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		50		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		45		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

**ELECTRICAL CHARACTERISTICS—18 V OPERATION**

$V_{SY} = 18\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

**Table 4.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to }18\text{ V}$			3	mV
		$V_{CM} = 0.3\text{ V to }17.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			4.5	mV
		$V_{CM} = 0\text{ V to }18\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			5	mV
		$V_{CM} = 0.3\text{ V to }17.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			11	mV
		$V_{CM} = 0\text{ V to }18\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			14	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	20	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.9	nA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }18\text{ V}$	80	95		dB
		$V_{CM} = 0.3\text{ V to }17.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	77			dB
		$V_{CM} = 0\text{ V to }18\text{ V}; -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	72			dB
		$V_{CM} = 0.3\text{ V to }17.7\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	65			dB
		$V_{CM} = 0\text{ V to }18\text{ V}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	63			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega; V_O = 0.5\text{ V to }17.5\text{ V}$	88	100		dB
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	82			dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	73			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		$\mu\text{V}/^\circ\text{C}$
Input Resistance	$R_{IN}$			10		G $\Omega$
Input Capacitance						
Differential Mode	$C_{INDM}$			3.5		pF
Common Mode	$C_{INCM}$			10.5		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega\text{ to }V_{CM}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	17.97			V
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega\text{ to }V_{CM}; -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			30	mV
Short-Circuit Current	$I_{SC}$			$\pm 12$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}; A_V = +1$		15		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to }18\text{ V}$	90	120		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	70			dB
Supply Current per Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$		18	22	$\mu\text{A}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			33	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		70		V/ms
Settling Time to 0.1%	$t_S$	$V_{IN} = 1\text{ V step}; R_L = 100\text{ k}\Omega; C_L = 10\text{ pF}$		12		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		200		kHz
Phase Margin	$\Phi_M$	$R_L = 1\text{ M}\Omega; C_L = 10\text{ pF}; A_V = +1$		60		Degrees
Channel Separation	CS	$f = 10\text{ kHz}; R_L = 1\text{ M}\Omega$		105		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		5		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		50		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		45		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage	(V <sub>-</sub> ) – 300 mV to (V <sub>+</sub> ) + 300 mV
Input Current <sup>1</sup>	±10 mA
Differential Input Voltage	±V <sub>SY</sub>
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

<sup>1</sup> The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer board.

Table 6. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead MSOP (RM-8)	142	45	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = 25°C, unless otherwise noted.

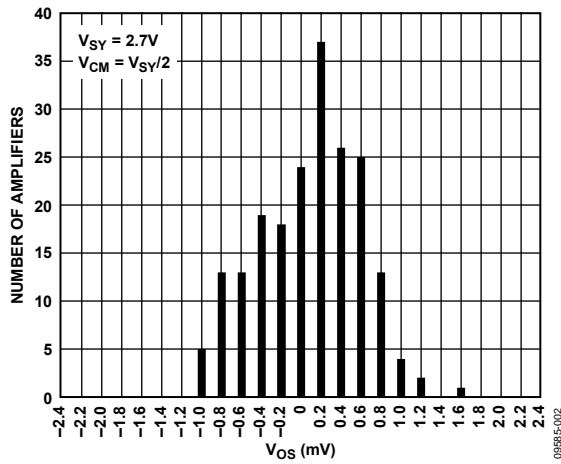


Figure 2. Input Offset Voltage Distribution

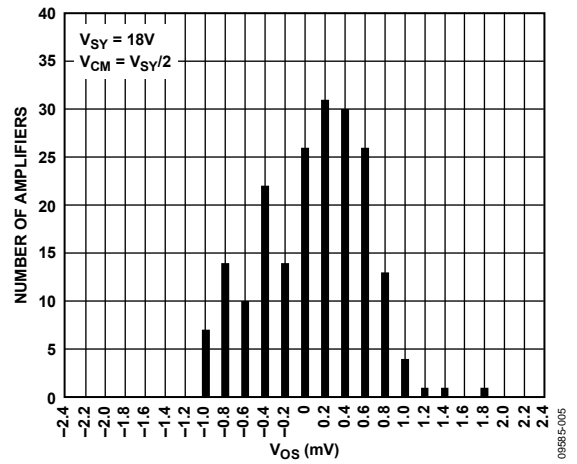


Figure 5. Input Offset Voltage Distribution

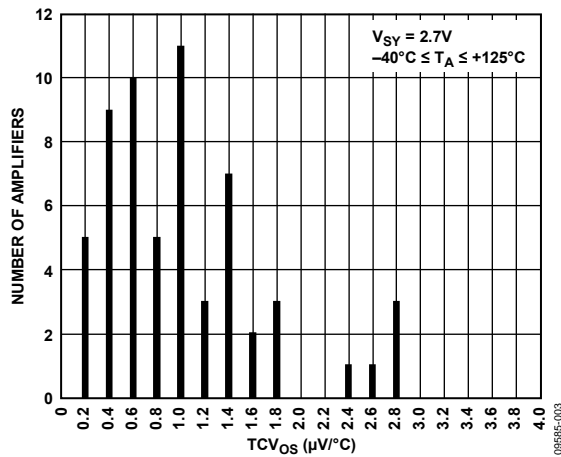


Figure 3. Input Offset Voltage Drift Distribution

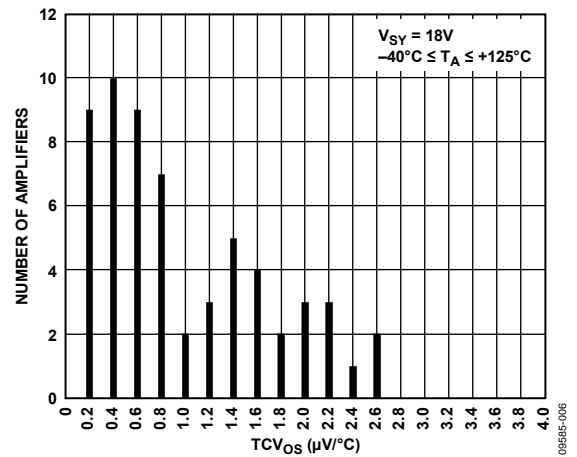


Figure 6. Input Offset Voltage Drift Distribution

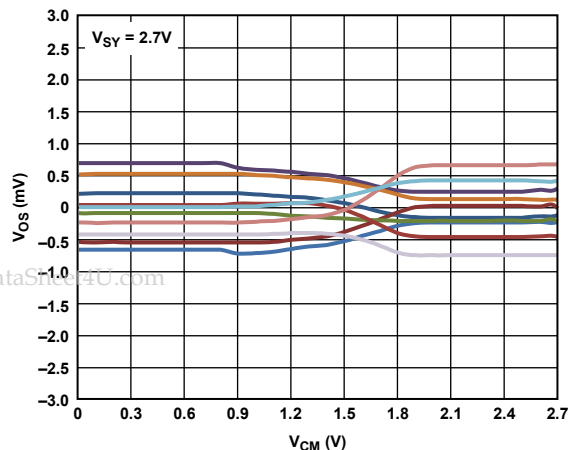


Figure 4. Input Offset Voltage vs. Common-Mode Voltage

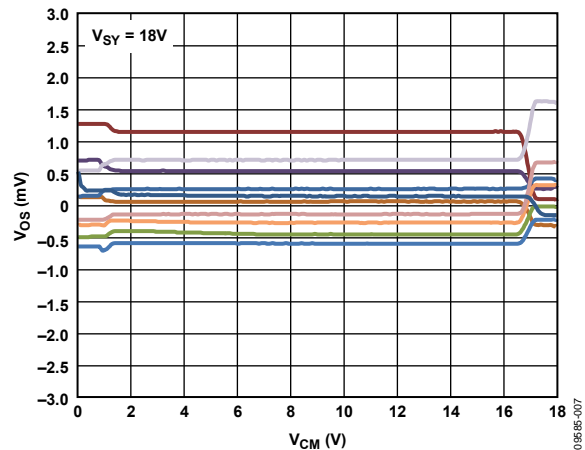


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

# AD8546

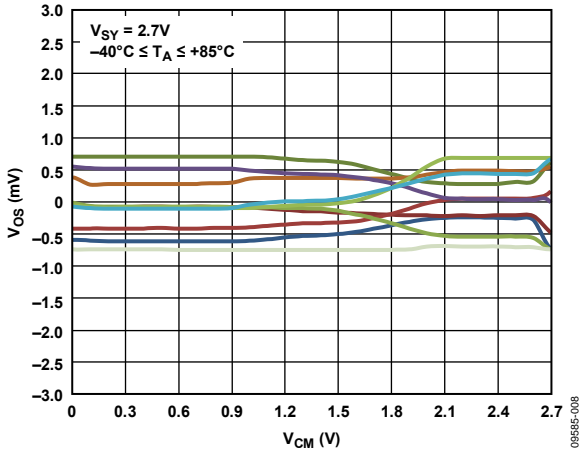


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

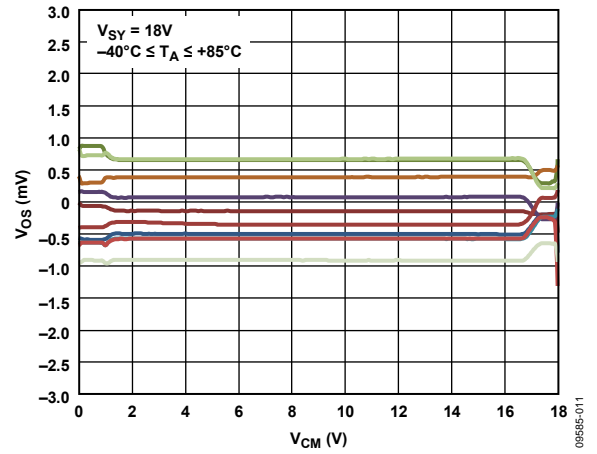


Figure 11. Input Offset Voltage vs. Common-Mode Voltage

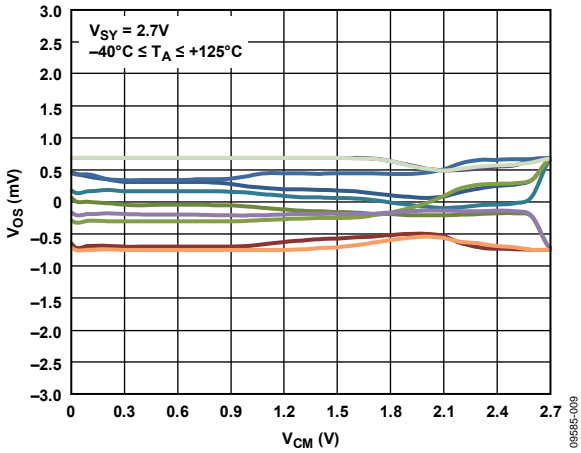


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

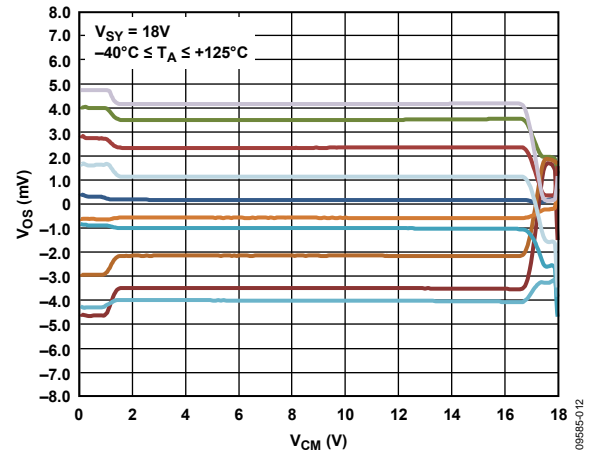


Figure 12. Input Offset Voltage vs. Common-Mode Voltage

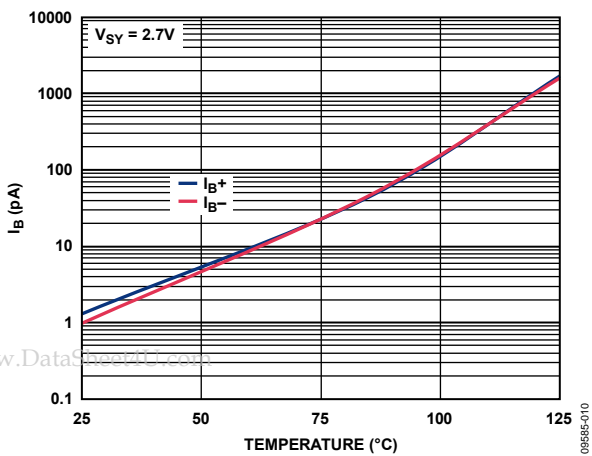


Figure 10. Input Bias Current vs. Temperature

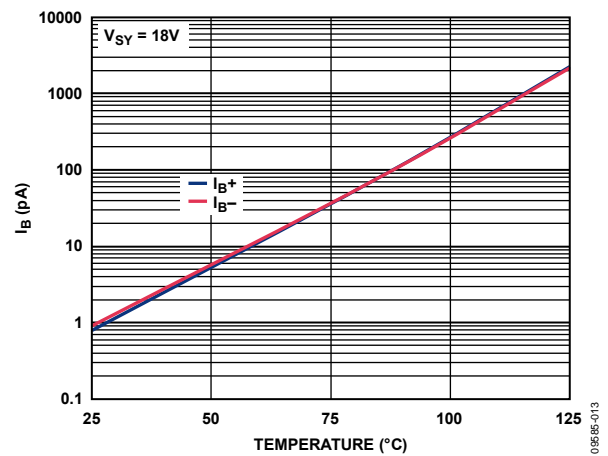


Figure 13. Input Bias Current vs. Temperature



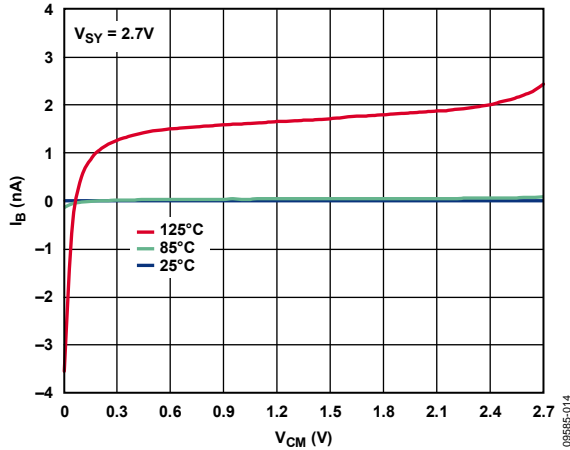


Figure 14. Input Bias Current vs. Common-Mode Voltage

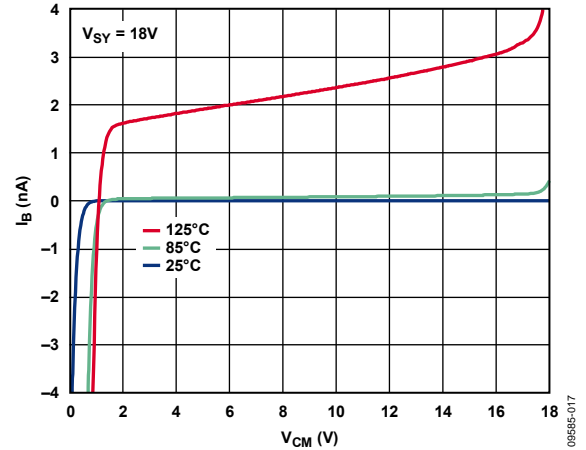


Figure 17. Input Bias Current vs. Common-Mode Voltage

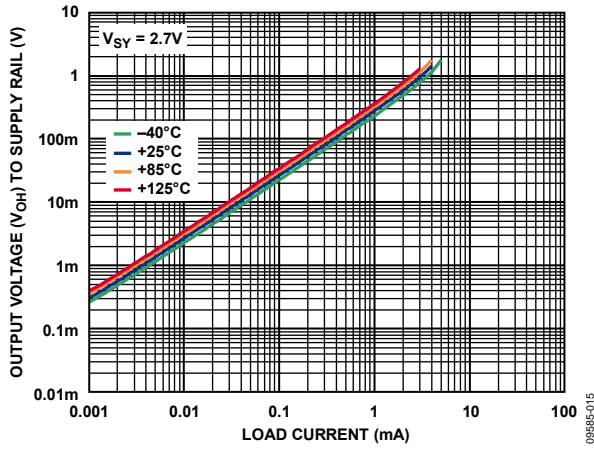


Figure 15. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Load Current

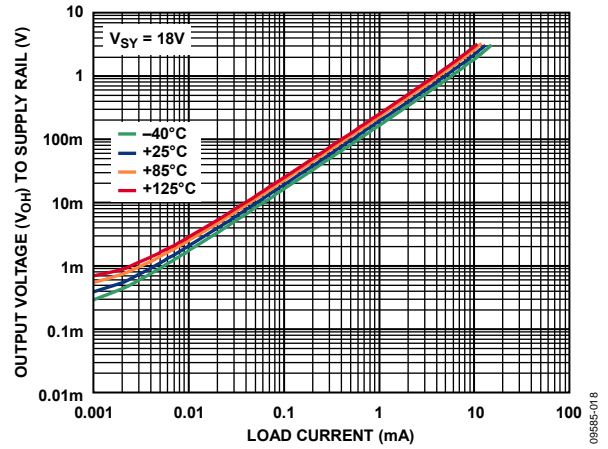


Figure 18. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Load Current

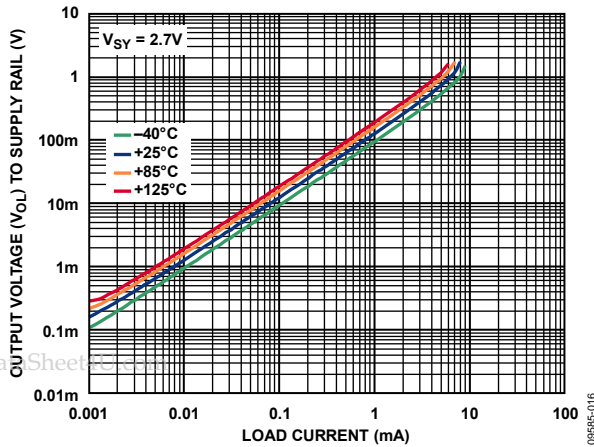


Figure 16. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Load Current

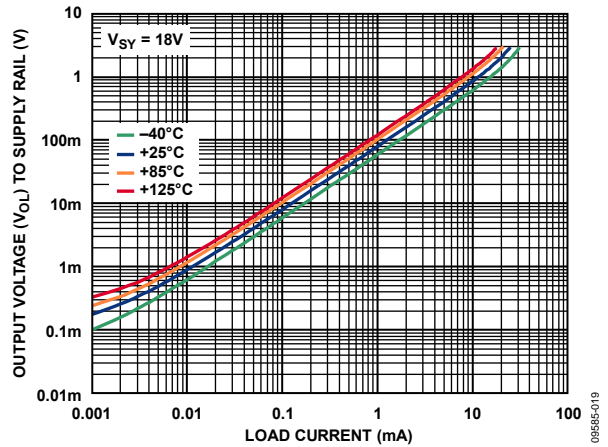


Figure 19. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Load Current

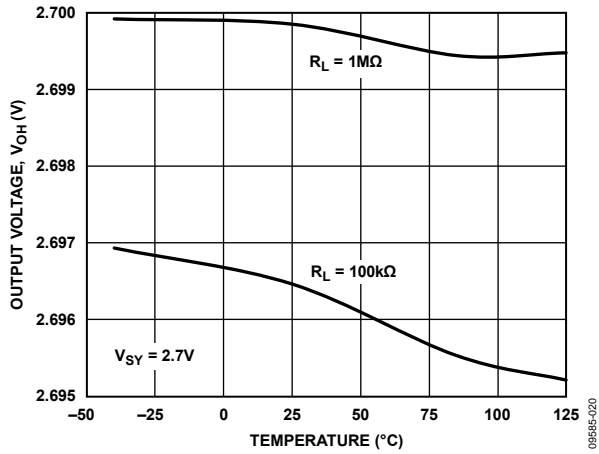


Figure 20. Output Voltage ( $V_{OH}$ ) vs. Temperature

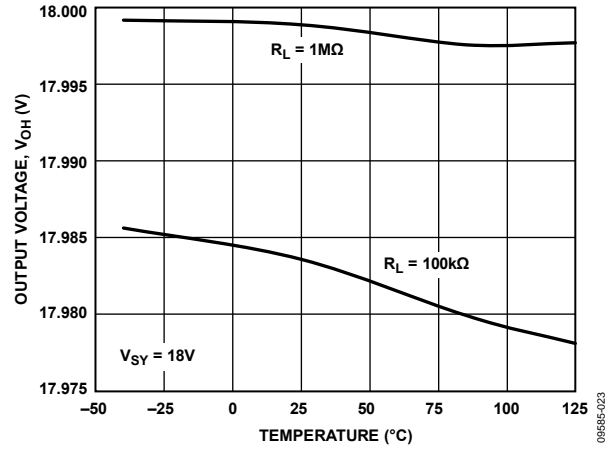


Figure 23. Output Voltage ( $V_{OH}$ ) vs. Temperature

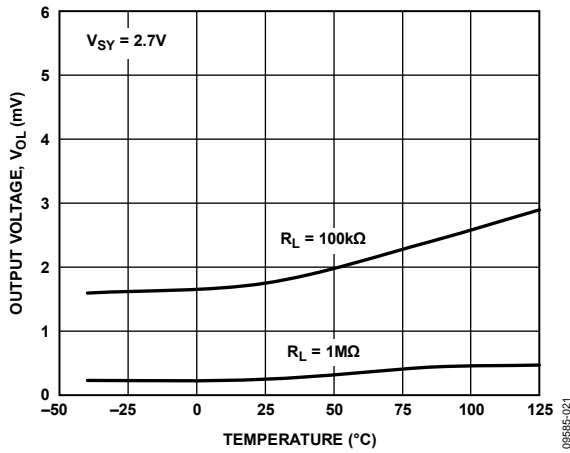


Figure 21. Output Voltage ( $V_{OL}$ ) vs. Temperature

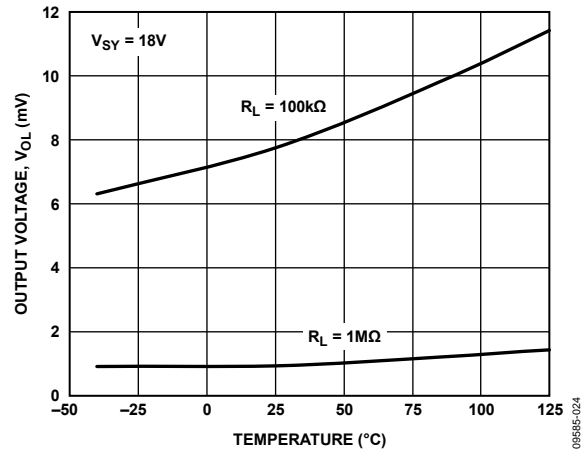


Figure 24. Output Voltage ( $V_{OL}$ ) vs. Temperature

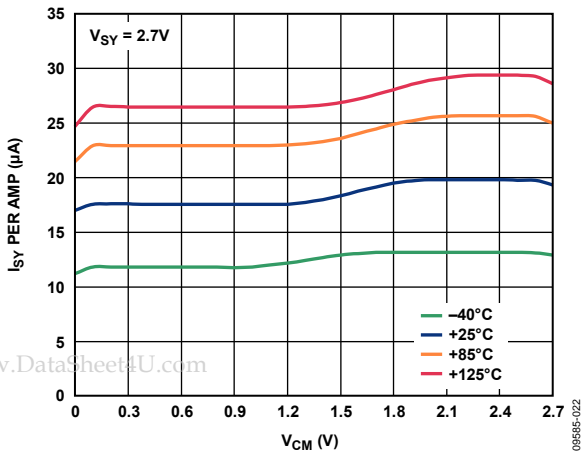


Figure 22. Supply Current per Amplifier vs. Common-Mode Voltage

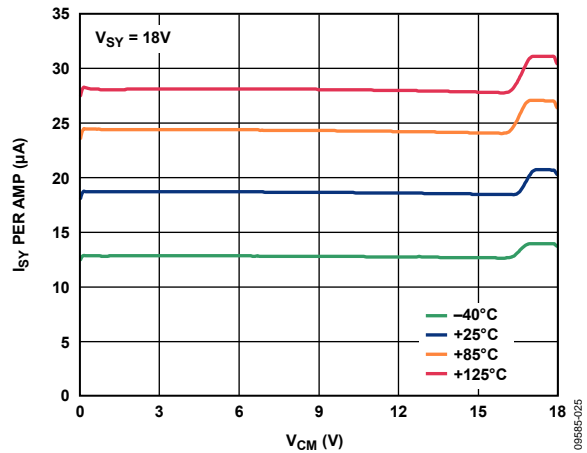


Figure 25. Supply Current per Amplifier vs. Common-Mode Voltage

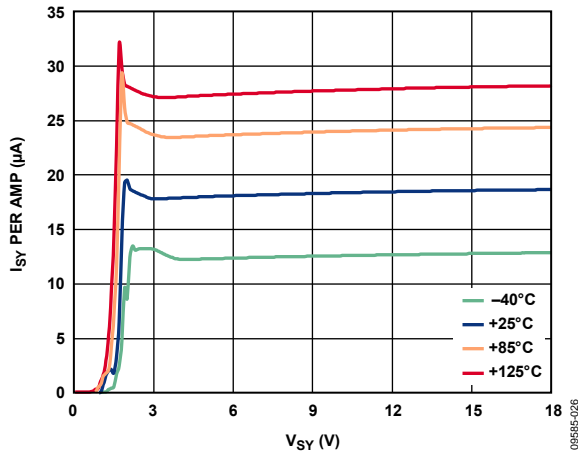


Figure 26. Supply Current per Amplifier vs. Supply Voltage

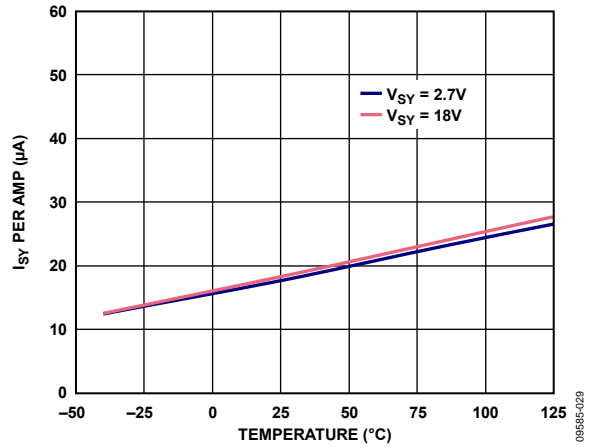


Figure 29. Supply Current per Amplifier vs. Temperature

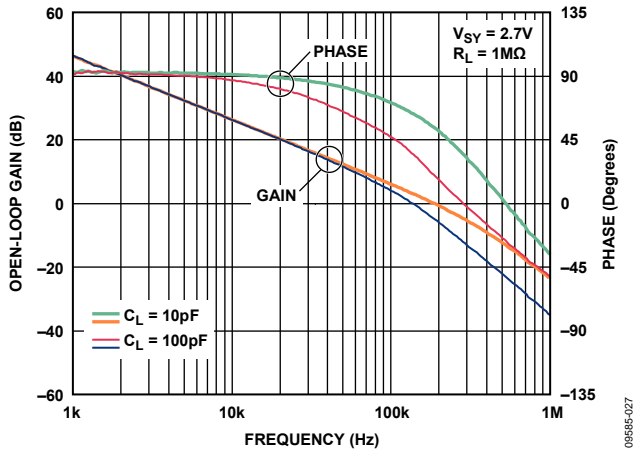


Figure 27. Open-Loop Gain and Phase vs. Frequency

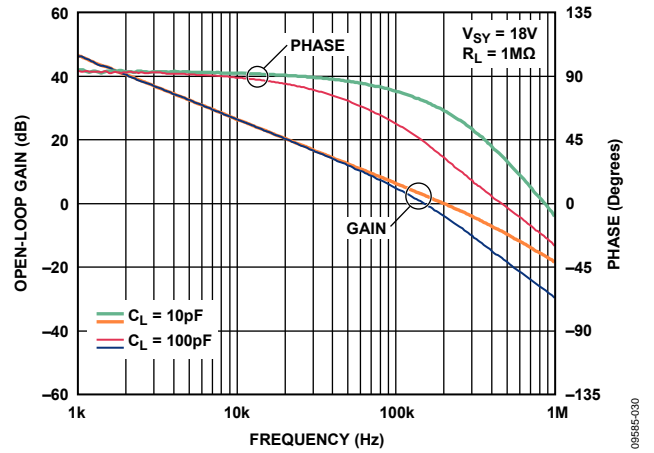


Figure 30. Open-Loop Gain and Phase vs. Frequency

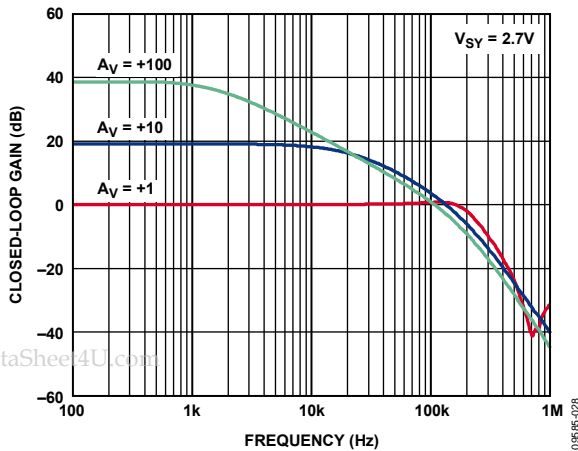


Figure 28. Closed-Loop Gain vs. Frequency

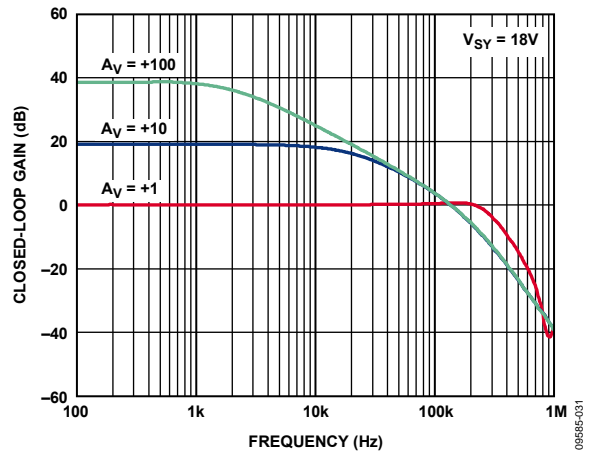


Figure 31. Closed-Loop Gain vs. Frequency

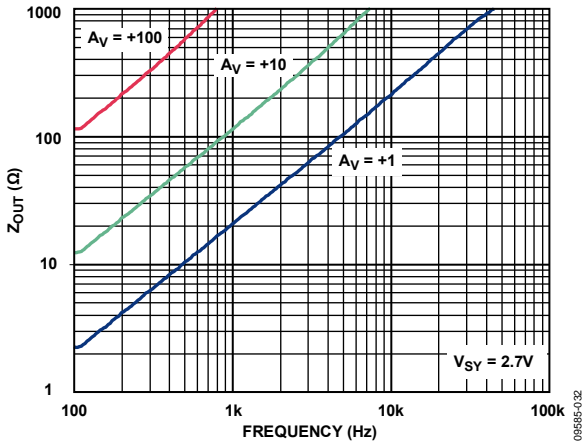


Figure 32. Output Impedance vs. Frequency

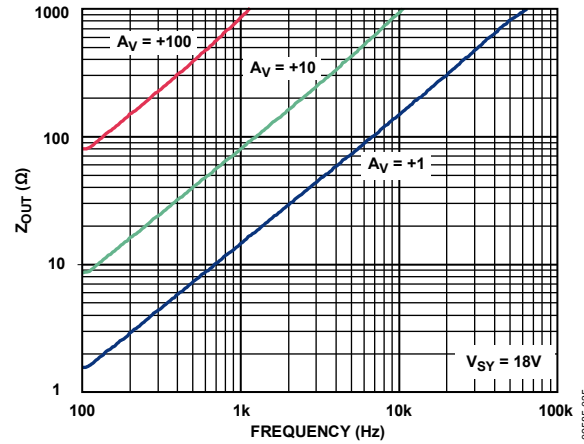


Figure 35. Output Impedance vs. Frequency

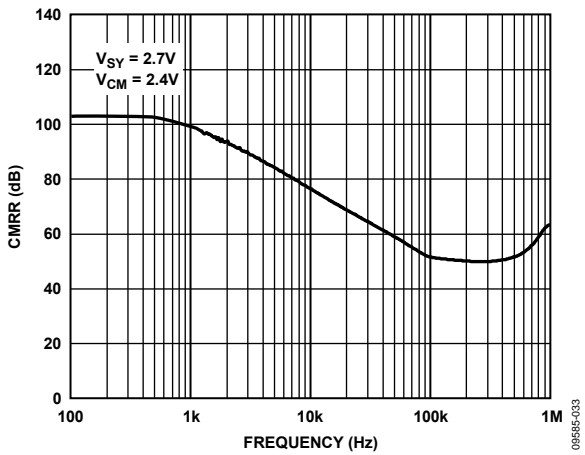


Figure 33. CMRR vs. Frequency

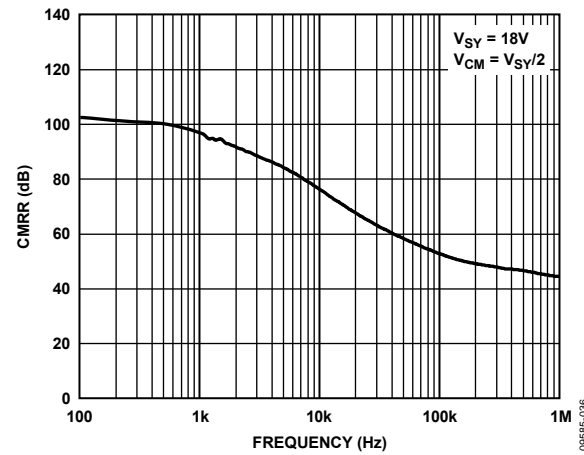


Figure 36. CMRR vs. Frequency

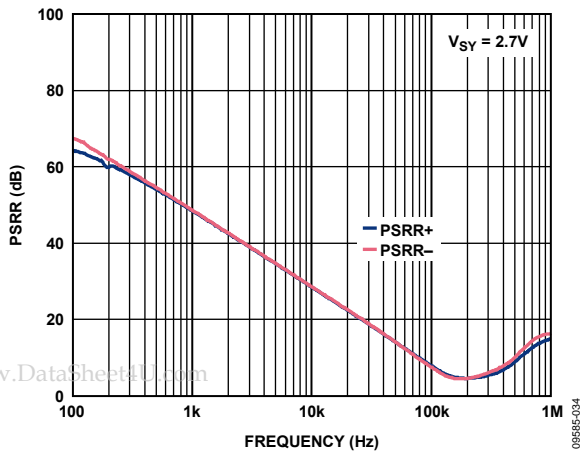


Figure 34. PSRR vs. Frequency

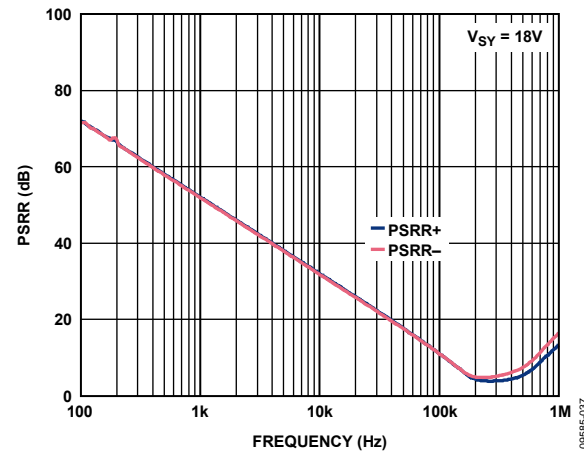


Figure 37. PSRR vs. Frequency

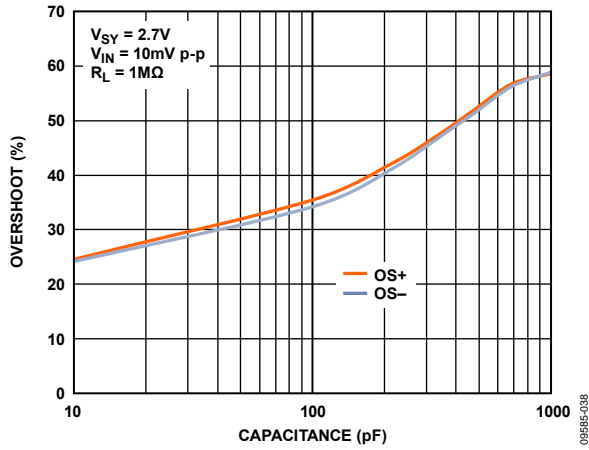


Figure 38. Small Signal Overshoot vs. Load Capacitance

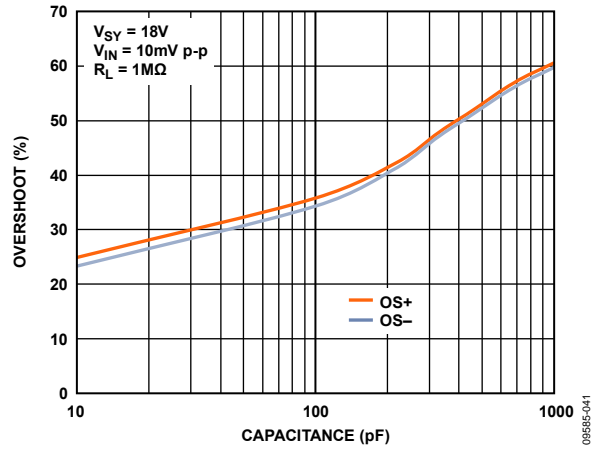


Figure 41. Small Signal Overshoot vs. Load Capacitance

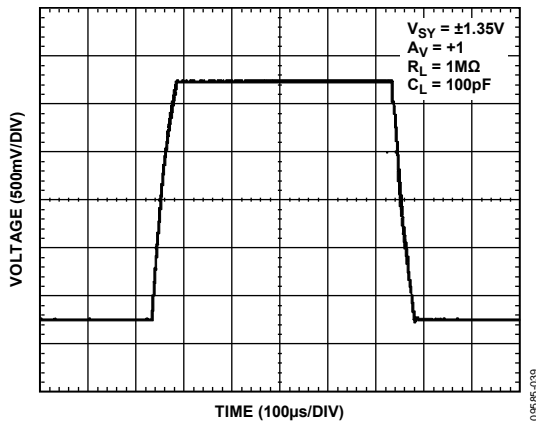


Figure 39. Large Signal Transient Response

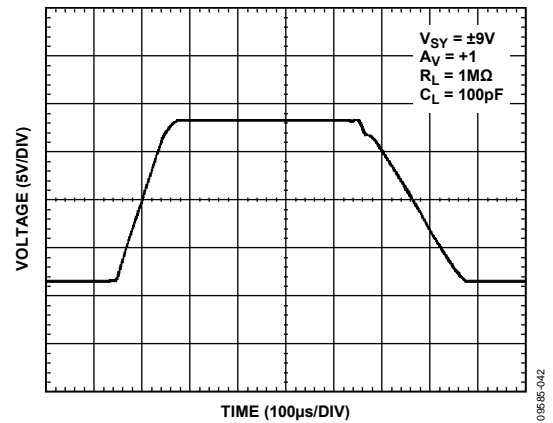


Figure 42. Large Signal Transient Response

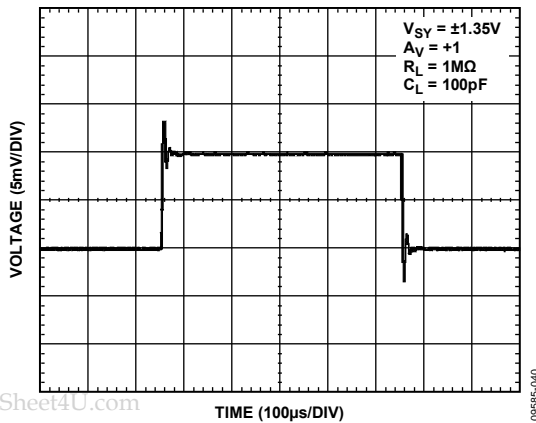


Figure 40. Small Signal Transient Response

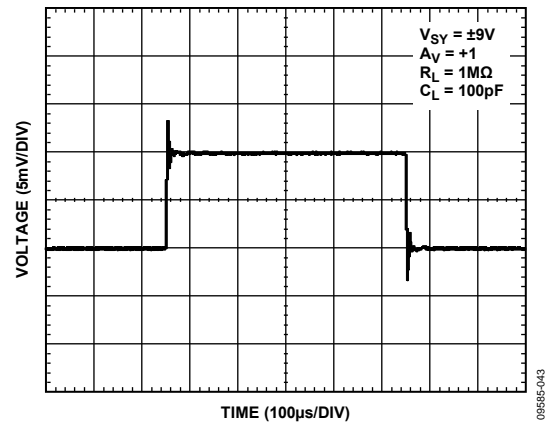


Figure 43. Small Signal Transient Response

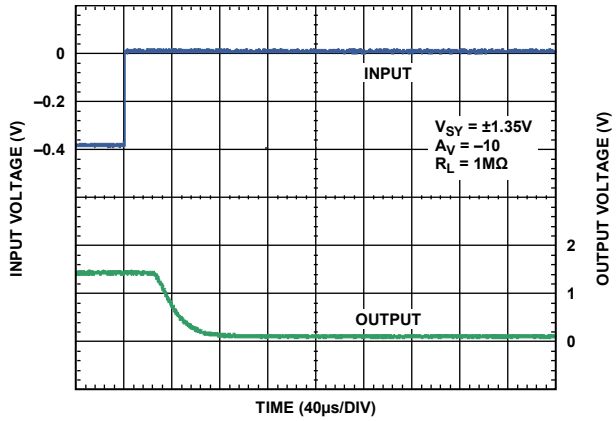


Figure 44. Positive Overload Recovery

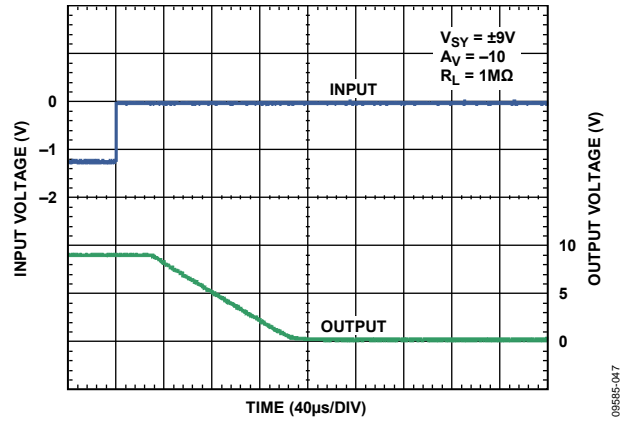


Figure 47. Positive Overload Recovery

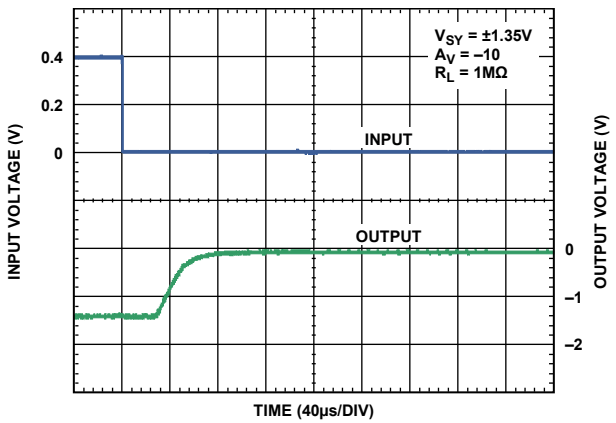


Figure 45. Negative Overload Recovery

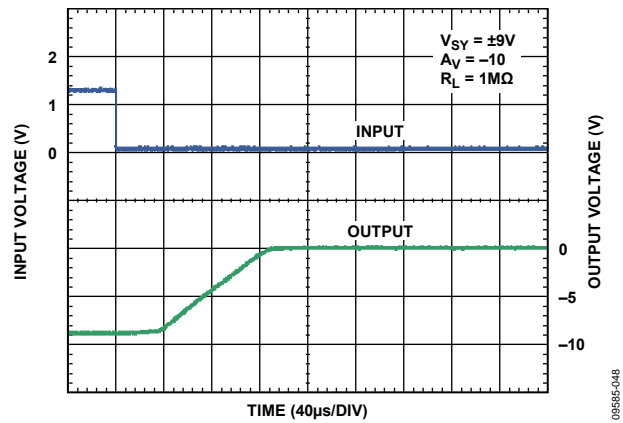


Figure 48. Negative Overload Recovery

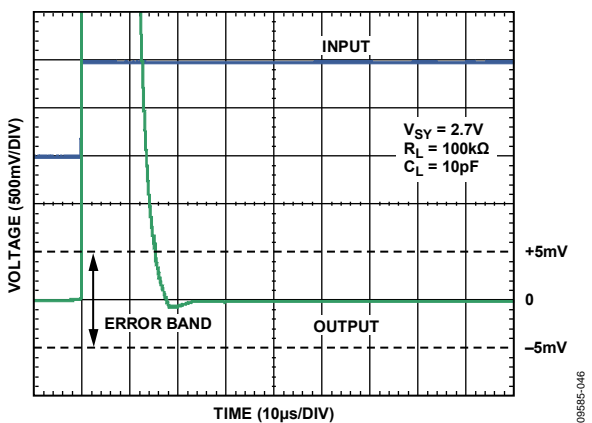


Figure 46. Positive Settling Time to 0.1%

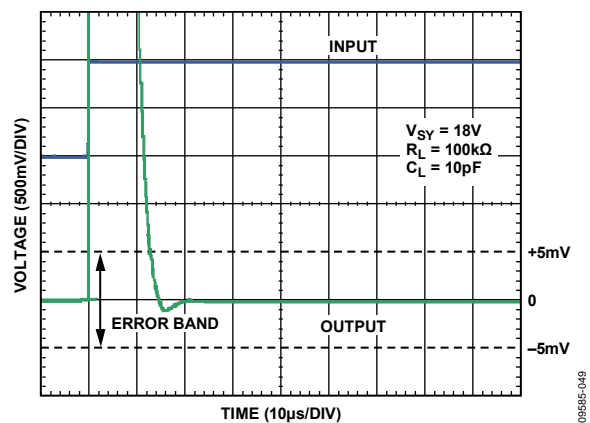


Figure 49. Positive Settling Time to 0.1%

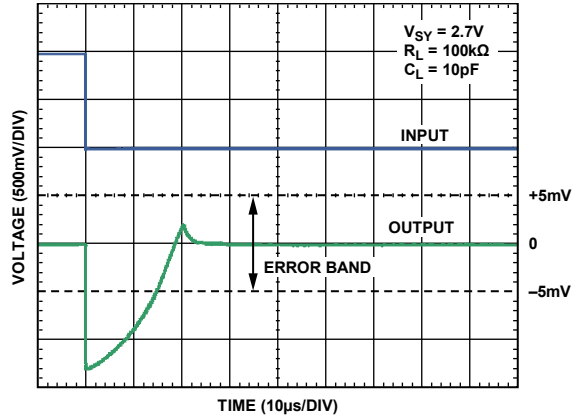


Figure 50. Negative Settling Time to 0.1%

09885-060

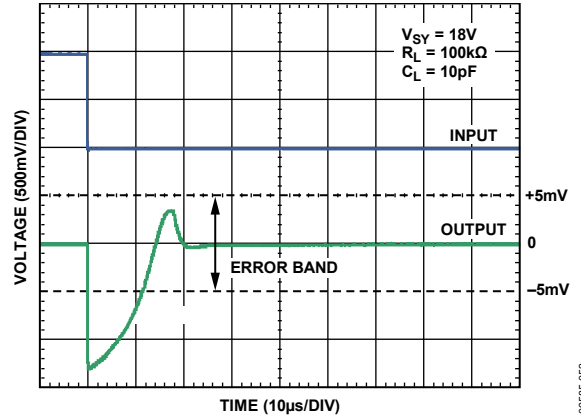


Figure 53. Negative Settling Time to 0.1%

09885-063

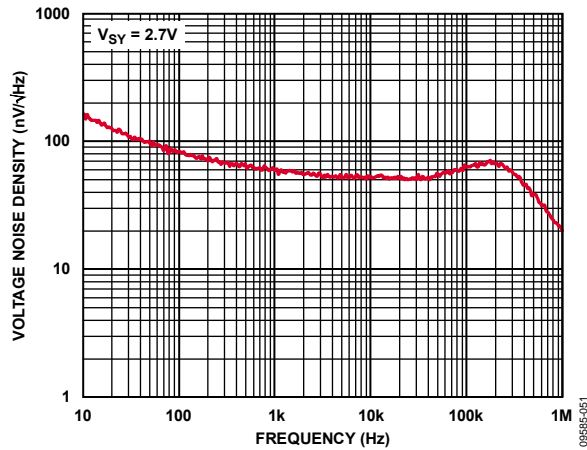


Figure 51. Voltage Noise Density vs. Frequency

09885-051

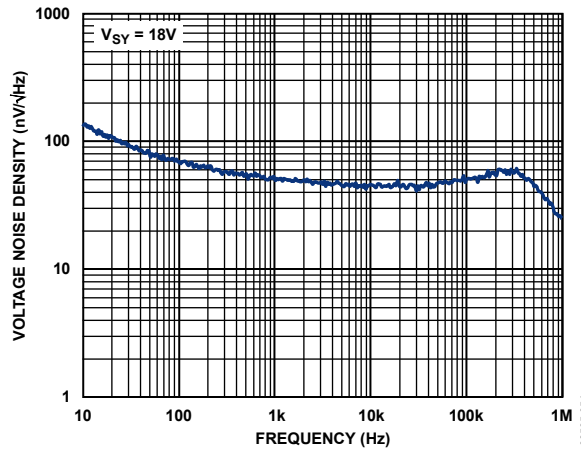


Figure 54. Voltage Noise Density vs. Frequency

09885-054

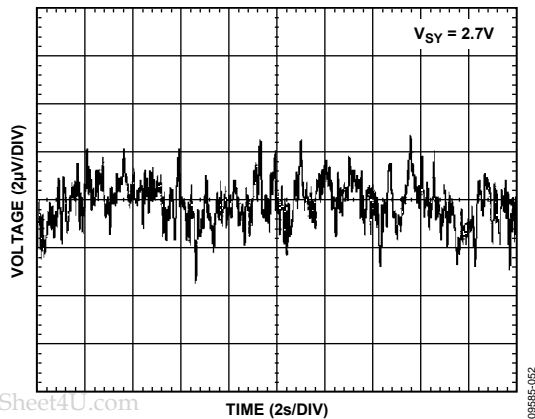


Figure 52. 0.1 Hz to 10 Hz Noise

09885-052

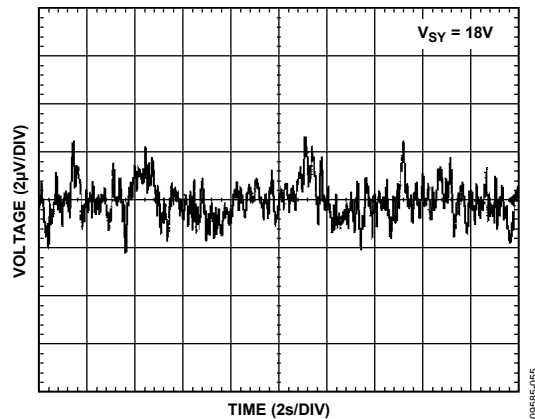


Figure 55. 0.1 Hz to 10 Hz Noise

09885-055

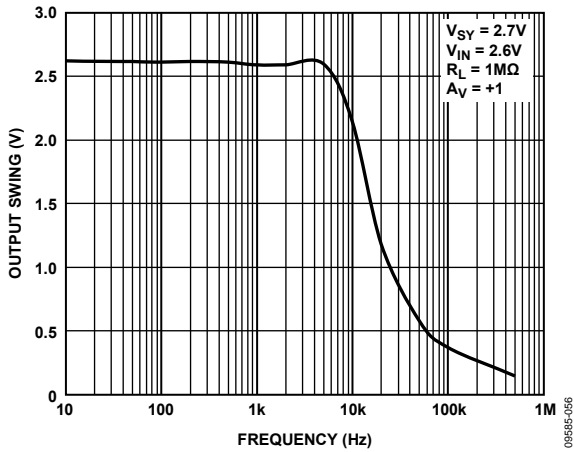


Figure 56. Output Swing vs. Frequency

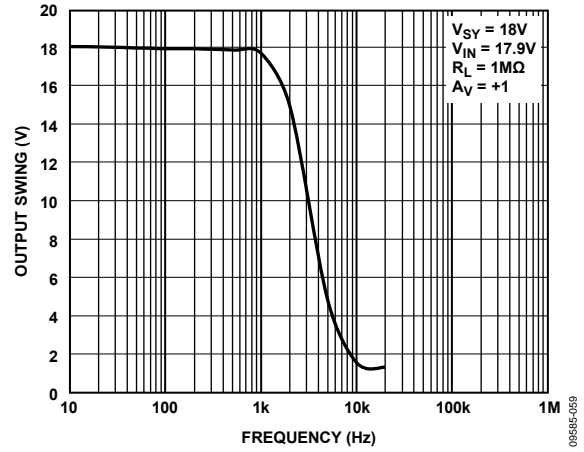


Figure 59. Output Swing vs. Frequency

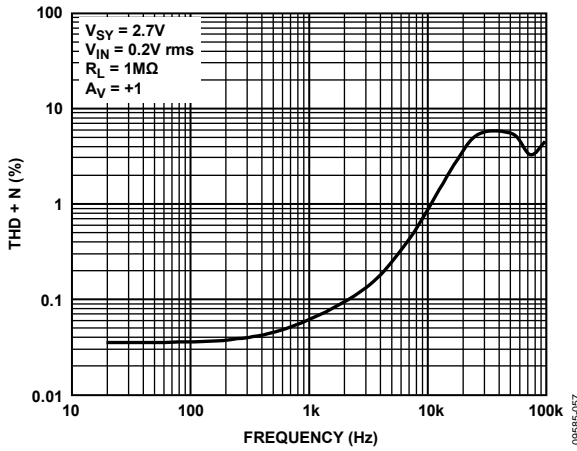


Figure 57. THD + N vs. Frequency

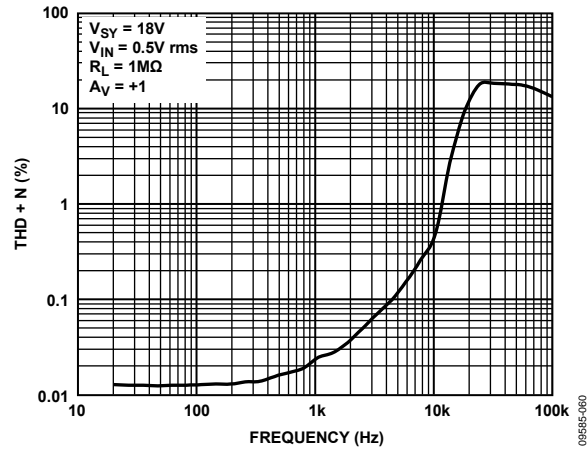


Figure 60. THD + N vs. Frequency

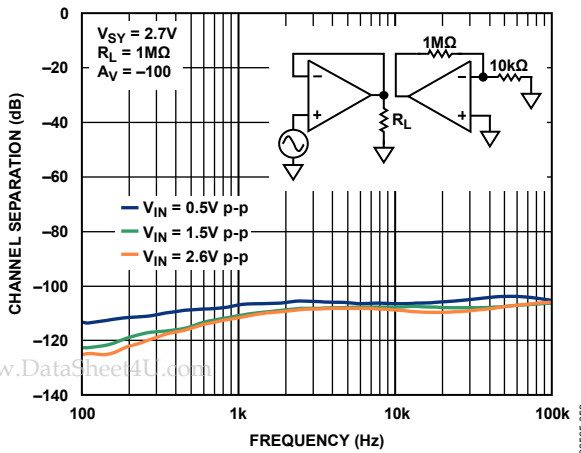


Figure 58. Channel Separation vs. Frequency

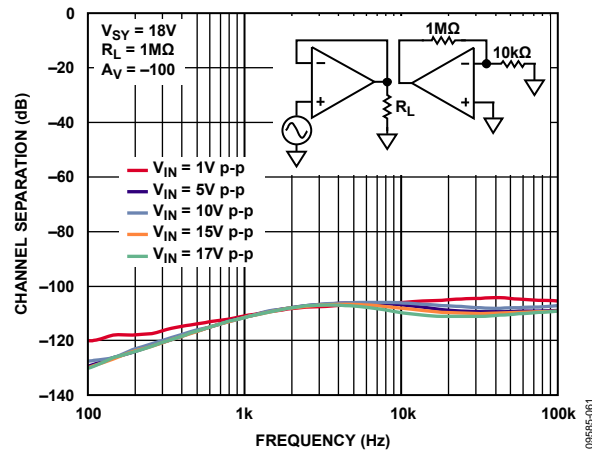


Figure 61. Channel Separation vs. Frequency



## APPLICATIONS INFORMATION

The AD8546 is a low input bias current, micropower CMOS amplifier that operates over a wide supply voltage range of 2.7 V to 18 V. The AD8546 also employs unique input and output stages to achieve a rail-to-rail input and output range with a very low supply current.

### INPUT STAGE

Figure 62 shows the simplified schematic of the AD8546. The input stage comprises two differential transistor pairs, an NMOS pair (M1, M2) and a PMOS pair (M3, M4). The input common-mode voltage determines which differential pair turns on and is more active than the other.

The PMOS differential pair is active when the input voltage approaches and reaches the lower supply rail. The NMOS pair is needed for input voltages up to and including the upper supply rail. This topology allows the amplifier to maintain a wide dynamic input voltage range and maximize signal swing to both supply rails.

For the majority of the input common-mode voltage range, the PMOS differential pair is active. Differential pairs commonly exhibit different offset voltages. The handoff from one pair to the other creates a step-like characteristic that is visible in the  $V_{OS}$  vs.  $V_{CM}$  graphs (see Figure 4 and Figure 7). This characteristic is inherent in all rail-to-rail amplifiers that use the dual differential pair topology. Therefore, always choose a common-mode voltage that does not include the region of handoff from one input differential pair to the other.

Additional steps in the  $V_{OS}$  vs.  $V_{CM}$  curves are also visible as the input common-mode voltage approaches the power supply rails. These changes are a result of the load transistors (M8, M9, M14, and M15) running out of headroom. As the load transistors are forced into the triode region of operation, the mismatch of their

drain impedances contributes to the offset voltage of the amplifier. This problem is exacerbated at high temperatures due to the decrease in the threshold voltage of the input transistors. Refer to Figure 8, Figure 9, Figure 11, and Figure 12 for typical performance data.

Current Source I1 drives the PMOS transistor pair. As the input common-mode voltage approaches the upper rail, I1 is steered away from the PMOS differential pair through the M5 transistor. The bias voltage, VB1, controls the point where this transfer occurs.

M5 diverts the tail current into a current mirror consisting of the M6 and M7 transistors. The output of the current mirror then drives the NMOS transistor pair. Note that the activation of this current mirror causes a slight increase in supply current at high common-mode voltages (see Figure 22 and Figure 25).

The AD8546 achieves its high performance by using low voltage MOS devices for its differential inputs. These low voltage MOS devices offer excellent noise and bandwidth per unit of current. Each differential input pair is protected by proprietary regulation circuitry (not shown in the simplified schematic). The regulation circuitry consists of a combination of active devices that maintain the proper voltages across the input pairs during normal operation and passive clamping devices that protect the amplifier during fast transients. However, these passive clamping devices begin to forward-bias as the common-mode voltage approaches either power supply rail. This causes an increase in the input bias current (see Figure 14 and Figure 17).

The input devices are also protected from large differential input voltages by clamp diodes (D1 and D2). These diodes are buffered from the inputs with two 10 k $\Omega$  resistors (R1 and R2). The differential diodes turn on whenever the differential voltage exceeds approximately 600 mV; in this condition, the differential input resistance drops to 20 k $\Omega$ .

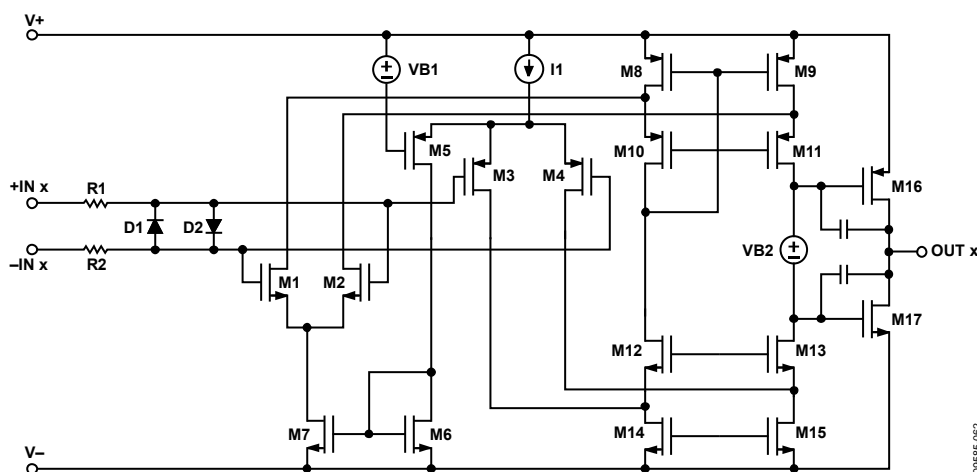


Figure 62. Simplified Schematic

# AD8546

## OUTPUT STAGE

The AD8546 features a complementary output stage consisting of the M16 and M17 transistors (see Figure 62). These transistors are configured in Class AB topology and are biased by the voltage source, VB2. This topology allows the output voltage to go within millivolts of the supply rails, achieving a rail-to-rail output swing. The output voltage is limited by the output impedance of the transistors, which are low  $R_{ON}$  MOS devices. The output voltage swing is a function of the load current and can be estimated using the output voltage to supply rail vs. load current diagrams (see Figure 15, Figure 16, Figure 18, and Figure 19).

## RAIL-TO-RAIL INPUT AND OUTPUT

The AD8546 features rail-to-rail input and output with a supply voltage from 2.7 V to 18 V. Figure 63 shows the input and output waveforms of the AD8546 configured as a unity-gain buffer with a supply voltage of  $\pm 9$  V and a resistive load of 1 M $\Omega$ . With an input voltage of  $\pm 9$  V, the AD8546 allows the output to swing very close to both rails. Additionally, it does not exhibit phase reversal.

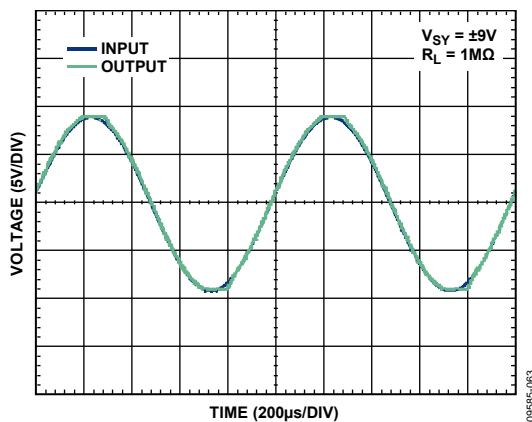


Figure 63. Rail-to-Rail Input and Output

## RESISTIVE LOAD

The feedback resistor alters the load resistance that an amplifier sees. It is, therefore, important to be aware of the value of the feedback resistors selected for use with the AD8546. The AD8546 is capable of driving resistive loads down to 100 k $\Omega$ . The following two examples, inverting and noninverting configurations, show how the feedback resistor changes the actual load resistance seen at the output of the amplifier.

### Inverting Configuration

Figure 64 shows the AD8546 in an inverting configuration with a resistive load,  $R_L$ , at the output. The actual load seen by the amplifier is the parallel combination of the feedback resistor,  $R_2$ , and the load,  $R_L$ . The combination of a feedback resistor of 1 k $\Omega$  and a load of 1 M $\Omega$  results in an equivalent load resistance of 999  $\Omega$  at the output. In this condition, the AD8546 is incapable of driving such a heavy load; therefore, its performance degrades greatly.

To avoid loading the output, use a larger feedback resistor, but consider the effect of resistor thermal noise on the overall circuit.

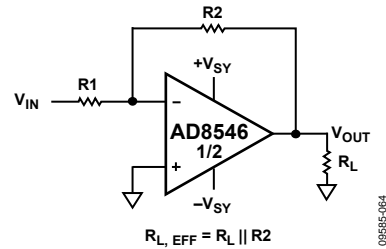


Figure 64. Inverting Op Amp Configuration

### Noninverting Configuration

Figure 65 shows the AD8546 in a noninverting configuration with a resistive load,  $R_L$ , at the output. The actual load seen by the amplifier is the parallel combination of  $R_1 + R_2$  and  $R_L$ .

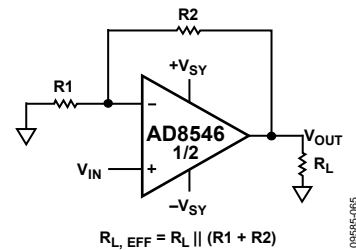


Figure 65. Noninverting Op Amp Configuration

## COMPARATOR OPERATION

An op amp is designed to operate in a closed-loop configuration with feedback from its output to its inverting input. Figure 66 shows the AD8546 configured as a voltage follower with an input voltage that is always kept at midpoint of the power supplies. The same configuration is applied to the unused channel. A1 and A2 indicate the placement of ammeters to measure supply current.  $I_{SY+}$  refers to the current flowing from the upper supply rail to the op amp, and  $I_{SY-}$  refers to the current flowing from the op amp to the lower supply rail. As expected, Figure 67 shows that in normal operating condition, the total current flowing into the op amp is equivalent to the total current flowing out of the op amp, where  $I_{SY+} = I_{SY-} = 36 \mu A$  for the dual AD8546 at  $V_{SY} = 18$  V.

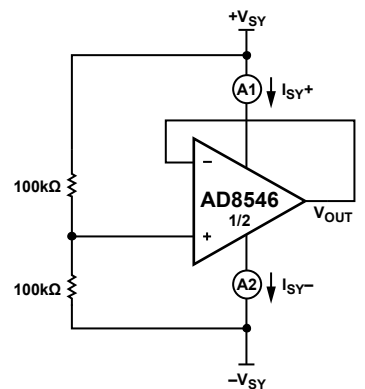


Figure 66. Voltage Follower Configuration

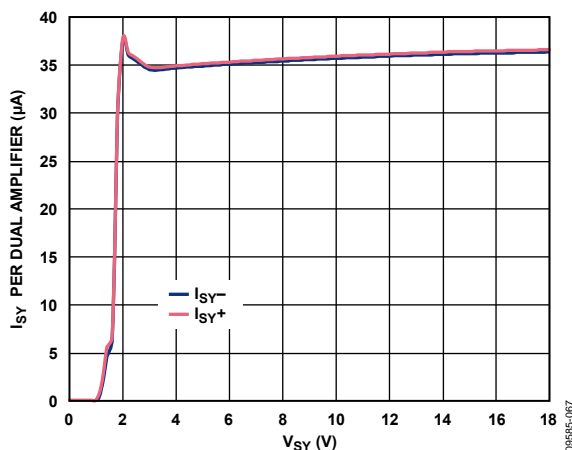


Figure 67. Supply Current vs. Supply Voltage (Voltage Follower)

In contrast to op amps, comparators are designed to work in an open-loop configuration and to drive logic circuits. Although op amps are different from comparators, occasionally an unused section of a dual op amp is used as a comparator to save board space and cost; however, this is not recommended.

Figure 68 and Figure 69 show the AD8546 configured as a comparator, with 100 k $\Omega$  resistors in series with the input pins. Any unused channels are configured as buffers with the input voltage kept at the midpoint of the power supplies.

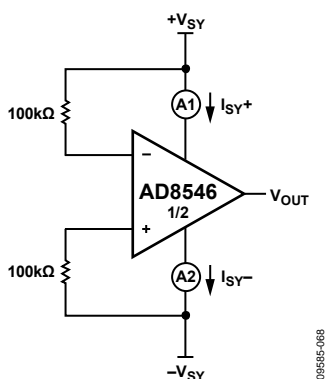


Figure 68. Comparator A

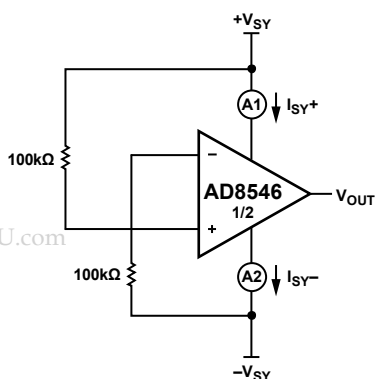


Figure 69. Comparator B

The AD8546 has input devices that are protected from large differential input voltages by Diode D1 and Diode D2 (see Figure 62). These diodes consist of substrate PNP bipolar transistors and conduct whenever the differential input voltage exceeds approximately 600 mV; however, these diodes also allow a current path from the input to the lower supply rail, thus resulting in an increase in the total supply current of the system. As shown in Figure 70, both configurations yield the same result. At 18 V of power supply,  $I_{SY+}$  remains at 36  $\mu$ A per dual amplifier, but  $I_{SY-}$  increases to 140  $\mu$ A in magnitude per dual amplifier.

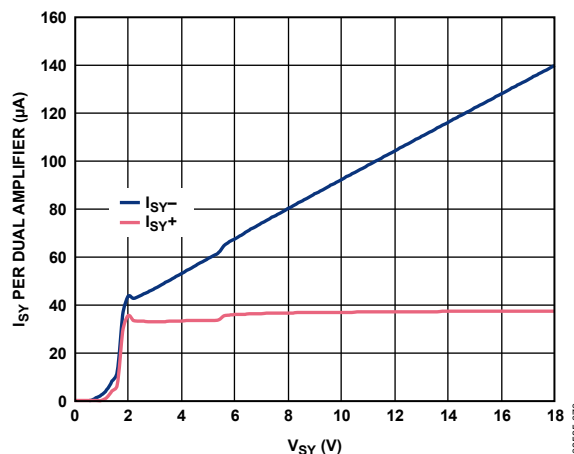


Figure 70. Supply Current vs. Supply Voltage (AD8546 as a Comparator)

Note that 100 k $\Omega$  resistors are used in series with the input of the op amp. If smaller resistor values are used, the supply current of the system increases much more. For more information about using op amps as comparators, see the [AN-849](#) Application Note, *Using Op Amps as Comparators*.

#### 4 mA TO 20 mA PROCESS CONTROL CURRENT LOOP TRANSMITTER

A 2-wire current transmitter is often used in distributed control systems and process control applications to transmit analog signals between sensors and process controllers. Figure 71 shows a 4 mA to 20 mA current loop transmitter.

The transmitter is powered directly from the control loop power supply, and the current in the loop carries signal from 4 mA to 20 mA. Thus, 4 mA establishes the baseline current budget within which the circuit must operate.

The AD8546 is an excellent choice due to its low supply current of 33  $\mu$ A per amplifier over temperature and supply voltage. The current transmitter controls the current flowing in the loop, where a zero-scale input signal is represented by 4 mA of current and a full-scale input signal is represented by 20 mA. The transmitter also floats from the control loop power supply,  $V_{DD}$ , whereas signal ground is in the receiver. The loop current is measured at the load resistor,  $R_L$ , at the receiver side.

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With a zero-scale input, a current of  $V_{REF}/R_{NULL}$  flows through  $R'$ . This creates a current flowing through the sense resistor,  $I_{SENSE}$ , determined by the following equation:

$$I_{SENSE, MIN} = (V_{REF} \times R') / (R_{NULL} \times R_{SENSE})$$

With a full-scale input voltage, current flowing through  $R'$  is increased by the full-scale change in  $V_{IN}/R_{SPAN}$ . This creates an increase in the current flowing through the sense resistor.

$$I_{SENSE, DELTA} = (\text{Full-Scale Change in } V_{IN} \times R') / (R_{SPAN} \times R_{SENSE})$$

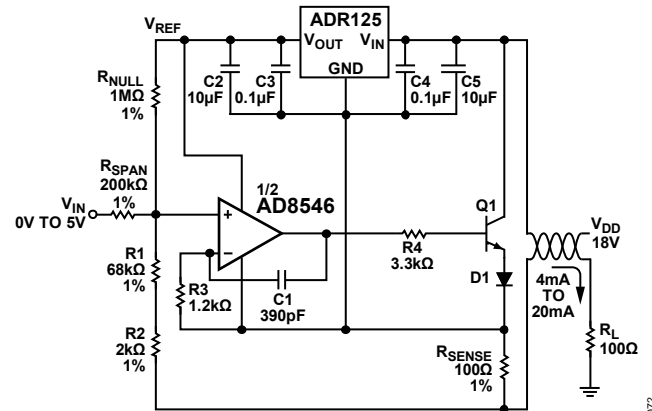
Therefore

$$I_{SENSE, MAX} = I_{SENSE, MIN} + I_{SENSE, DELTA}$$

When  $R' \gg R_{SENSE}$ , the current through the load resistor at the receiver side is almost equivalent to  $I_{SENSE}$ .

Figure 71 shows a design for a full-scale input voltage of 5 V. At 0 V of input, loop current is 3.5 mA, and at a full-scale input of 5 V, the loop current is 21 mA. This allows software calibration to fine-tune the current loop to the 4 mA to 20 mA range.

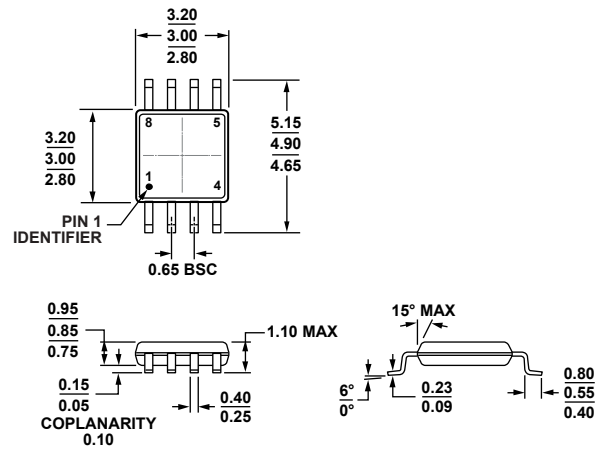
The AD8546 and ADR125 together consume only 160  $\mu$ A quiescent current, making 3.34 mA current available to power additional signal conditioning circuitry or to power a bridge circuit.



NOTES  
1.  $R1 + R2 = R'$ .

Figure 71. 4 mA to 20 mA Current Loop Transmitter

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 72. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2009-B

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
AD8546ARMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2V
AD8546ARMZ-RL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2V
AD8546ARMZ-R7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2V

<sup>1</sup> Z = RoHS Compliant Part.

**AD8546**

**NOTES**

**NOTES**

**AD8546**

**NOTES**

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