Gate Drive Characteristics and Requirements for HEXFET®s

Topics covered:

Gate drive vs base drive
Enhancement vs Depletion
N vs P-Channel
Max gate voltage
Zener diodes on gate?
The most important factor in gate drive: the impedance of the gate drive circuit
Switching 101 or Understanding the waveforms
What happens if gate drive impedance is high? dv/dt induced turn-on
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Related topics

(Note: Most of the gate drive considerations and circuits are equally applicable to IGBTs. Only MOSFETs are mentioned for the sake of simplicity. Special considerations for IGBTs are contained in INT-990)

1. GATE DRIVE VS BASE DRIVE

The conventional bipolar transistor is a current-driven device. As illustrated in Figure 1(a). a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of a drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

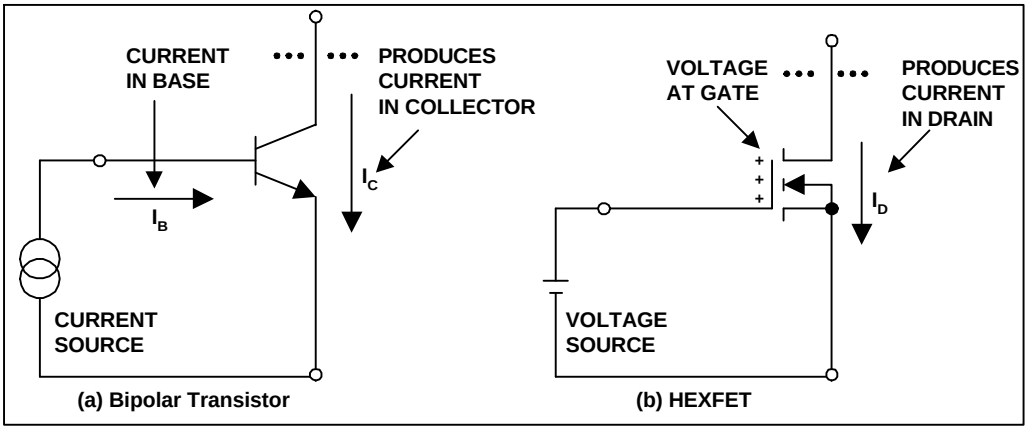

Figure 1. Bipolar Transistor is Current Driven, HEXFET is Voltage Driven

The HEXFET®is fundamentally different: it is a voltage-controlled power MOSFET device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain (see Figure 1b). The gate is isolated electrically from the source by a layer of silicon dioxide. Theoretically, therefore, no current flows into the gate when a DC voltage is applied to it - though in practice there will be an extremely small current, in the order of nanoamperes. With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only the leakage current flows in the drain.

When a voltage is applied between the gate and source terminals, an electric field is set up within the HEXFET®. This field "inverts" the channel (Figure 2) from P to N, so that a current can flow from drain to source in an uninterrupted sequence of N-type silicon (drain-channel-source). Field-effect transistors can be of two types: enhancement mode and depletion mode. Enhancement-mode devices need a gate voltage of the same sign as the drain voltage in order to pass current.

Depletion-mode devices are naturally on and are turned off by a gate voltage of the same polarity as the drain voltage. All HEXFET®s are enhancement-mode devices.

All MOSFET voltages are referenced to the source terminal. An N-Channel device, like an NPN transistor, has a drain voltage that is positive with respect to the source. Being enhancement-mode devices, they will be turned on by a positive voltage on the gate. The opposite is true for P-Channel devices, that are similar to PNP transistors.

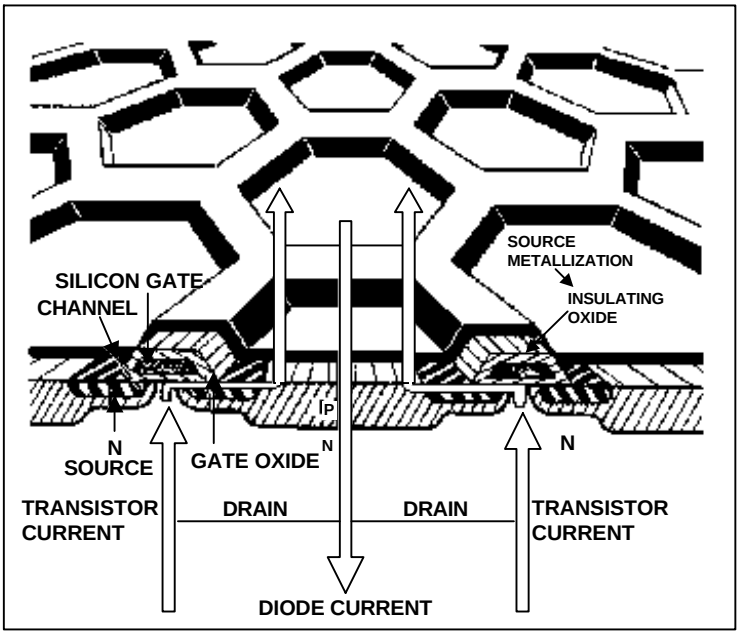

Figure 2. Basic HEXFET Structure

Although it is common knowledge that HEXFET®transistors are more easily driven than bipolars, a few basic considerations have to be kept in mind in order to avoid a loss in performance or outright device failure.

2. GATE VOLTAGE LIMITATIONS

Figure 2 shows the basic HEXFET®structure. The silicon oxide layer between the gate and the source regions can be punctured by exceeding its dielectric strength. The data sheet rating for the gate-to-source voltage is between 10 and 30 V for most HEXFET®s.

Care should be exercised not to exceed the gate-to-source maximum voltage rating. Even if the applied gate voltage is kept below the maximum rated gate voltage, the stray inductance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to the destruction of the oxide layer. Overvoltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. A gate drive circuit with very low impedance insures that the gate voltage is not exceeded in normal operation. This is explained in more detail in the next section.

Zeners are frequently used "to protect the gate from transients". Unfortunately they also contribute to oscillations and have been known to cause device failures. A transient can get to the gate from the drive side or from the drain side. In either case, it would be an indication of a more fundamental problem: a high impedance drive circuit. A zener would compound this problem, rather than solving it. Sometimes a zener is added to reduce the ringing generated by the leakage of a gate drive transformer, in combination with the input capacitance of the MOSFET. If this is necessary, it is advisable to insert a small series resistor (5-10 Ohms) between the zener and the gate, to prevent oscillations.

3. THE IMPEDANCE OF THE GATE CIRCUIT

To turn on a power MOSFET a certain charge has to be supplied to the gate to raise it to the desired voltage, whether in the linear region, or in the "saturation" (fully enhanced) region. The best way to achieve this is by means of a voltage source, capable of supplying any amount of current in the shortest possible time. If the device is operated as a switch, a large transient current capability of the drive circuit reduces the time spent in the linear region, thereby reducing the switching losses.

On the other hand, if the device is operated in the linear mode, a large current from the gate drive circuit minimizes the relevance of the Miller effect, improving the bandwidth of the stage and reducing the harmonic distortion. This can be better understood by analyzing the basic switching waveforms at turn-on and turn-off for a clamped inductive load, as shown in Figures

3 and 5. Figure 3 shows the waveforms of the drain current, drain-to-source voltage and gate voltage during the turn-on interval. For the sake of simplicity, the equivalent impedance of the drive circuit has been assumed as purely resistive.

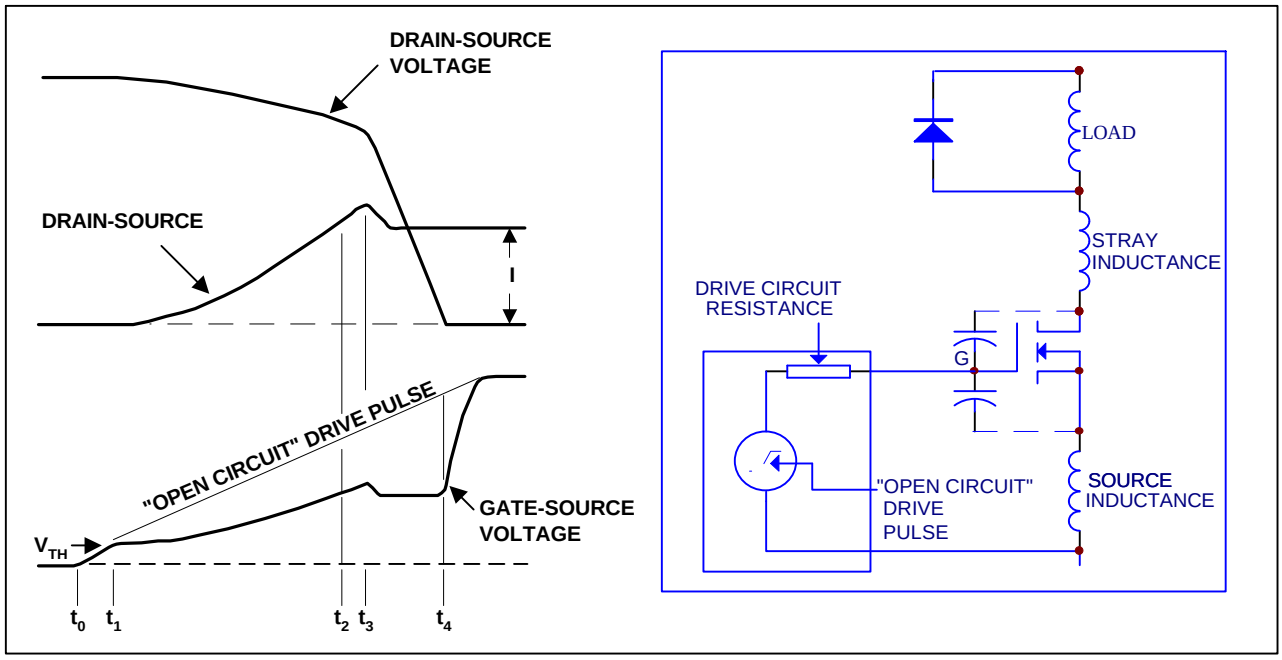

Figure 3. Waveforms at Turn-On

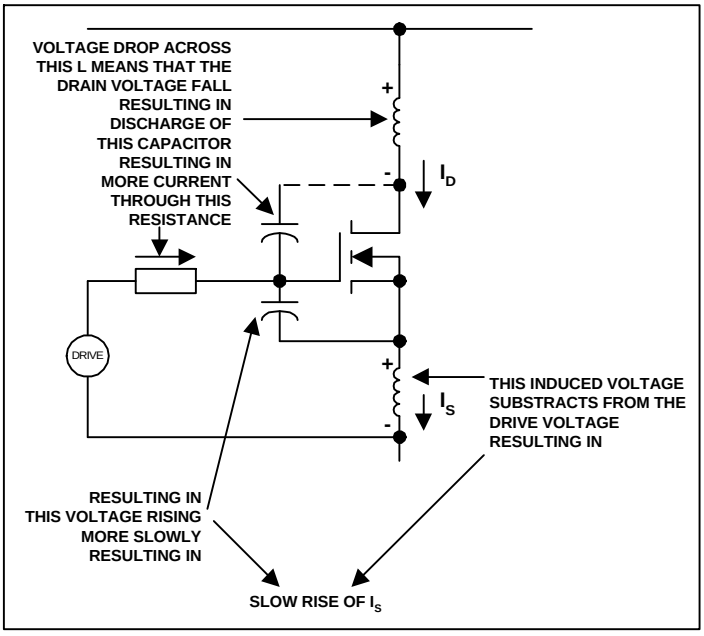

Figure 4. Diagrammatic Representation of Effects When Switching-ON

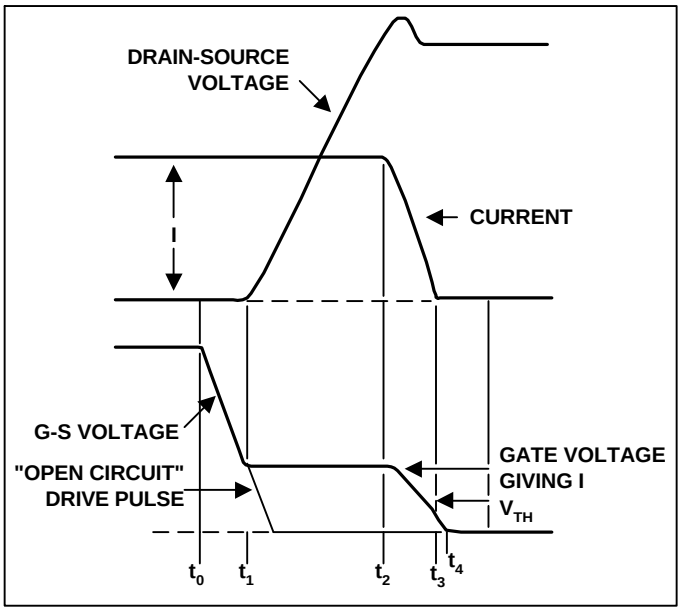

Figure 5. Waveforms at Turn-OFF

At time, t_0, the drive pulse starts to rise. At t_0 it reaches the threshold voltage of the HEXFET®s and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original “path”. First, inductance in series with the source which is common to the gate circuit (“common source inductance”) develops an induced voltage as a result of the increasing source current. This voltage counteracts the applied gate drive voltage, and slows down the rate of rise of voltage appearing directly across the gate and source terminals; this in turn slows down the rate of rise of the source current. This is a negative feedback effect: increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so called “Miller” effect. During the period t_1 to t_2 some voltage is dropped across “unclamped” stray circuit inductance in series with the drain, and the drain-source voltage starts to fall. The

decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitive load on the drive circuit.
This in turn increases the voltage drop across the source impedance of the drive circuit, and decreases the rate of rise of voltage appearing between the gate and source terminals. Obviously, the lower the impedance of the gate drive circuit, the less this effect will be. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which in turn slows down the rise of gate-source voltage, and tends to resist the increase of drain current. These effects are illustrated diagramatically in Figure 4. This state of affairs continues throughout the period t_1 to t_2, as the current in the HEXFET®rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, when the freewheeling rectifier goes into reverse recovery.

Finally, at time t_3 the freewheeling rectifier starts to support voltage and drain current and voltage start to fall. The rate of fall of drain voltage is now governed almost exclusively by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current estab-lished by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the drain current, while the drain voltage falls. Obviously, the lower the impedance of the gate-drive circuit, the higher the discharge current through the drain-gate self-capacitance, the faster will be the fall time of the drain voltage and the switching losses.

Finally, at time t_4, the HEXFET®is switched fully on, and the gate-to-source voltage rises rapidly towards the applied “open circuit” value.

Similar considerations apply to the turn-off interval. Figure 5 shows theoretical waveforms for the HEXFET®in the circuit of Figure 4 during the turn-off interval. At t_o the gate drive starts to fall until, at t_l , the gate voltage reaches a level that just sustains the drain current and the device enters the linear mode of operation. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. Once again, the lower the impedance of the drive circuit, the greater the charging current into the drain-gate capacitance, and the faster will be the rise time of the drain voltage. At t_3 the rise of drain voltage is complete, and the gate voltage and drain current start to fall at a rate determined by the gate-source circuit impedance.

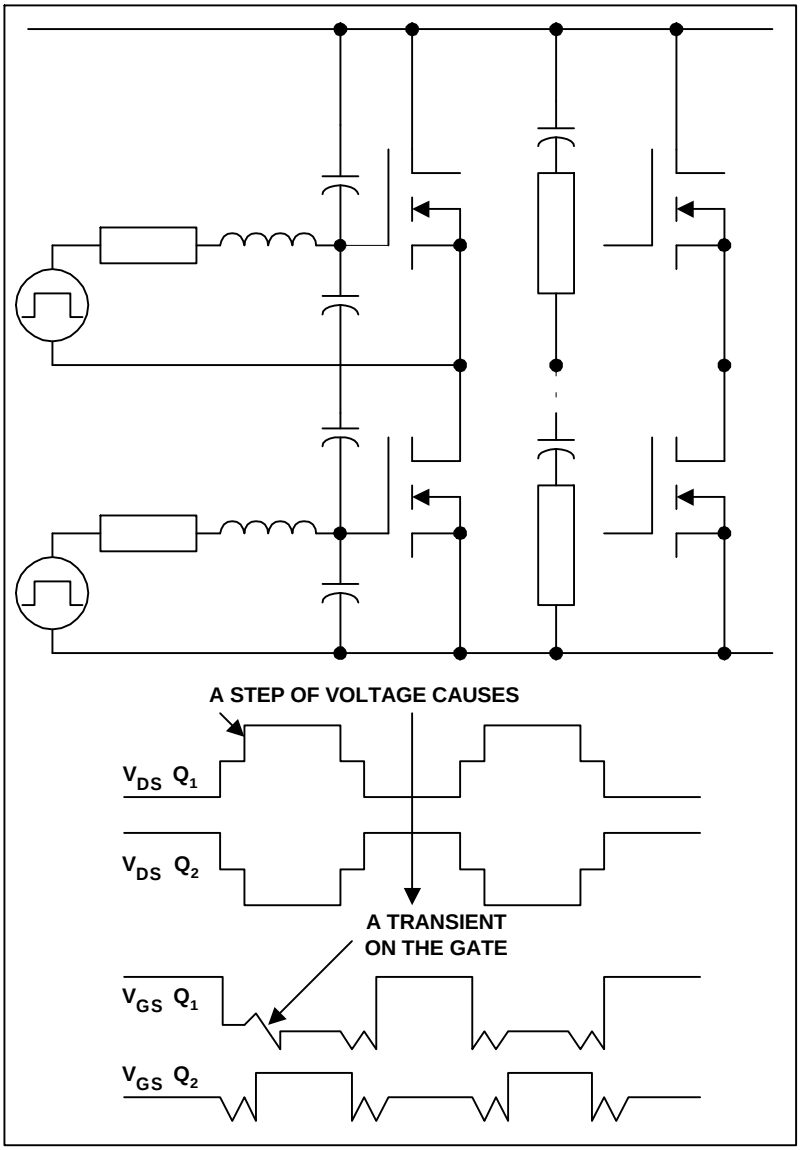

Figure 6. Transients of Voltage Induced on the Gate by Rapid Changes on the Drain-to-Source Voltage

We have seen how and why a low gate drive impedance is important to achieve high switching performance. However, even when switching performance is of no great concern, it is important to minimize the impedance in the gate drive circuit to clamp unwanted voltage transients on the gate. With reference to Figure 6, when one HEXFET®is turned on or off, a step of voltage is applied between drain and source of the other device on the same leg. This step of voltage is coupled to the gate through the gate-to-drain capacitance, and it can be large enough to turn the device on for a short instant (“dv/dt induced turn-on”). A low gate drive impedance would keep the voltage coupled to the gate below the threshold.

In summary: MOS-gated transistors should be driven from low impedance (voltage) sources, not only to reduce switching losses, but to avoid dv/dt induced turn-on and reduce the susceptibility to noise.

4. DRIVING STANDARD HEXFET®S FROM TTL

Table 1 shows the guaranteed sourcing and sinking currents for different TTL families at their respective voltages. From this table, taking as an example of the 74LS series, it is apparent that, even with a sourcing current as low as 0.4 mA, the guaranteed logic one voltage is 2.4V (2.7 for 74LS and 74S). This is lower than the possible threshold of a HEXFET®. The use of a pull-up resistor in the output, as shown in Figure 7, takes the drive voltage up to 5 V, as necessary to drive the gate of Logic Level HEXFET®s, but is not sufficient to fully enhance standard HEXFET®s. Section 8 covers the drive characteristics of the logic level devices in detail.

Logic Conditions	54 / 74	54H / 74H	(54L) / 74L	(54LS) / 74LS	74S
Logic Zero Min. sink current for V_{OL}	16mA ≤ 0.4V	20mA ≤ (0.4V) /	20mA ≤ (0.3V) / 0.4V	(4) / 8 ≤ (0.4V) / 0.5V	20mA 0.5V
Logic One Max. source current for V_{OH}	-0.4mA ≥2.4V	-0.5mA ≥2.4V	-0.2mA ≥2.4V	-0.4mA ≥ (2.5) / 2.7V	-1.0mA ≥2.7V
Typical Gate Propagation Delay	10ns	7ns	50ns	12ns	4ns

Table 1. Driving HEXFET®s from TTL (Totem Pole Outputs)

Open collector buffers, like the 7406, 7407, etc., possibly with several drivers connected in parallel as shown in Figure 9, give enough voltage to drive standard devices into "full enhancement", i.e. data sheet on-resistance. The impedance of this drive circuit, however, gives relative long switching times. Whenever better switching performance is required, interface circuits should be added to provide fast current sourcing and sinking to the gate capacitances. One simple interface circuit is the complementary source-follower stage shown in Figure 9. To drive a MOSFET with a gate charge of 60 nC in 60 ns an average gate current of 1 A has to be supplied by the gate drive circuit, as indicated in INT-944. The on-resistance of the gate drive MOSFETs has to be low enough to support the desired switching times.

With a gate charge of 60 nC and at a switching frequency is 100kHz, the power lost in the gate drive circuit is approximately:

$P = V_{GS} \times Q_G \times f = 12 \times 60 \times 10^{-9} \times 100 \times 10^{3} = 72mW$

The driver devices must be capable of supplying 1A without significant voltage drop, but hardly any power is dissipated in them.

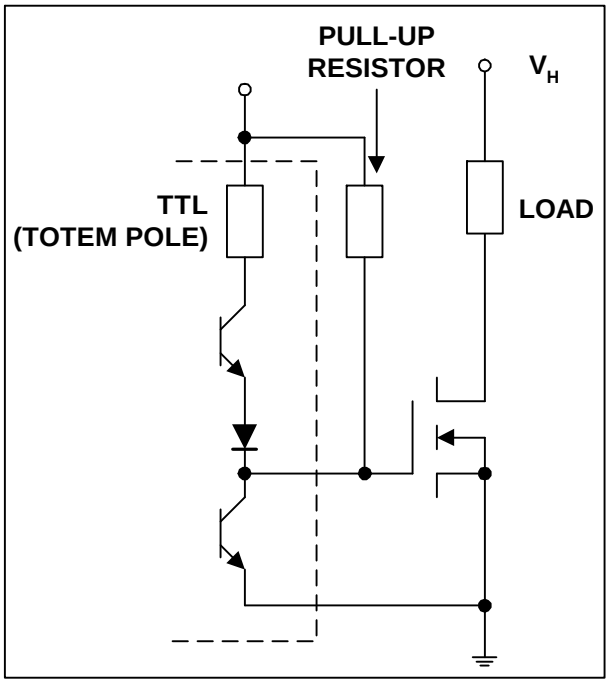

Figure 7. Direct Drive from TTL Output

5. DRIVING STANDARD HEXFET®S FROM C-MOS

While the same general considerations presented above for TTL would also apply to C-MOS, there are three substantial differences that should be kept in mind:

1. C-MOS has a more balanced source/sink characteristic that, on a first approximation, can be thought of as a 500 ohm resistance for operation over 8V and a 1k ohm for operation under 8V (Table 2).

2. C-MOS can operate from higher supply voltages than 5V so that HEXFET® saturation can be guaranteed.
3. Switching times are longer than those for TTL (Table 2).

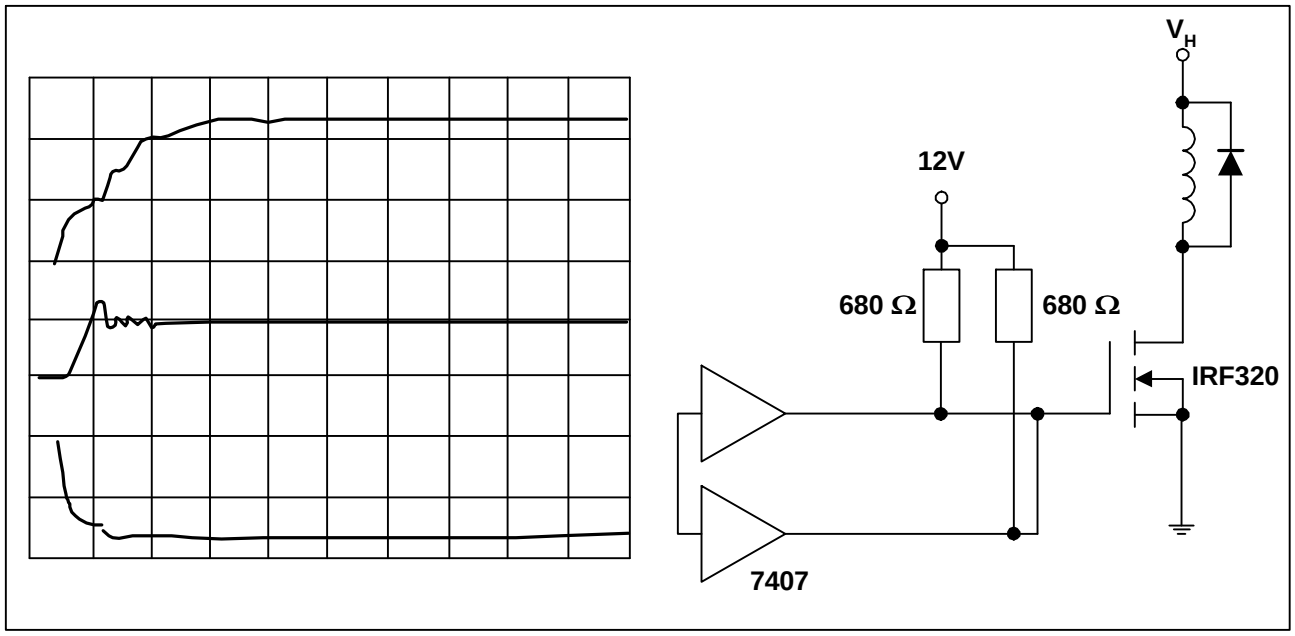

Figure 8. High Voltage TTL driver and its waveforms

When C-MOS outputs are directly coupled to the gate of a HEXFET®, the dominant limitation to performance is not the switching time, but the internal impedance (assuming that C-MOS are operated from a 10V or higher voltage supply). It will certainly not be able to turn OFF the HEXFET® as fast as the TTL, while the turn-ON waveform will be slightly better than what can be achieved with a 7407 with a 680 ohm pull-up resistor. Of course, gates can be paralleled in any number to lower the impedance and this makes C-MOS a very simple and convenient means of driving HEXFET®s. Drivers can also be used, like the 4049 and 4050 which have a much higher current sinking capability (Table 2), but they do not yield any significant improvement in current sourcing.

For better switching speeds, buffer circuits, like the one shown in Figure 9, should be considered, not only to provide better current sourcing and sinking capability, but also to improve over the switching times of the C-MOS output itself and the dv/dt noise immunity.

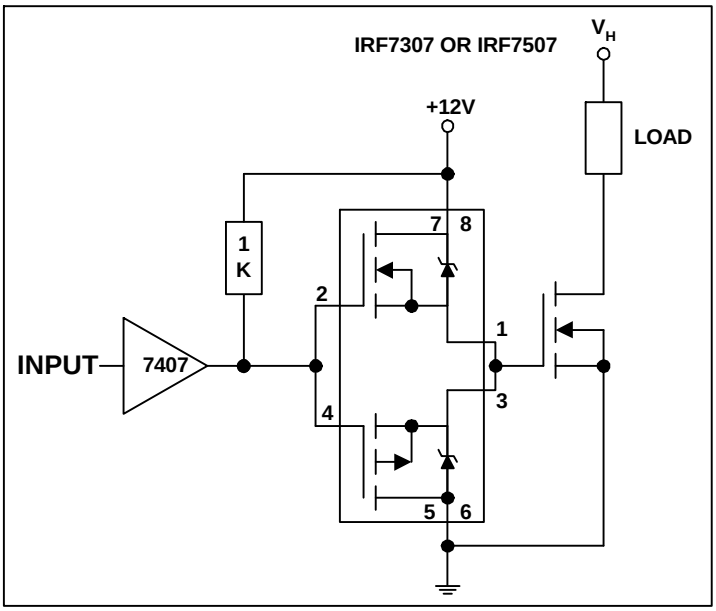

Figure 9. Simple Interface to Drive HEXFETs from TTL

6. DRIVING HEXFET®S FROM LINEAR CIRCUITS

The complementary source follower configuration of Figure 9 can also be used in linear applications to improve drive capability from an opamp or other analog source.

Most operational amplifiers have a very limited slew rate, in the order of few V/microsec. This would limit the bandwidth to less than 25kHz. A larger bandwidth can be obtained with better operational amplifiers followed by a current booster, like the ones shown in Figures 10 or 11. For a system bandwidth of 1MHz, the opamp bandwidth must be significantly higher than 1MHz and its slew rate at least 30V/μs.

Logic Supply Voltage / Logic Conditions	Standard Buffered Outputs			4049 / 4050 Drivers		
	5V	10V	15V	5V	10V	15V
Logic Zero: Approximate sink current for $V_{OL} \leq 1.5V$	1.5mA	3.5mA	4mA	20mA	40mA	40mA
Logic One: Minimum source current for V_{OH}	-0.5mA $\geq$ 4.6V	-13mA $\geq$ 9.5V	-3.4mA $\geq$ 13.5V	-1.25mA $\geq$ 2.5V	-1.25mA $\geq$ 9.5V	-3.75mA $\geq$ 13.5V
Typical switching times of logic drive signals:						
RISE	100ns	50ns	40ns	100ns	50ns	40ns
FALL	100ns	50ns	40ns	40ns	20ns	15ns

Table 2. Driving HEXFET®s from C-MOS (Buffered)

When analog signals determine the switching frequency or duty cycle of a HEXFET®, as in PWM applications, a voltage comparator is normally used to command the switching. Here, too, the limiting factors are the slew rate of the comparator and its current drive capability. Response times under 40ns can be obtained at the price of low output voltage swing (TTL compatible). Once again, the use of output buffers like the ones shown in Figures 9, may be necessary to improve drive capability and dv/dt immunity. If better switching speeds are desired. a fast op-amp should be used.

In many applications, when the HEXFET®is turned on, current transfers from a freewheeling diode into the HEXFET®. If the switching speed is high and the stray inductances in the diode path are small, this transfer can occur in such a short time as to cause a reverse recovery current in the diode high enough to short out the dc bus. For this reason, it may be necessary to slow down the turn-on of the HEXFET®while leaving the turn-off as fast as practical. Low impedance pulse shaping circuits can be used for this purpose, like the ones in Figures 12 and 13.

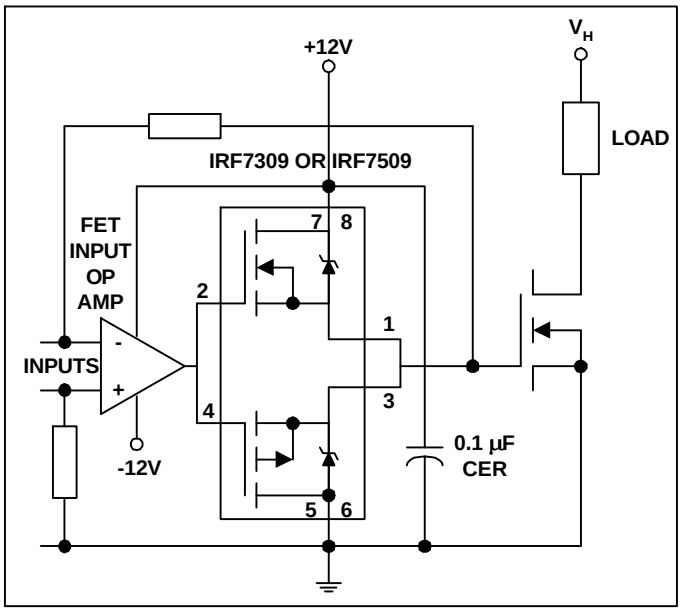

Figure 10. Dual Supply Op-Amp Drive Circuit

7. DRIVE CIRCUITS NOT REFERENCED TO GROUND

To drive a HEXFET®into saturation, an appropriate voltage must be applied between the gate and source. If the load is connected between source and ground, and the drive voltage is applied between gate and ground, the effective voltage between gate and source decreases as the device turns on. An equilibrium point is reached in which the amount of current flowing in the load is such that the voltage between gate and source maintains that amount of drain current and no more. Under these conditions the voltage drop across the MOSFET is certainly higher than the threshold voltage and the power dissipation can be very high. For this reason, the gate drive circuit is normally referenced to the source rather than to the ground. There are

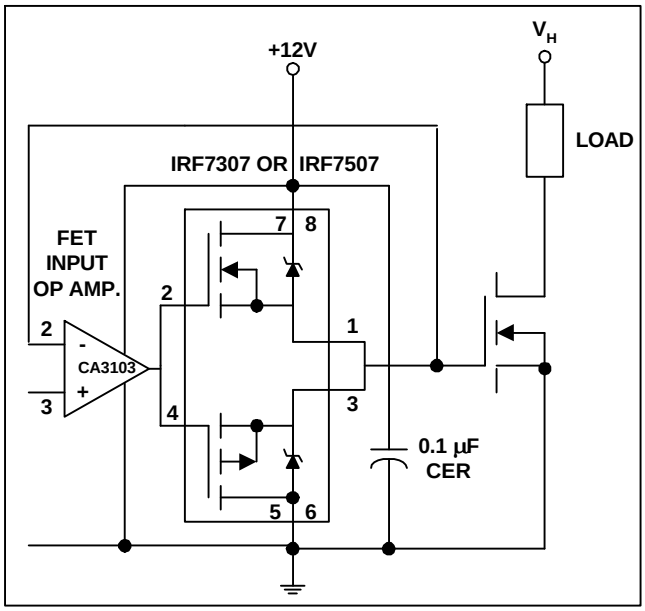

Figure 11. Single Supply Op-Amp Drive Circuit (Voltage Follower)

basically three ways of developing a gate drive signal that is referenced to a floating point:

1. By means of optically coupled isolators.
2. By means of pulse transformers.

By means of DC to DC chopper circuits with transformer isolation.

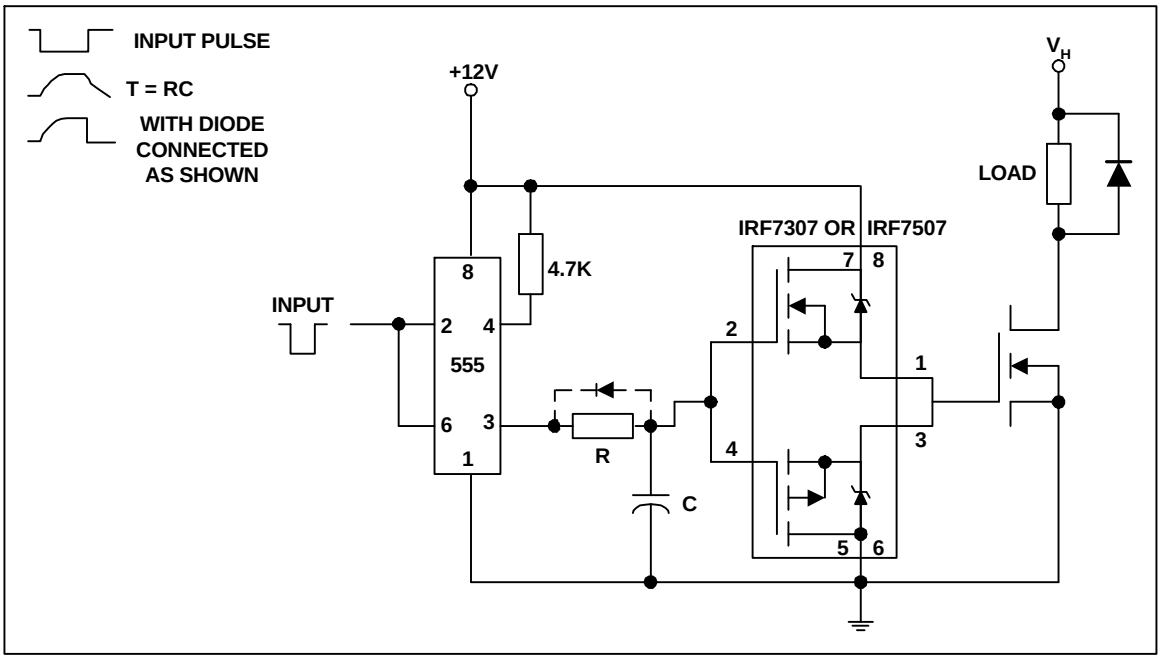

Figure 12. A pulse shaper. The 555 is used as an illustration of a Schmitt Trigger pulse shaper

7.1 MGDs with optocouplers

Most optocouplers require a separate supply grounded to the source on the receiving end of the optical link and a booster stage at the output, as shown in Figure 14a. One of the major difficulties encountered in the use of optocouplers is their susceptibility to noise. This is of particular relevance in applications where high currents are being switched rapidly. Because of the dv/dt seen by the V_{EE} pin, the optocoupler needs to be rated for high dv/dt, in the order of 10 V/ns.

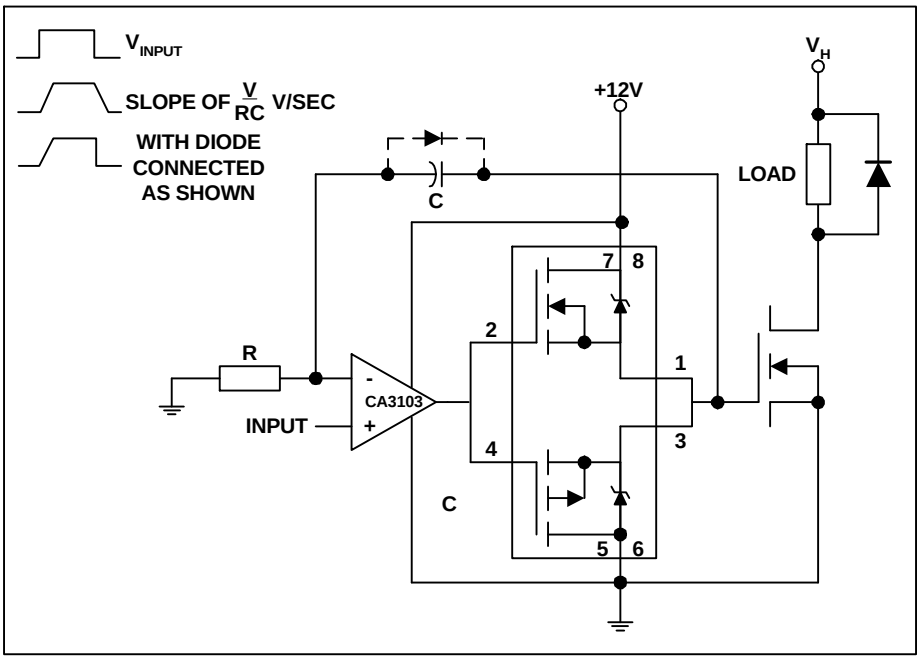

Figure 13. Pulse shaper implemented with an integrator

Figure 15a shows an MGD with under-voltage lockout and negative gate bias. When powered with a 19 V floating source, the gate drive voltage swings between +15V and -3.9V. D1 and R2 offset the emitter voltage by 3.9V. The switching waveforms shown in Figure 15b are similar to those in Figure 14b except for the negative bias. Q3, D2 and R5 form the under voltage lockout circuit.

The LED D2 is used as low voltage, low current reference diode. Q3 turns on when the voltage at the anode of D2 exceeds the sum of the forward voltage of LED and the base-emitter voltage of Q3. This enables the operation of the optocoupler. The tripping point of the under voltage lock-out circuit is 17.5V. The start-up wave forms are shown in Figure 16.

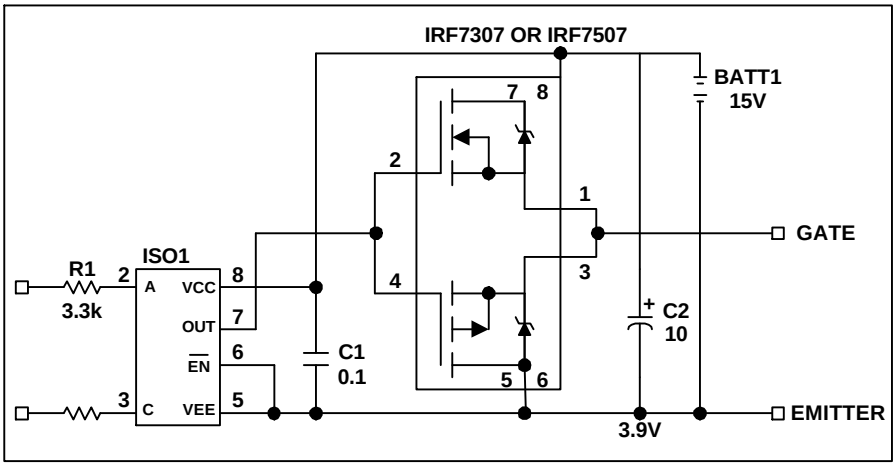

Figure 14a. Simple high current optoisolated driver

The auxiliary supply for the optocoupler and its associated circuitry can be developed from the drain voltage of the MOSFET itself, as shown in Figure 17, 18 and 19. This supply can be used in conjunction with the UV-lockout shown in Figure 15 to provide a simple high-quality optoisolated drive.

The circuit in Figure 17a can be modified to provide higher output current. By changing C1 to 680pF and R3 to 5.6k, its performance changes to what is shown in Figures 20, 21 and 22. Other methods of developing isolated supplies are discussed in Section 9.

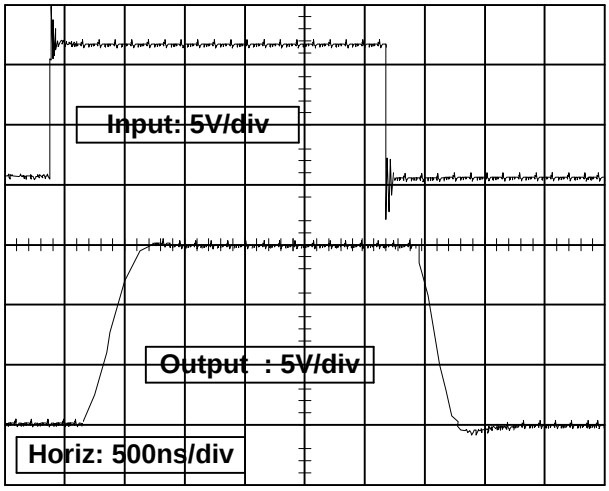

Figure 14b: Waveforms associated with the circuit of Figure 14a when loaded with 100nF

7.2 Pulse transformers

A pulse transformer is, in principle, a simple, reliable and highly noise-immune method of providing isolated gate drive. Unfortunately it has many limitations that must be overcome with additional components. A transformer can only transfer to the secondary the AC component of the input signal. Consequently, their output voltage swings from negative to positive by an amount that changes with the duty cycle, as shown in Figure 23. As a stand-alone component they can be used for duty cycles between 35 and 65%.

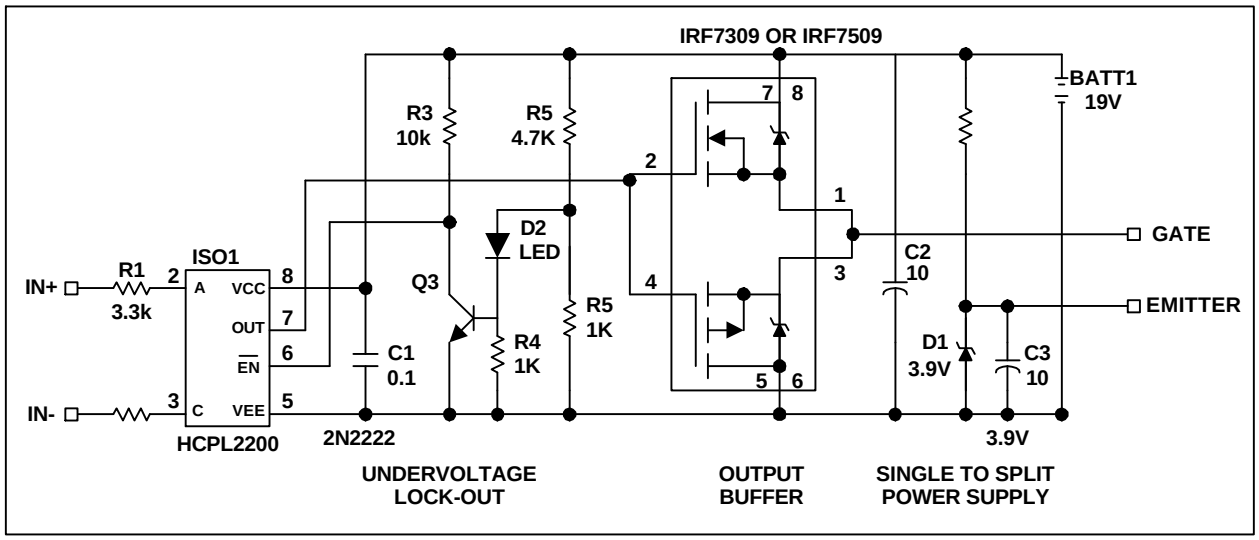

Figure 15a: Optoisolated driver with UV lockout and negative gate bias

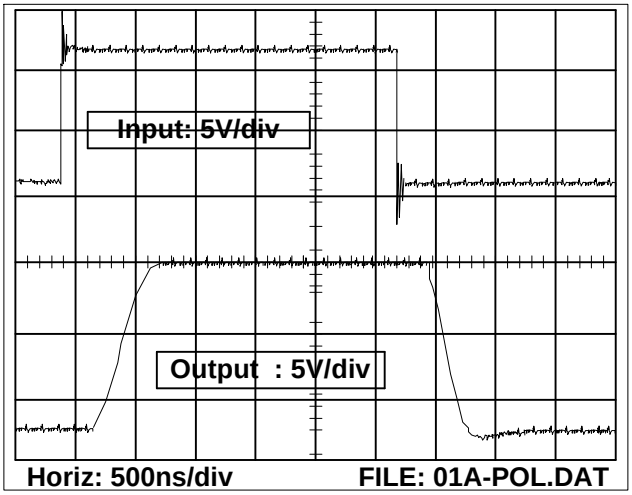

Figure 15b: Waveforms of the circuit in Figure 21a when loaded with 100nF

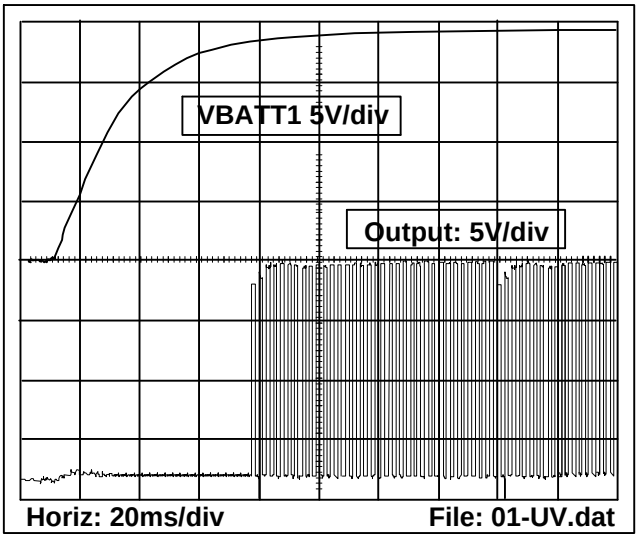

Figure 16. Start-up waveforms for the circuit of Figure 15a.

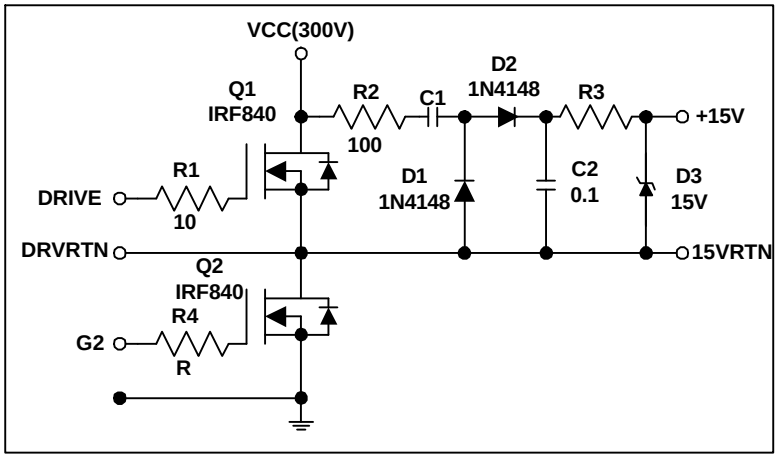

Figure 17a. Drive supply developed from the drain voltage

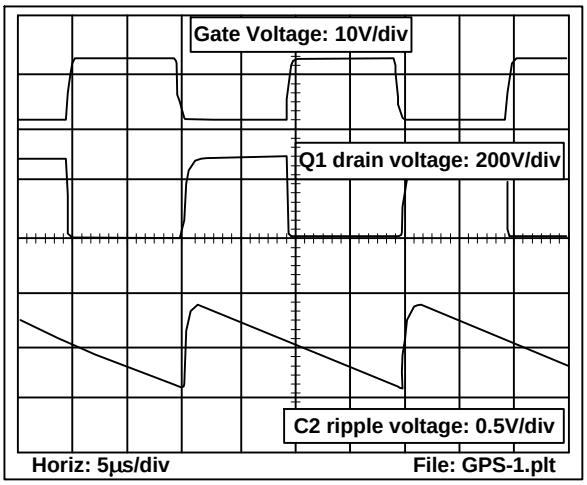

Figure 17b. Waveforms of the circuit in Figure 23a.C1 = 100 pF, R3 = 5.6 k, f = 50 kHz

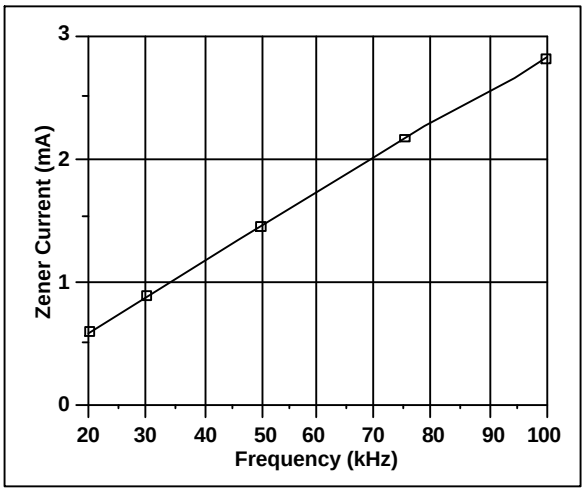

Figure 18. Zener current (max output current) for the circuit in Figure 23a.

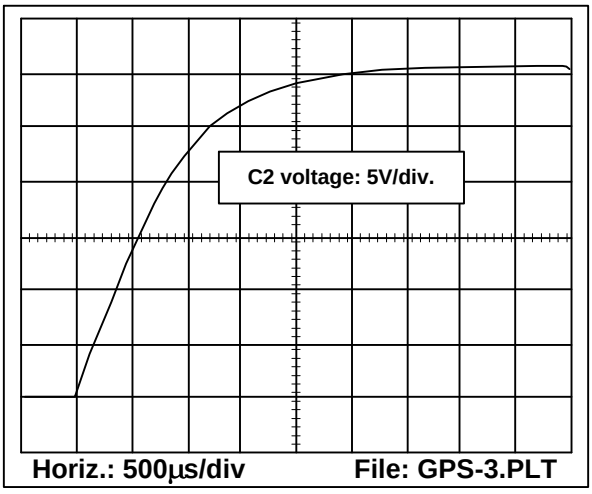

Figure 19. Start-up voltage at 50 kHz for the circuit in Figure 23a.

They have the additional advantage of providing a negative gate bias. One additional limitation of pulse transformers is the fact that the gate drive impedance is seriously degraded by the leakage inductance of the transformer. Best results are normally obtained with a few turns of twisted AWG30 wire-wrap wire on a small ferrite core.

Lower gate drive impedance and a wider duty-cycle range can be obtained with the circuit in Figure 24a. In this circuit, Q1 and Q2 (a single Micro-8 package) are used to buffer the input and drive the primary of the transformer. The complementary MOS output stage insures low output impedance and performs wave shaping. The output stage is fed by a dc restorer made by C2 and D1 that references the signal to the positive rail. D1 and D2 are also used to generate the gate drive voltage.

The input and output wave form with 1nF load capacitance are shown in Figure 24b. The turn-on and turn-off delays are 50ns. The rise and fall times are determined by the 10 Ohm resistor and the capacitive load. This circuit will operate reliably between 20 and 500 kHz, with on/off times from 0.5 to 15 microsecs.

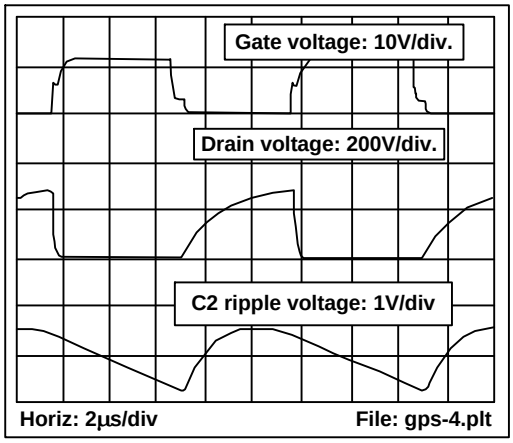

Figure 20. Waveforms of the circuit in Figure 23a. with C1=680pF, R3=1k, f=100kHz.

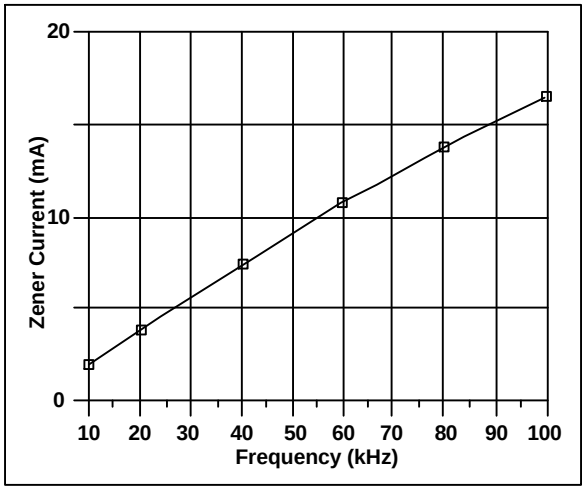

Figure 21. Zener current (max output current) for the circuit in Figure 23a. with C1 = 680pF, R3 = 1k

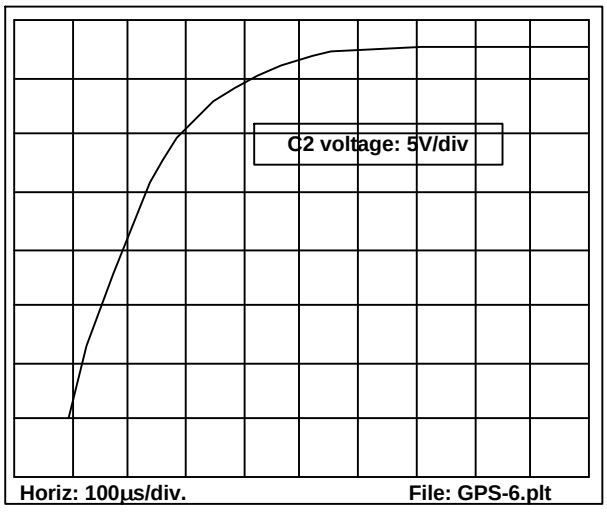

Figure 22. Start-up voltage at 100 kHz for the circuit in Figure 23a. with C1=680pF, R3=R3=1k

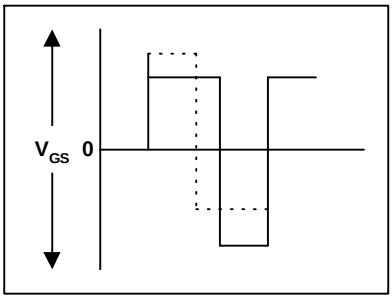

Figure 23. Volt-seconds across winding must balance

Due to the lack of an under voltage lock-out feature, the power-up and power down behavior of the circuit is important. Intentionally C1 and C2 are much bigger in value then C3 so that the voltage across C3 rises to an adequate level during the first incoming pulse. The power-up wave forms at 50kHz switching frequency and 50% duty cycle are shown in Figure 25. During the first pulse, the output voltage is 10V only, and drops back below 10V at the fifth pulse.

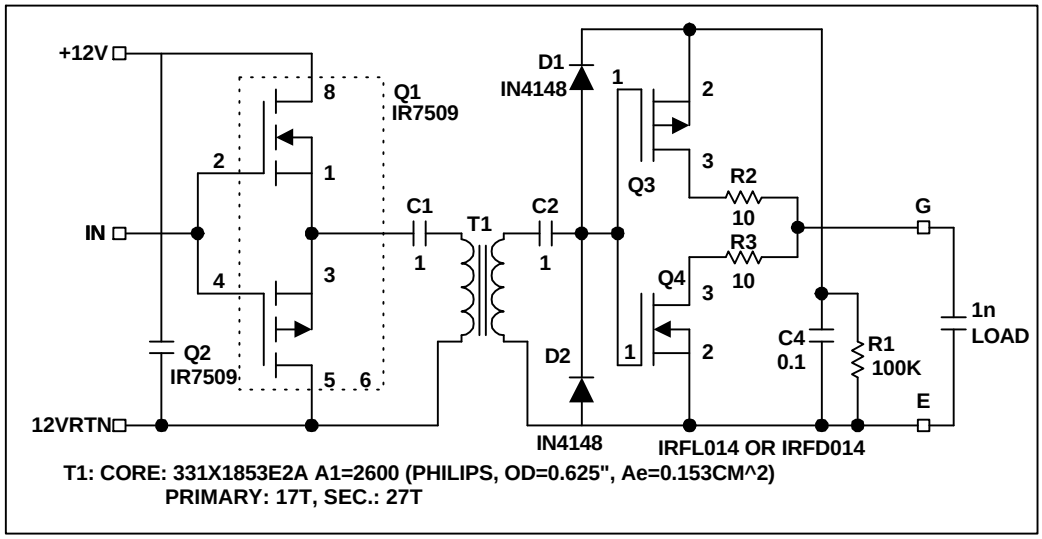

Figure 24a. Improving the performance of a gate drive transformer

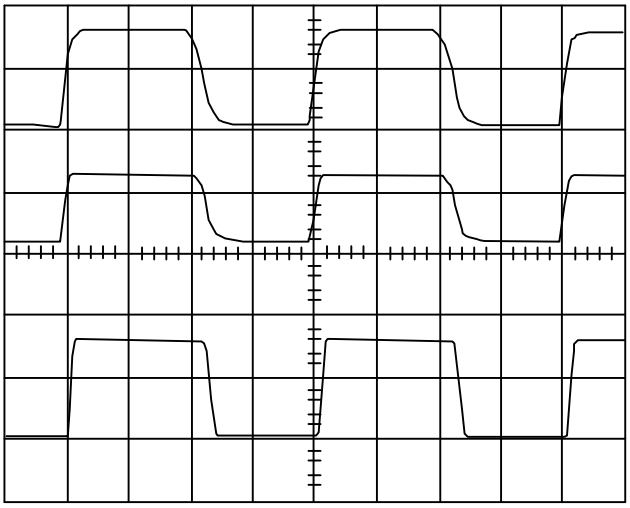

Figure 24b. Waveforms associated with the circuit of Figure 24a

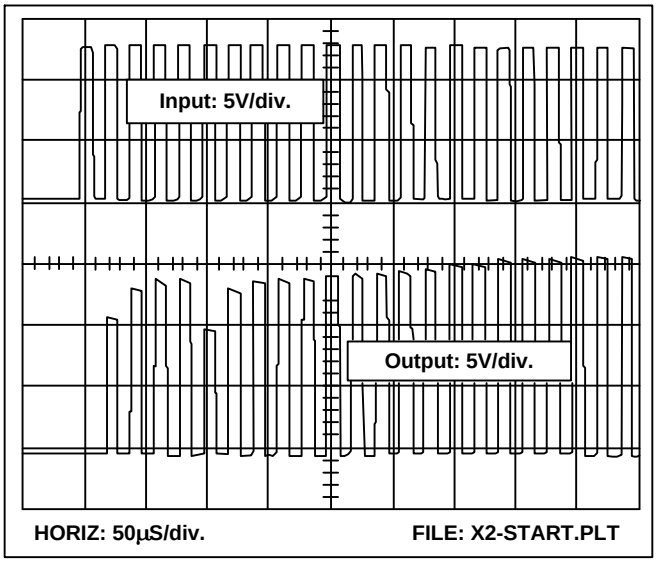

Figure 25. Waveforms during start-up for the circuit in Figure 24a.

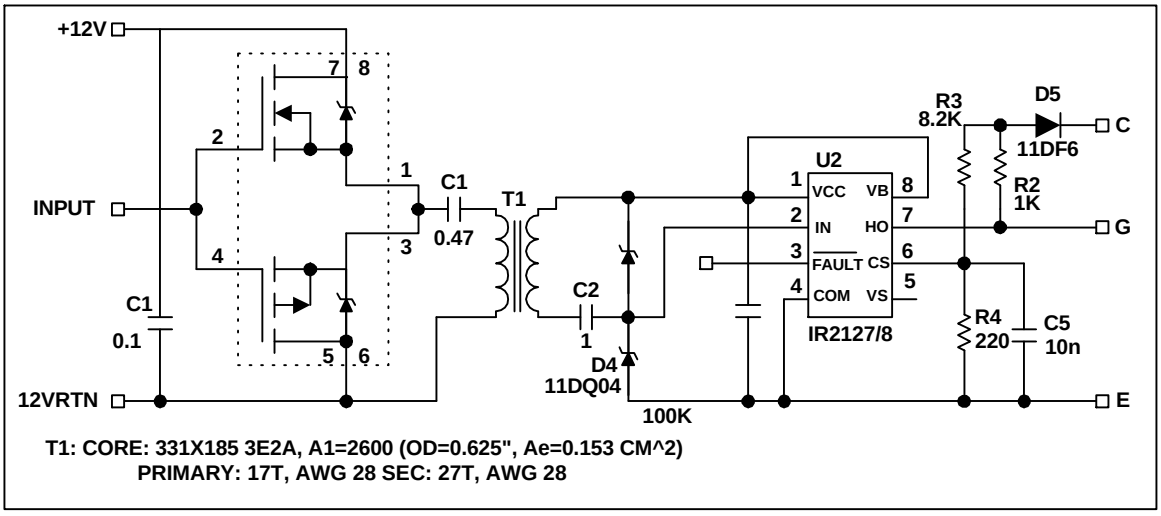

Figure 26a. Transformer-coupled MGD with UV lockout and short-circuit protection

The power down of the circuit is smooth and free from voltage spikes. When the pulse train is interrupted at the input, the C2 capacitor keeps the input of the CMOS inverter high and R1 discharges C3. By the time the input to the CMOS inverter drops below the threshold voltage of Q4, C3 is completely discharged the output remains low.

The addition of a MOS-Gate Driver IC improves the performance of the circuit in Figure 24a, at the expenses of prop delay. The circuit shown in Figure 26a has the following features:

- No secondary supply required
- Propagation delay ~500ns (CL= 10nF)
- Duty cycle range 5% to 85%
- Nominal operating frequency 50kHz (20kHz to 100kHz)
- Short circuit protection with Vce sensing. Threshold Vce = 7.5V
- Undervoltage lock-out at Vcc = 9.5V
- Over voltage lock out at Vcc = 20V

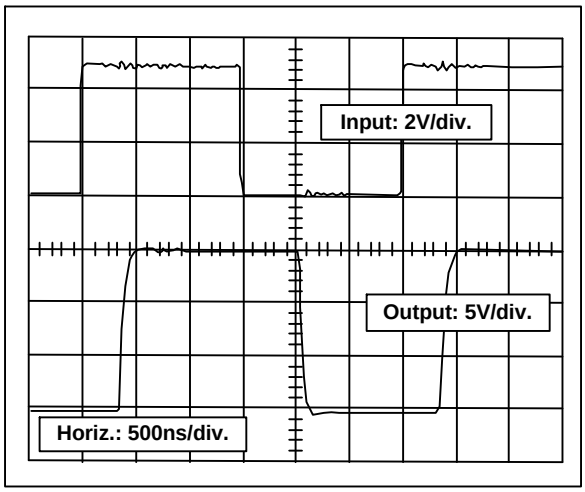

Figure 26b. Waveforms associated with the circuit of Figure 26a.

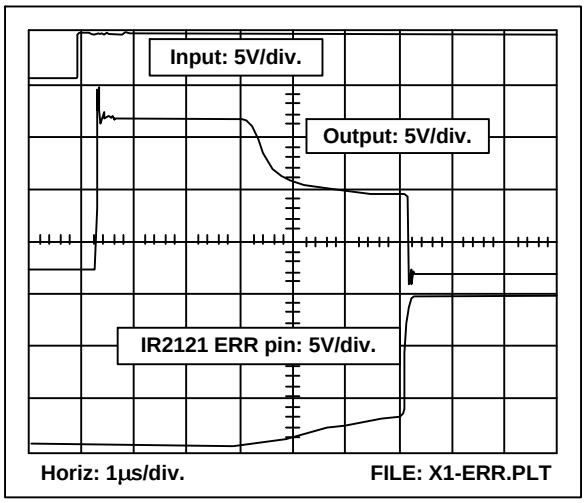

Figure 27. Shutdown due to high V_{CEsat}

The short circuit protection is implemented with a Vce sensing circuit in combination with the current sense input (CS) of IR2127/8. When the HO pin if U2 goes high R3 starts charging C5. Meanwhile the IGBT turns on, the collector voltage drops to the saturation level, D5 goes into conduction and C5 discharges. When the collector voltage is high, D5 is reverse biased and the voltage on C5 keeps raising. When C5 voltage exceeds 250mV the IR2127/8 shuts down the output. The fault to shut-down delay is approximately 2 microsecs.

For operation with a large duty cycle, several options are available. The circuits described in AN-950 use a saturating transformer to transfer the drive charge to the gate. The circuit shown in Figure 28a, on the other hand, achieves operation over a wide range of duty cycles by using the MGD as a latch. It has the following features:

- Frequency range from DC to 900kHz.
- Turn-on delay: 250ns.
- Turn-off delay 200ns
- Duty cycle range from 1% to 99% at 100kHz.
- Under voltage and over voltage lockout.
- Optional short circuit protection, as shown in Figure 26a

In the circuit of Figure 28a the transformer is small (8 turns), since it transmits only short pulses to the secondary side. The MGD on the secondary side of the transformer is latched by the feedback resistor R4. Figures 28b and 28c show the performance of this circuit at the two extremes of 900 kHz and 2.5 Hz

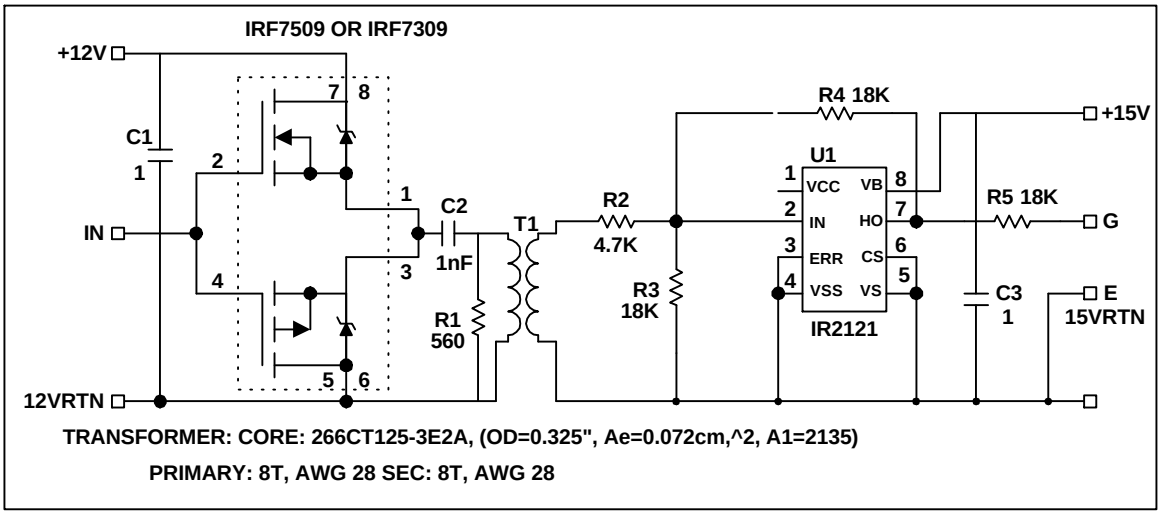

Figure 28a. Transformer-coupled MGD for operation from DC to 900 kHz

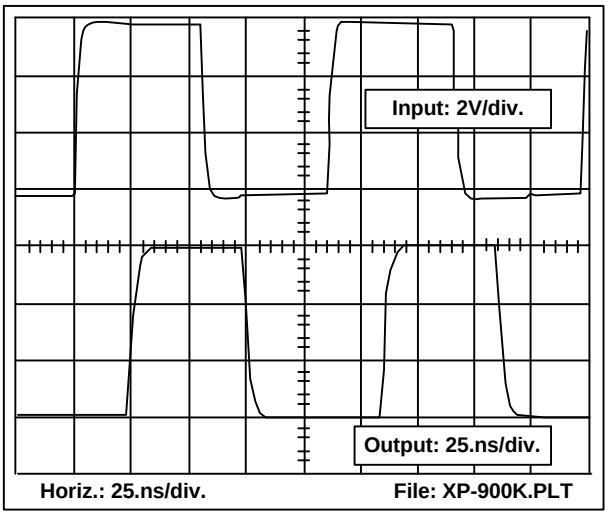

Figure 28b. Waveforms associated with the circuit of Figure 28a operated at 900 kHz

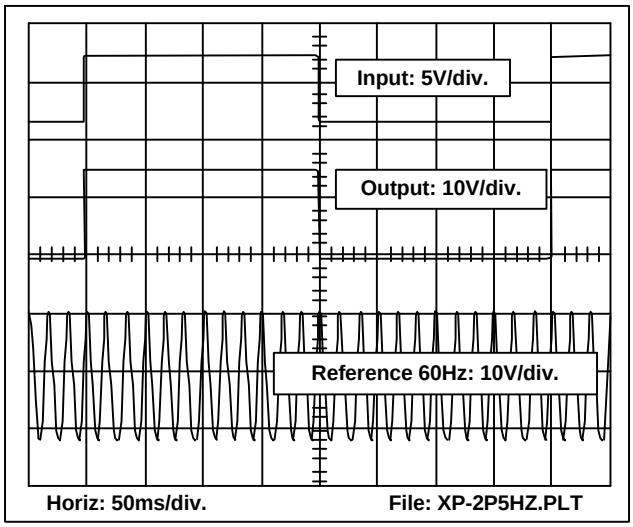

Figure 28c. Waveforms associated with the circuit of Figure 28a operated at 2.5 Hz

7.2 Chopping gate drives

Chopper circuits can maintain a gate drive signal for an indefinite period of time, have good noise immunity performance and, with some additional circuitry, the isolated supply can be avoided.

The basic operating principle is shown in Figure 29. To turn on the MOSFET, a burst of high frequency is transmitted to the secondary side. The MOSFET is turned off by interrupting the high frequency. The diode and the bipolar transistor form a crowbar that rapidly discharges the gate.

In addition to providing the gate drive signal, the high frequency transformer is frequently used to power auxiliary circuitry, like short-circuit protection, thus avoiding a dedicated supply.

8. DRIVE REQUIREMENTS AND SWITCHING CHARACTERISTICS OF LOGIC LEVEL HEXFET®S

Many applications require a power MOSFET to be driven directly from 5 V logic circuitry. The on-resistance of standard power MOSFETs is specified at 10 V gate drive, and are generally not suitable for direct interfacing to 5V logic unless an oversized MOSFET is employed.

Logic level HEXFET®s are specifically designed for operation from 5V logic and have guaranteed on-resistance at 5 or 4.5 V gate voltage. Some have guaranteed on-resistance at 2.7 V.

Some important considerations for driving logic level HEXFET®s are discussed in this section and typical switching performance of these is illustrated when driven by some common logic drive circuits.

8.1 Comparison to Standard HEXFET®s

Some devices are available as Logic-level HEXFET®s as well as standard HEXFET®s. The logic-level version uses a thinner gate oxide and different doping concentrations. This has the following effects on the input characteristics:

- Gate Threshold voltage is lower.
- Transconductance is higher.
- Input capacitance is higher.
- Gate-source breakdown voltage is lower.

While input characteristics are different, reverse transfer capacitance, on-resistance, drain-source breakdown voltage, avalanche energy rating, and output capacitance are all essentially the same. Table 3 summarizes the essential comparisons between standard and logic level HEXFET®s.

Characteristics and Ratings		Standard HEXFET® (IRF Series)	Comparable Logic Level HEXFET® (IRL Series)
Gate Threshold Voltage	$V_{GS(on)}$	2 - 4V	1 - 2V
On-Resistance	$R_{DS(on)}$	Logic level HEXFET® has same value of $R_{DS(on)}$ V_{GS} = 5V as standard HEXFET® at V_{GS} = 10V $R_{DS(on)}$ of logic level HEXFET® also speed at V_{GS} = 4V	
Transconductance	gfs	Typically 39% larger for logic level HEXFET®	
Input Capacitance	Crs	Typically 33% larger for logic level HEXFET®	
Output Capacitance	Crss	Essentially the same	
Reverse Transfer Capacitance	Crss	Essentially the same	
Gate Charge Gate-Source	Qgs	Essentially the same	
Gate-Drain	Qgd	Essentially the same	
Total	Qg	Essentially same as V_{GS} = 10V	Essentially same at V_{GS} = 5V
Drain Source Breakdown Voltage	BV_{DSS}	Same	
Continuous Drain Current	I_D	Same	
Single Pulse Avalanche Energy	E_{AS}	Same	
Max. Gate-Source Voltage	V_{GS}	± 20V	±10V

Table 3: Essential Comparisons of Standard and Logic Level HEXFET®s

The gate charge for full enhancement of the logic level HEXFET®is, however, about the same as for a standard HEXFET®because the higher input capacitance is counteracted by lower threshold voltage and higher transconductance. Since the logic level HEXFET®needs only one half the gate voltage, the drive energy is only about one half of that needed for the standard HEXFET®. Since the gate voltage is halved, the gate drive resistance needed to deliver the gate charge in a given time is also halved, relative to a standard HEXFET®. In other words, for the same switching speed as a standard HEXFET®power MOSFET, the drive circuit impedance for the logic level HEXFET®must be approximately halved.

The equivalence of switching times at one half the gate resistance for the logic level HEXFET®is illustrated by the typical switching times for the IRL540 and the IRF540 HEXFET®s shown in Table 4, using data sheet test conditions.

Gate Resistance	Gate Voltage	Drain Current	Typical Values (ns)			
R_G (Ω)	V_{GS} (V)	I_D (A)	$t_{D\ on}$	t_r	$t_{D\ on}$	t_r
9	10	28	15	72	40	50
4.5	5	28	15	72	44	56

Table 4: Typical Resistive Switching Times for IRL540 and IRF540

TTL families do not actually deliver 5V in their V_{OH} condition, even into an open circuit. The 5V level can, however, be reached by the addition of a pull-up resistor from the output pin to the 5V bus, as illustrated in Figure 30. Without the pull-up resistor, the $R_{DS(on)}$ value at V_{GS} = 5V may not be attained, and the value specified at V_{GS} = 4V should be used for worst case design.

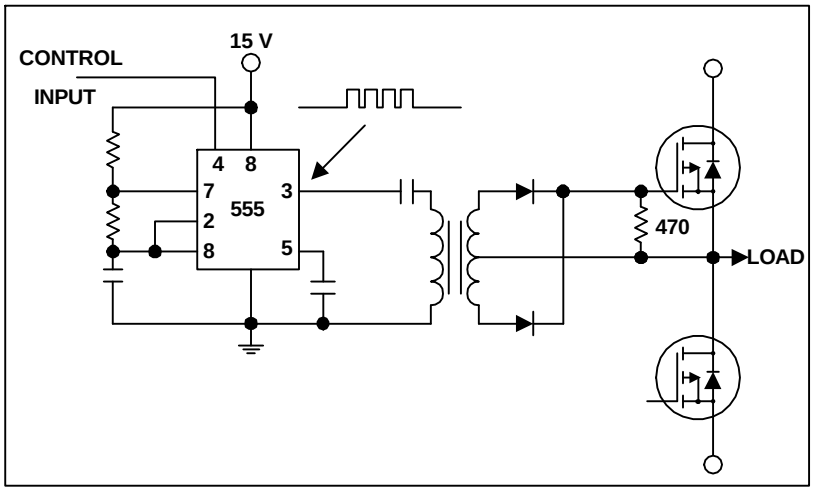

Figure 29.

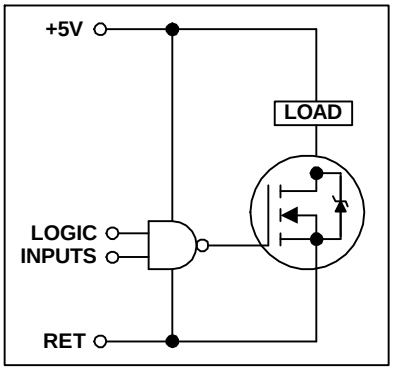

Figure 30. Pull-up resistor used to deliver 5V gate drive

8.2 Driving Logic Level HEXFET®s

The gate threshold voltage of MOSFETs decreases with temperature. At high temperature it can approach the $V_{OL(max)}$ specification of the logic driver. Care should be exercised to insure that $V_{TH(min)}$ at the highest operating temperature is greater than $V_{OL(max)}$ of the various logic families in order to guarantee complete turn off.

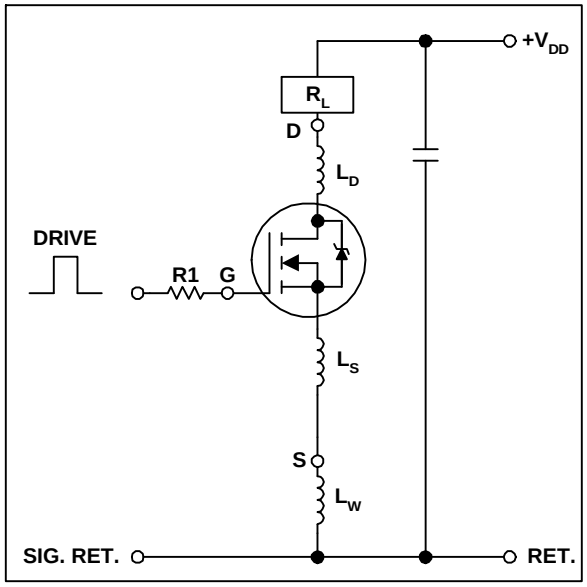

Figure 31a. High common mode inductance

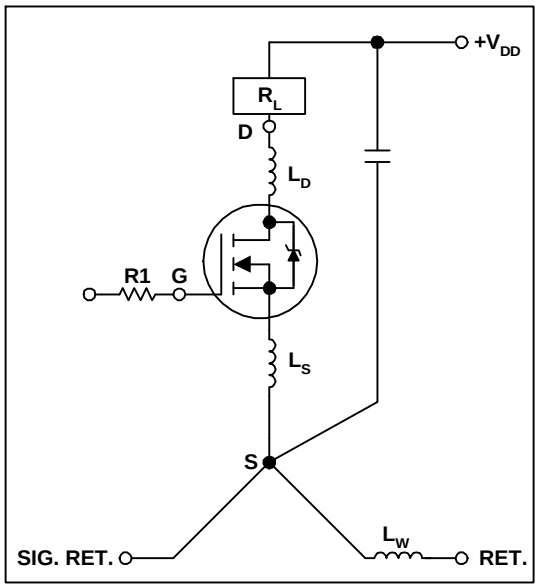

Figure 31b. Minimum common mode inductance

Common source inductance plays a significant role in switching performance. In the circuit of Figure 31a the switching performance is degraded due to the fact that V_{GS} is reduced by (L_S + L_W) di/dt, where di/dt is the rate of change of the drain current. By eliminating L_W from the drive circuit, V_{GS} can approach the applied drive voltage because only L_S (the internal source inductance) is common.

This can be done by separately connecting the power return and the drive signal return to the source pin of the switching HEXFET®, as shown in Figure 31b. Thus, the load current I_D does not flow through any of the external wiring of the drive circuit; consequently, only the internal source inductance L_S is common to both load and drive circuits.

In the case of logic level HEXFET®s, for which V_{GS} is 5V and not 10V, the loss of drive voltage due to common mode inductance has proportionately twice the effect as it would on a 10V drive signal, even though actual values of L_S and L_W are the same.

8.3 Resistive Switching Tests

In the following tests of switching performance, the physical layout of the test circuit was carefully executed so to minimize the common source inductance. The following precautions were also observed:

1. R_L was built by paralleling 0.5W resistors to achieve the desired load resistance (see Table 5).
2. To minimize inductance in the load circuit, a 10 μF low-ESR low-ESL capacitor was connected directly from $+V_{DD}$ to the source of the DUT.
3. To provide a low source impedance for the 5V gate pulse of the DUT, a 0.1 μF low-ESR low-ESL capacitor was connected directly between pin 14 and pin 7 of the driver IC.
4. To provide minimum common source impedance, the source of the DUT was the common return point of all ac and dc system grounds.
5. To reduce stray inductances and thus achieve maximum switching speeds, the physical size of the high current loop (R_L, DUT, 10 μF) was reduced to the smallest practical limits.

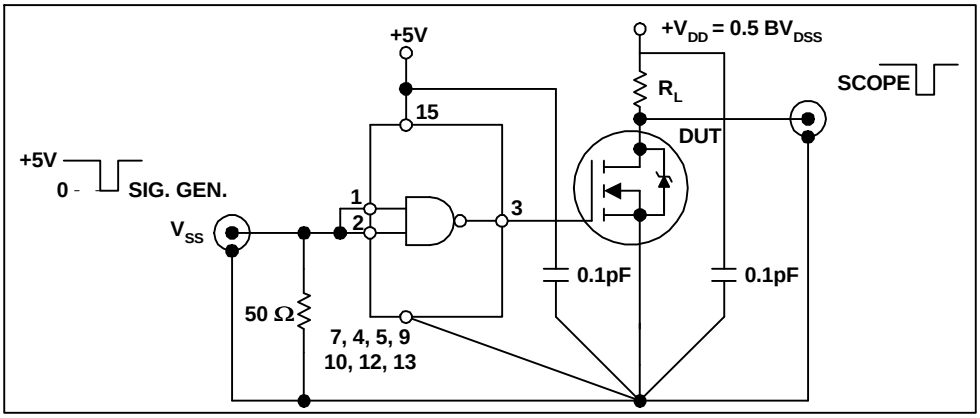

Figure 32. Switching test circuit. Logic level driver is one-quarter of a quad NAND gate.

Only the 5 volt families have been tested as logic level HEXFET®drives: bipolar and CMOS (and their derivatives), as indicated below.

TTL GATES

DM7400N:	Standard TTL
74F00PC:	High Speed TTL
DM74S00N:	Schottky TTL
DM74LS00N:	Low Power Schottky TTL
DM74AS00N:	Advanced Schottky TTL

CMOS GATES

74AC00PC: Advanced CMOS
74ACT00PC: TTL Compatible CMOS
MM74HC00N: Micro CMOS
MM74HCT00N: TTL Compatible Micro CMOS

BIPOLAR
DS0026: High Speed MOSFET Driver

The test conditions for the resistive switching performance is shown in Table 5. The resistive switching times obtained with the above TTL and CMOS gates are tabulated in Table 6. In this table t_{on} = Time in microseconds from 90% to 10% V_{DD} and t_{off} = Time in microseconds from 10% to 90% V_{DD}. Inductive switching gives faster voltage rise times than resistive switching due to the resonant charging of the output capacitance of the device. Voltage fall times are essentially the same.

LOGIC LEVEL HEXFET®	SWITCHING VOLTAGE (V)	SWITCHING CURRENT (A)	R_{DSON} (Ω)	R_L (Ω)
IRLZ14	30	8	0.24	3.25
IRLZ24	30	16	0.12	1.5
IRLZ34	30	24	0.06	1.2
IRLZ44	30	40	0.034	0.7
IRLZ514	50	5	0.60	9.5
IRLZ524	50	8	0.30	5.9
IRLZ524	50	12	0.18	4.0
IRLZ544	50	25	0.085	1.9

Table 5. Resistive Switching Conditions

Logic Family	Logic Level HEXFET®,															
Quad, Dual Input	IRLZ14		IRLZ24		IRLZ34		IRLZ44		IRL514		IRL524		IRL534		IRL544	
Nand Gate	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}
DM7400N STANDARD TTL	0.173	0.018	0.663	0.026	0.700	0.076	1.491	0.146	0.151	0.022	0.238	0.041	0.263	0.060	0.616	0.124
7400FDOPC HIGH SPEED TTL	0.124	0.008	0.490	0.013	0.429	0.068	0.863	0.146	0.104	0.004	0.159	0.034	0.176	0.059	0.372	0.136
DM7400 SCHOTTKY TTL	0.133	0.092	0.549	0.020	0.503	0.032	1.068	0.142	0.116	0.006	0.183	0.041	0.212	0.057	0.441	0.132
DM74LS LOW POWER SCHOTTKY TTL	0.174	0.038	0.778	0.093	0.706	0.146	1.438	0.342	0.155	0.040	0.240	0.062	0.267	0.090	0.567	0.199
DM4SDON ADVANCED SCHOTTKY TTL	0.126	0.008	0.567	0.013	0.446	0.023	0.896	0.149	0.111	0.005	0.161	0.127	0.176	0.058	0.336	0.130
74ACOOPC ADVANCED CMOS	0.012	0.007	0.120	0.012	0.125	0.027	0.251	0.139	0.036	0.004	0.052	0.028	0.066	0.055	0.125	0.125
74ACTOOPC TTL COMPATIBLE CMOS	0.012	0.006	0.121	0.011	0.125	0.016	0.233	0.127	0.033	0.044	0.052	0.027	0.060	0.055	0.120	0.122
MM74CHCOON MICRO CMOS	0.066	0.039	0.179	0.091	0.227	0.147	0.508	0.328	0.058	0.044	0.092	0.068	0.111	0.096	0.232	0.213
MM74HCTCO4 TTL COMPATIBLE MICRO CMOS	0.066	0.030	0.179	0.060	0.227	0.123	0.504	0.269	0.068	0.035	0.092	0.051	0.111	0.086	0.232	0.186
DS0026 HIGH SPEED MOSFET DRIVER	0.052	0.005	0.016	0.005	0.014	0.007	0.032	0.016	0.021	0.004	0.036	0.004	0.036	0.005	0.029	0.009

Table 6. Results of the resistive load switching test

Typical Test Oscillograms

IRLZ24: 60V, 0.1 Ohm, N-Channel, TO-220 logic level HEXFET®was driven by each of the logic families listed in Table 4 and the comparative resistive switching times photographed.

9. SIMPLE AND INEXPENSIVE METHODS TO GENERATE ISOLATED GATE DRIVE SUPPLIES

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In several applications, dc-to-dc converters are used to power the MOS Gate Driver. Although the gate drive requires little power, the noisy environment, the isolation voltage and creepage distance requirements and the high dv/dt between the primary and secondary size make the design of the DC-to-DC converter somewhat complicated. Its key parameters are listed below: OUTPUT VOLTAGE, CURRENT. The output voltage of the DC-to-DC converter is the sum of the positive and negative drive voltage to the gate. The load current required from the DC-to-DC converter is the sum of the current consumption of the drive circuit and the average drive current to the gate.

dv/dt CAPABILITY. When the DC-DC converter powers a high side switch, the secondary side of the converter is connected to the output of the power circuit. The rapid change of high voltage at the output of power circuit stresses the isolation of the transformer and injects noise to the primary side of the transformer. Switching noise at the primary side disturbs the operation of the converter and the control circuit for the power stage, causing false triggering and shoot-through. Therefore a transformer with high voltage isolation, appropriate creepage distances and low winding-to-winding capacitance is required in this application.

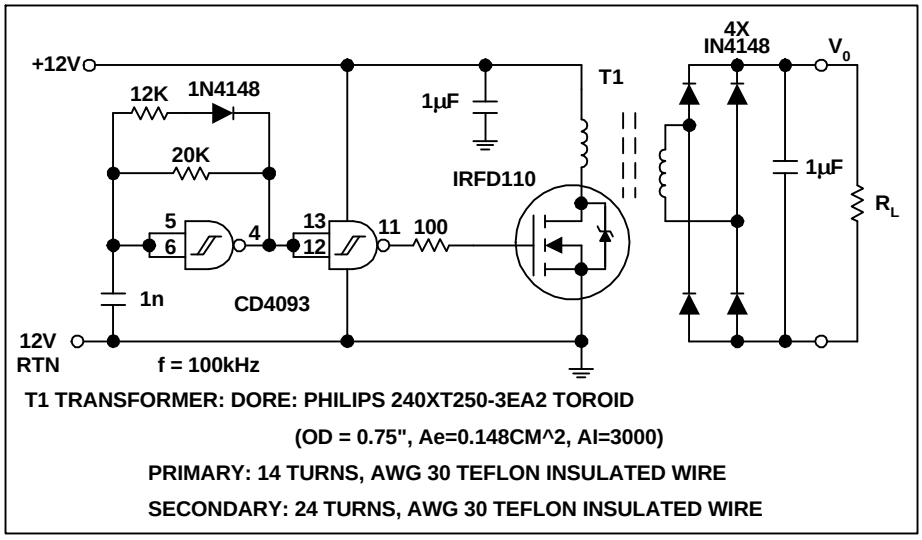

Figure 33a. 100 kHz Forward converter

SMALL SIZE. To reduce the interwinding capacitances the transformer must be made small. This implies operation at high frequency. Small size and compact layout help reducing the EMI and RFI generated by the converter. Figure 33a shows a forward converter made with two CD4093 gates to generate the clock and drive the MOSFET. Energy as transferred to the secondary when the MOSFET is on, in about 33% of the cycle. When the MOSFET is off, the secondary winding is used to demagnetize the transformer and transfer the magnetizing energy to the load, thus eliminating the need for a demagnetizing winding. The switching waveforms are shown in Figure 33b. The ringing in the drain voltage during the fly-back period is due to the loose coupling between the primary and the secondary windings. The load current vs. output voltage characteristic of the circuit is shown in Figure 34. When the output current falls below 5 mA, the circuit works as flyback converter because the demagnetizing current flows through the output. A minimum load of 5mA is required to limit the output voltage at 15V.

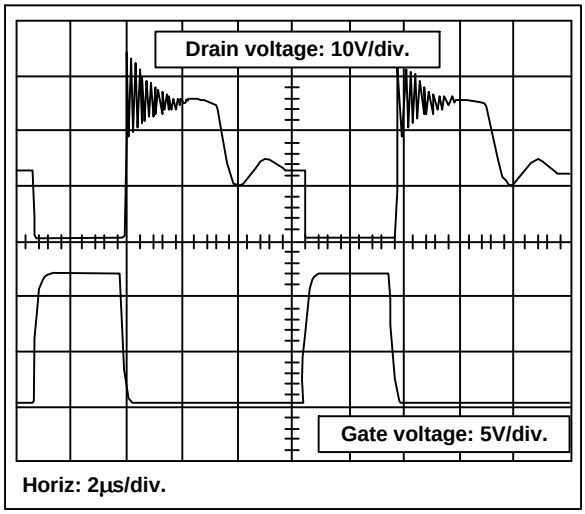

Figure 33b. Waveforms associated with the circuit in Figure 33a

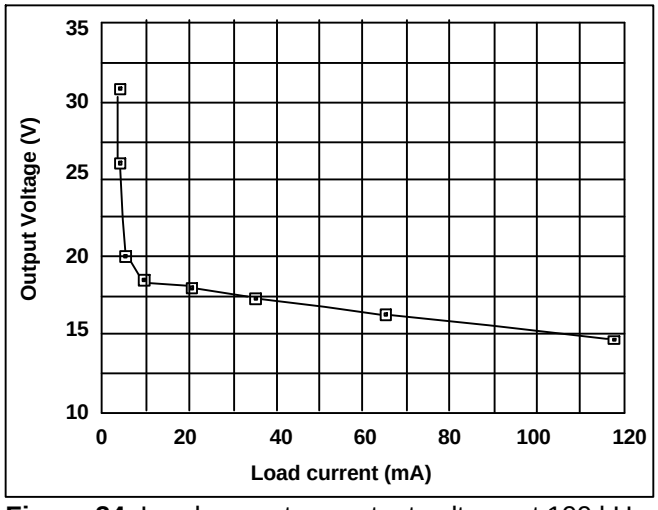

Figure 34. Load current vs. output voltage at 100 kHz, Rout = 27.7 Ohms

If the converter is loaded with a constant and predictable load, a zener can provide the necessary regulation. Otherwise a three-terminal regulator or a small zener-driven MOSFET may be necessary.

The circuit in Figure 35a is similar to the previous one, except that the higher switching frequency is higher (500 kHz) and the transformer is smaller. The remaining three gates in the package are connected in parallel to drive the MOSFET and reduce the switching losses. The switching waveforms are shown in Figure 35b. The output resistance (Rout) of this circuit is higher than the circuit shown in Figure 33a, mainly because the stray inductance of the smaller transformer is higher and the effects of the stray inductance are higher. Figure 37a shows a push-pull operated at 500 kHz. The single gate oscillator produces a 50% duty cycle output, while the remaining gates in the package are used to drive the push-pull output stage. The primary of the transformer sees half the voltage compared to the previous circuit, therefore the number of turns at the primary were reduced to half.

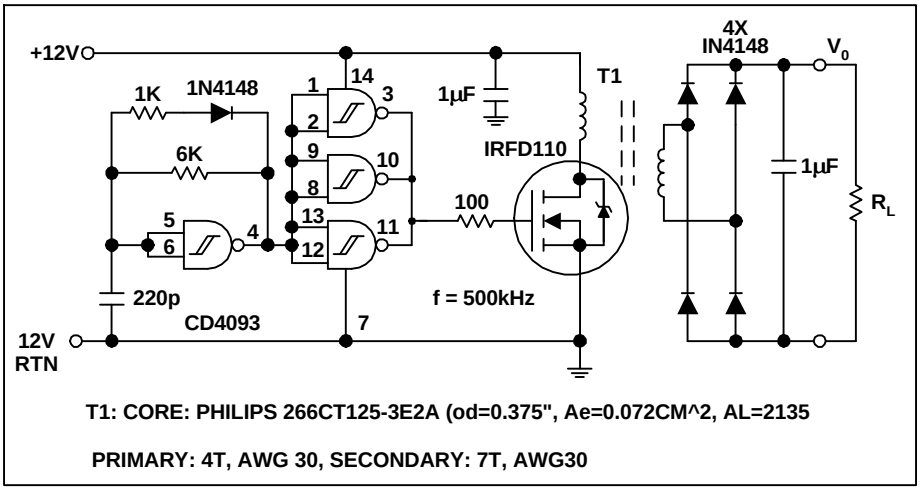

Figure 35a. 500 kHz Forward converter

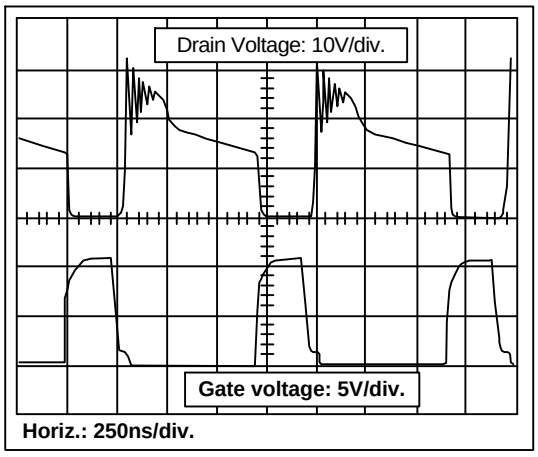

Figure 35b. Waveforms associated with the circuit in Figure 35a

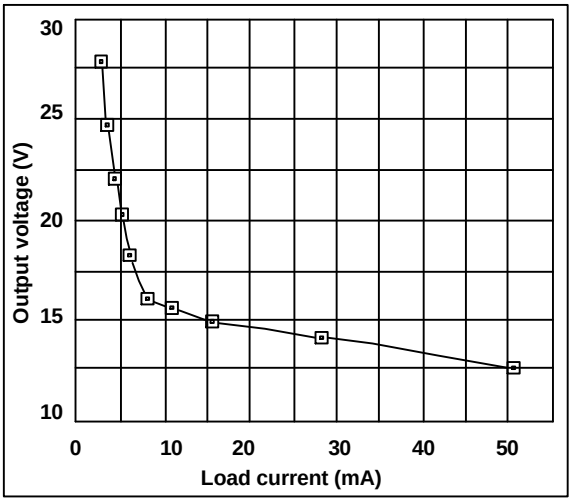

Figure 36. Load current vs. output voltage, Rout = 27.7 Ohms

10. PHOTOVOLTAIC GENERATORS AS GATE DRIVERS

A photovoltaic generator is a solid state power supply powered by light, normally an LED. The combination of the LED and the photovoltaic generator in one package is called a Photovoltaic Isolator or PVI and is available in a 8-pin DIP package. As a voltage source, the PVI can function as a "dc transformer" by providing an isolated low current to a load. While an optoisolator requires a bias supply to transmit a signal across a galvanic barrier, the PVI actually transmits the energy across the barrier. More information on the PVI can be found in Application Note GBAN-PVI-1 which appears in the Microelectronic Relay Designer' s Manual. This data book also contains the data sheet for the photovoltaic isolator, the PVI1050. A circuit is also provided in the AN to significantly speed up turn off of the switch. As a gate driver the PVI has significant limitations: its short circuit current is in the order of 30 microA with a very high internal impedance. Its simplicity, however, makes it appealing in solid-state relay replacements, where switching times are not important and switching transients are not present.

A typical application is the ac switch described below. The IGBT and the power MOSFET are not suited to switching AC waveforms directly. The IGBT can only conduct current in one direction while the power MOSFET has an anti-parallel diode that will conduct during every negative half-cycle. Bidirectional blocking capability can be achieved by connecting two power MOSFETs source to source, or two IGBTs with anti-parallel diodes emitter to emitter, as shown in Figure 39.

In the case of the MOSFET, there is the possibility that, for low current levels, the current flows through both MOSFET channels, instead that one MOSFETs and diode, thereby achieving lower overall voltage drop. The MOSFET channel is a bidirectional switch, that is, it can conduct current in the reverse direction.

If the voltage across the MOSFET channel is less than the VF of the intrinsic diode (which typically has a higher VF than discrete diodes), then the majority of the current will flow through the MOSFET channel instead of the intrinsic diode. The gate drive for both the MOSFETs and IGBTs must be referenced to the common sources or emitters of the devices. Since this node will be swinging with the AC waveform, an isolated drive is necessary. The PVI can be used, as shown in Figure 40.

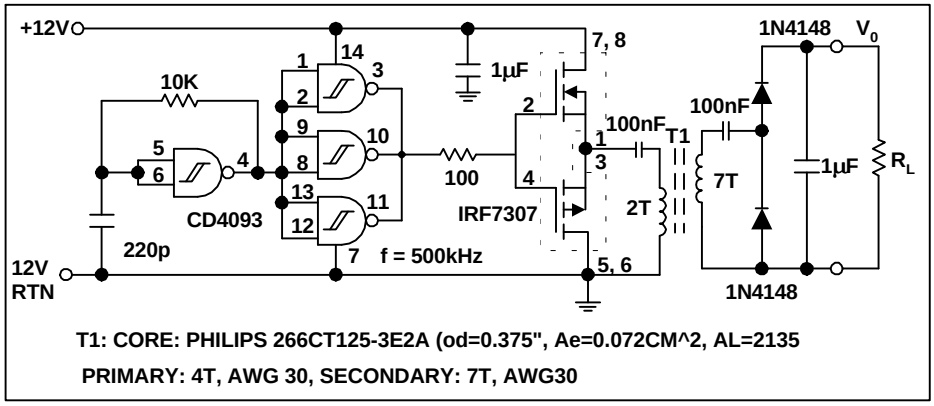

Figure 37a. 500 kHz Forward converter

11. RESONANT GATE DRIVE TECHNIQUES

As indicated in Section 14, gate drive losses in hard switching are equal to Qgs x Vgs x f. An IRF630 operated at 10 Mhz with a gate voltage of 12 V would have *gate drive losses* of 3.6 W, independent from the value of the gate drive resistor. Clearly, to achieve hard switching at this frequency, the resistance of the gate drive circuit is limited to whatever is associated with the internal impedance of the driver and with the gate structure of the device itself. Furthermore, the stray inductance of the gate drive circuit must be limited to tens of nH. The design and layout of such a circuit is not an easy task.

An alternative method to drive the gate in such an application is to design a resonant circuit that makes use of the gate capacitance and stray inductance as its reactive components, adding whatever inductance is necessary to achieve resonance at the desired frequency. This method can reduce the peak of the gate drive current and losses in half, while simplifying the design of the gate drive circuit itself. Since the gate charge is not dissipated at every switching transition, but stored in a reactive component, the gate drive losses are proportional to the resistance of the gate drive circuit, rather than being independent from it. More information on this gate drive method can be found in an article by El-Hamamsy: Design of High-Efficiency RF Class-D Power Amplifier and in references at the end of this article (IEEE Transactions on Power Electronics, May 1994, page 297).

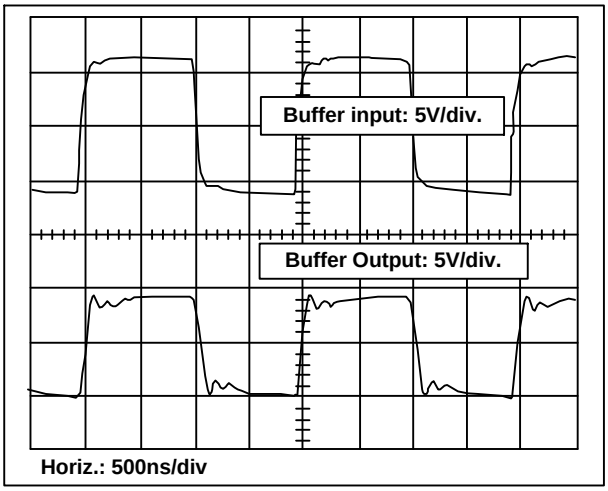

Figure 37b. Waveforms associated with the circuit in Figure 37a

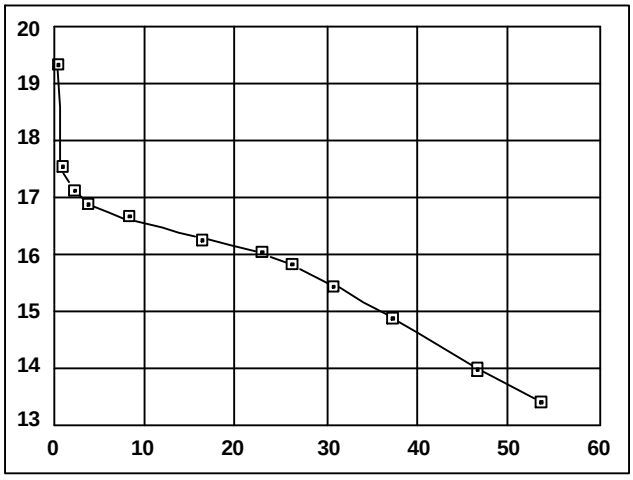

Figure 38. Load current vs. output voltage, Rout=27.7 Ohms

Related Topics

MOS-Gate Driver Ics
Transformer drive with wide duty cycle capability
Gate Charge
Three-phase MOS-Gate Driver
Photovoltaic Isolators (PVI)