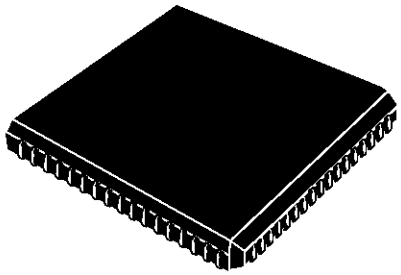
SGS-THOMSON MICROELECTRONICS

W.A.R.P.2.0

8-BIT FUZZY CO-PROCESSOR

PRELIMINARY DATA

- Digital Fuzzy Co-processor 8-bit I/O
- High Speed Rules Processing
  4 Input, 2 Output, 32 Rules in 33.1µs
- Up to 256 Rules (4 Antecedents, 1 Consequent)
- Up to 8 Input Configurable Variables
- Up to 16 Membership Functions for an Input Variable
- Antecedent Membership Functions with Triangular and Trapezoidal Shape
- Up to 4 Output Variables
- Up to 256 Membership Functions for all Consequents
- Singleton Consequent Membership Functions
- Defuzzification on chip
- Maximum Clock Frequency 40MHz
- A/D Start Convertion Pulse presettable
- Direct Interface to all popular microprocessor
- Handshaking Signal Polarity presettable
- Operates "STAND ALONE" (without µP) if desired
- Standard +5V Supply Voltage
- Software Tools and Emulators Availability
- Pin number: 52
- 68-lead Plastic Leaded Chip Carrier package.



PLCC68

Figure 1. Logic Diagram.

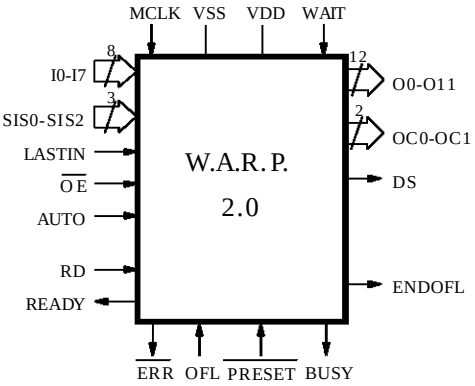


Figure 2. Simplified Block Diagram.

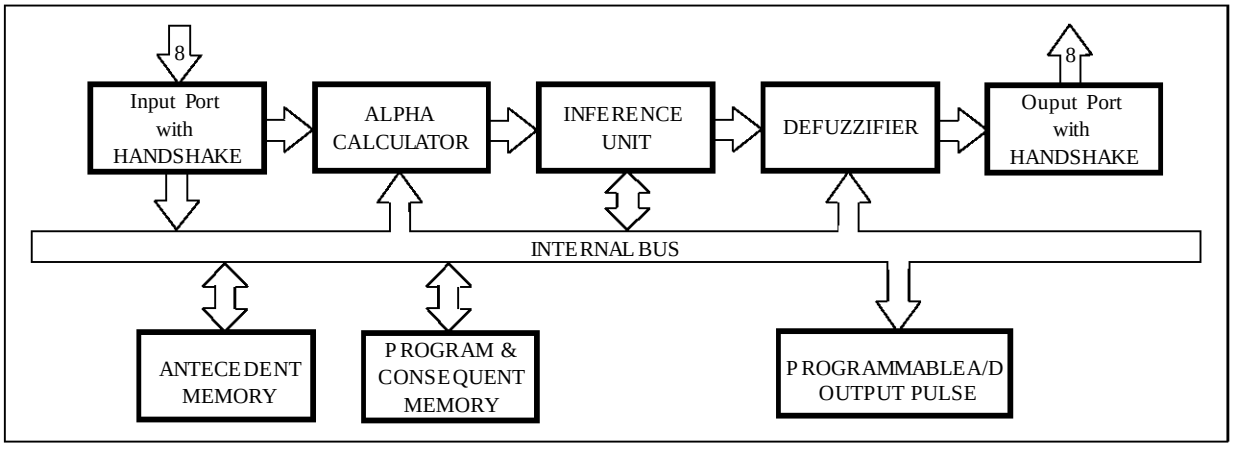
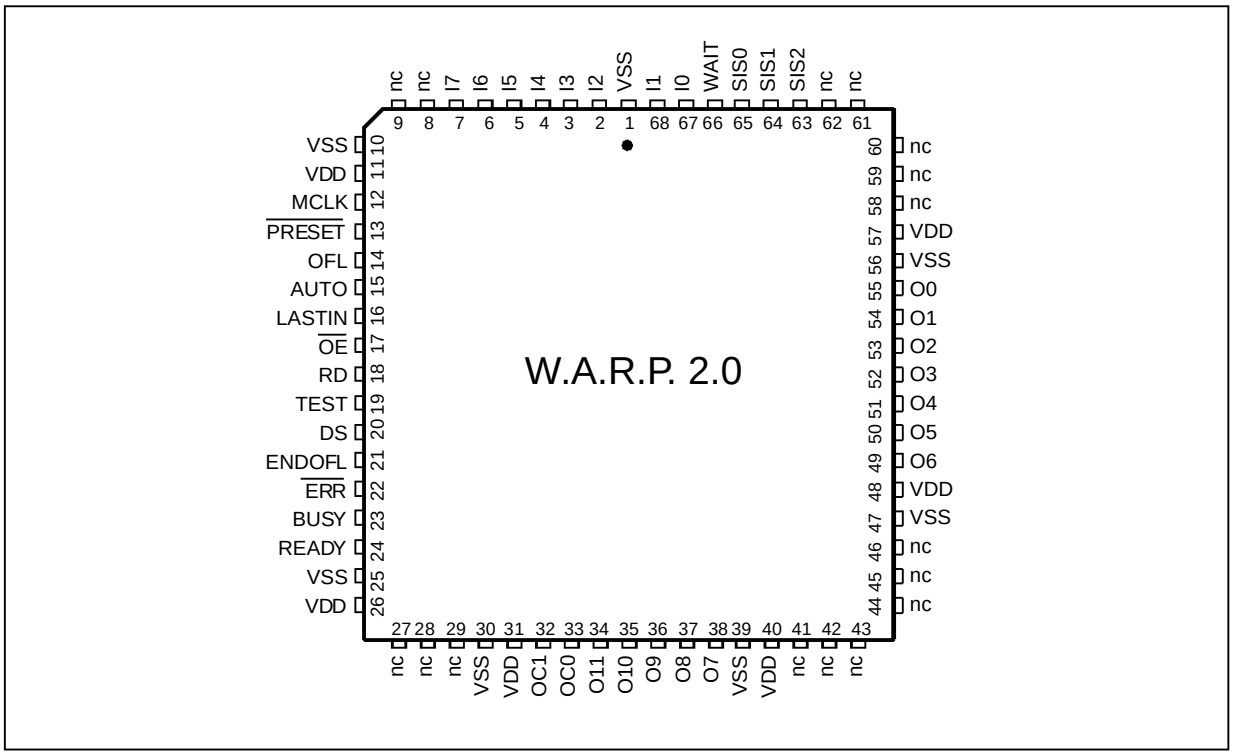


Figure 3. Pin Connections



Note: nc = Not Connected.

GENERAL DESCRIPTION

W.A.R.P.2.0 is a member of the W.A.R.P. family of fuzzy microprocessors, completely developed and produced by SGS-THOMSON Microelectronics using the high performance, reliable HCMOS4T (O.7µm) process.

W.A.R.P.2.0 can be used both as a Fuzzy Co-processor or as a stand-alone microcontroller. In the former case, it can work together with standard micros which shall perform normal control tasks while W.A.R.P.2.0 will be indipendently responsible for all the fuzzy related computing.

W.A.R.P.2.0 core includes the fuzzifier (ALPHA calculator), the inference unit, and the defuzzifier. The I/O capabilities demanded by microprocessor applications are fulfilled by W.A.R.P.2.0 with 8 Input and 4 Output lines which can be supported by handshaking signals.

The capability of preset the polarity of the handshaking signals simplifies the interface with the host processor.

An internal Start Conversion pulse is provided to allow simple use for waveform generation which can be directly applied to drive an A/D converter.

The output 3-STATE buffer can be temporarily frozen in order to synchronize W.A.R.P.2.0 with slower devices.

Running W.A.R.P.2.0 involves a downloading phase and an On-Line phase. The downloading phase allows the setting of the processor, in terms of I/O number, universe of discourse, Membership Functions (MFs) and rules. During this phase W.A.R.P.2.0 prepares its internal memories for the On-Line elaboration phase and loads the microcode in its program memory. This microcode, which drives the On-Line phase, is generated by the Compiler (see FUZZYSTUDIO™ 2.0 User Manual). After that W.A.R.P.2.0 is ready to run (On-Line phase) processing inputs and producing the related outputs according to the configuration loaded in the downloading phase. It is also possible to provide the processor with inputs in any order by specifying their identification numbers.

Two basic memories are available in W.A.R.P.2.0 : the Antecedent Memory (AM) and the Program/Consequent Memory (PCM). The antecedent MFs, portrayed by a resolution of 2^8 elements, are stored in the AM (256 bytes). W.A.R.P.2.0 exploits a SGS-THOMSON patented strategy to store the MFs in the AM.

The information about Rules and Consequent MFs are stored in the PCM (1.4 Kbyte).

FUZZYSTUDIO™ 2.0 is a powerful development environment consisting of board and software allows an easy configuration and use of W.A.R.P.2.0.

Table 1. Pin Description

Pin Assignment	Name	Pins Type	Function
11,26,31,40,48,57	VDD	-	Power Supply
1,10,25,30,39,47,56	VSS	-	Ground
19	TEST	I	Testing (It must be connected to VSS)
12	MCLK	I	Master Clock (up to 40 MHz)
13	$\overline{\text{PRESET}}$	I	Preset
15	AUTO	I	Auto/Manual-Boot
65	SIS0	I	Auto-Boot Speed (Ext. Memory Support AccessTime) / Input Selection bit 0
64	SIS1	I	Auto-Boot Speed (Ext. Memory Support Access Time) / Input Selection bit 1
63	SIS2	I	Auto-Boot Speed (Ext. Memory Support Access Time) / Input Selection bit 2
67	I0	I	Data Input bit 0
68	I1	I	Data Input bit 1
2	I2	I	Data Input bit 2
3	I3	I	Data Input bit 3
4	I4	I	Data Input bit 4
5	I5	I	Data Input bit 5
6	I6	I	Data Input bit 6
7	I7	I	Data Input bit 7
14	OFL	I	Off-Line/On-Line Switch
18	RD	I	Handshaking Read Ready
16	LASTIN	I	Last Input (Start Elaboration) bit
17	$\overline{\text{OE}}$	I	Output Enable/3-STATE bit
66	WAIT	I	Temporary Output Processing Stop
24	READY	O	Handshaking Output Signal
21	ENDOFL	O	Offline Phase (external memory downloading) End
23	BUSY	O	Elaboration Phase Indicator
20	DS	O	Data Strobe (Output Ready Signal)
22	$\overline{\text{ERR}}$	O	Error Flag
33	OC0	O	Output Identifier bit 0
32	OC1	O	Output Identifier bit 1
55	O0	O	External Memory Address/Defuzzified Output bit 0
54	O1	O	External Memory Address/Defuzzified Output bit 1
53	O2	O	External Memory Address/Defuzzified Output bit 2
52	O3	O	External Memory Address/Defuzzified Output bit 3
51	O4	O	External Memory Address/Defuzzified Output bit 4
50	O5	O	External Memory Address/Defuzzified Output bit 5
49	O6	O	External Memory Address/Defuzzified Output bit 6
38	O7	O	External Memory Address/Defuzzified Output bit 7
37	O8	O	External Memory Address bit 8 / Next Input Progressive Number bit 0
36	O9	O	External Memory Address bit 9 / Next Input Progressive Number bit 1
35	O10	O	External Memory Address bit 10 / Next Input Progressive Number bit 2
34	O11	O	External Memory Address bit 11 / Start Conversion for the external A/D

PIN DESCRIPTION

Signals READY, RD, WAIT, DS, BUSY, LASTIN and O11 (external A/D Start Conversion) have programmable polarity, see table 6 for default values.

V_{DD}, V_{SS}. Power is supplied to W.A.R.P. using these pins. V_{DD} is the power connection and V_{SS} is the ground connection; multi-connections are necessary.

MCLK. *Master Clock* (Input)**:** This is the input master clock whose frequency can reach up to 40MHz (MAX).
During the Off-Line phase with AUTO **High**, the MCLK is internally divided to utilize boot memories working with a slower frequency. The access speed is presettable by means of SIS0-SIS2 pins.

~~PRESET~~. *Preset* (Input, active Low) **:** This is the restart pin of W.A.R.P.. It is possible to restart the work during the computation (On-Line phase) or before the writing of internal memories (Off-Line phase). In both cases it must be put **Low** at least for a clock period. After ~~PRESET~~ **Low** the processor remains in the reset status 3 MCLK pulses.

AUTO. *Auto-Boot:* (Input, active High)**:** During the Off-Line phase AUTO **High** enables the automatic boot of W.A.R.P.2.0 whereas AUTO **Low** validates the manual downloading. The manual boot has to be performed using the handshaking signals RD/READY.
During the On-Line phase AUTO **High** disables the generation of the Start A/D conversion (O11) signal.

SIS0-SIS2. *Speed & Input Selection* (Inputs): During the Off-Line phase with AUTO **High** (Auto-Boot) SIS bus allows to choose the speed of downloading from the external memory which contains the start-up configuration of W.A.R.P.2.0. In that case (Auto-Boot) MCLK is internally divided to provide a slower sinchronization signal which is automatically used as RD for the reading of the external memory. Table 2 shows how to preset the frequency of this synchronization signal.
During the On-Line phase in Slave mode (see Register Bench description, Tab.5) SIS bus allows to provide W.A.R.P.2.0 with inputs in any order by specifying their identification number. The input and its identification number (SIS0-SIS2) will be acquired at the next active RD so they must be already stable when RD is given.

Table 2. Downloading Speed

SIS0	SIS1	SIS2	Internal Synchronization Signal Frequency
Low	Low	Low	MCLK/32
High	Low	Low	MCLK/16

I0-I7. *Input bus* (Input)**:** During the Off-Line phase these 8 data input pins accept addresses and data from the external boot memory containing W.A.R.P.2.0 configuration. This start-up memory (which can be a ZERO-POWER, the host processor memory, an EPROM, a Flash, the PC Memory, etc.) contains the fuzzy project built by means of FUZZYSTUDIO™ 2.0.
In On-Line mode this bus carries the input variables according to the prefixed order.

OFL. *Offline* (Input, active High)**:** When this pin is **High**, the chip is enabled to load data in the internal RAMs (Off-Line phase). It must be **Low** when the fuzzy controller is waiting for input values and during the processing phase (On-Line phase).
When OFL changes its status the processor remains presetted for 3 clock pulses.

LASTIN. *Last Input* (Input, default active High): During the On-Line phase in slave mode (see Register Bench description, table 5) LASTIN **High** indicates no other inputs have to be provided so W.A.R.P.2.0 can start the processing phase.
W.A.R.P.2.0 inputs are those in the input interface so if some variables do not need to be acquired again (because they change slower than others) they remain stored and no extra time is required to acquire them again.

$\overline{OE}$. *Output Enable* (Input, active Low): $\overline{OE}$ **Low** enables O0-011output bus or (if **High**) put it in 3-STATE.

WAIT. *Wait* (Input, default active High): This pin **High** stops the output processing. When WAIT is enabled W.A.R.P.2.0 finishes to compute the current output variable but it does not give it on the output bus until WAIT becomes **Low**. This signal allows to synchronize W.A.R.P.2.0 with slower devices.

RD. *Read* (Input, default active High): Both in Off-Line and in On-Line mode RD indicates data are ready to be acquired from the input bus I0-I7.

READY. *Ready* (Output, default active High): Both in Off-Line and in On-Line mode RD indicates data have been acquired from the input bus I0-I7 and are now stored in W.A.R.P.2.0 internal registers.

ENDOFL. *End of Off-Line phase* (Output, active High): This pin indicates the end of the downloading phase (Off-Line) so the content of the boot memory is already stored in W.A.R.P.2.0 internal memories. After ENDOFL is active the user can put OFL **Low** so the On-Line phase can start.

BUSY. *Busy Signal* (Output, default active High): When the elaboration phase is running this pin is active. When W.A.R.P.2.0 finishes to compute the last output variable, it puts BUSY **Low** and waits for new inputs.

DS. *Data Strobe* (Output, default active High): The strobe pin enables the user to utilize the output. When this pin is **High** it indicates that a new output variable has been calculated and it is ready on the output bus (O0-O7). This signal synchronizes the external devices and in particular the interfaces with the controlled processes (On-Line mode).

ERR. *Error* (Output, active Low): When this pin is active, W.A.R.P.2.0 has incurred in an internal error condition.

OC0-OC1. *Output Counter* (Output)**:** This 2 bit output bus provides the output variables with a progressive number during the On-Line phase. As a consequence it is possible to know to which variable correspond the data that are on the output data bus (O0-O7). The dimension of OC bus is connected with the maximum number of output variables (4).

O0-O11. *Output Bus* (Output): In the Off-Line phase these pins provide the addresses (12 bit) for its internal memories and send those addresses to the external memory support where data to load are located. These addresses sent on O0-O11 bus allow to identify the data that have to be loaded in W.A.R.P.2.0 internal memories.
In the On-Line phase O0-O7 carrie out the output values. When the DS is **High**, one output variable can be read by external devices. The resolution of output variables is 256 points (8 bit). If there is more than one output, the output variables are calculated one by one and they are provided in the sequence stabilized during the editing phase (see FUZZYSTUDIO™ 2.0 User Manual).

In On-Line mode O8-O10 provide the progressive number of the next variable to be acquired. These pins can be used to select the next input to provide on I0-I7 bus.

Still in on-line mode O11 allows to provide a preset-table signal which can be used as Start-Conversion for an A/D converter after (about 400 ns) OFL or BUSY fall.

FUNCTIONAL DESCRIPTION

W.A.R.P.2.0 works in two mode depending on the OFL control signal level (see table 3) :

Off-line MODE (OFL High)

On-line MODE (OFL Low)

OFF-LINE MODE

All W.A.R.P. memories are loaded during the Off-Line phase. The membership functions are written inside their related memories and the process control rules are loaded inside the PCM.
The addresses of the words to be written in the memories, are internally generated while the addresses of the external memory locations to be read are directly provided by W.A.R.P.2.0 by means of O0-O11 output pins.
Data must be loaded 8 bit a time in the data bus and can be read from an external non volatile memory or loaded by an host processor.

The Off-Line phase can be performed automatically (see figure 4) or manually (see figure 5).
When the auto-boot is chosen (AUTO = High) it is possible to configure the reading access time of the external memory. The auto-boot end is indicated by the ENDOFL signal.
The downloading phase requires:

F*NWordsDatabase clock pulses,

where F is 16 or 32 (see table 2).

NWordsDatabase is the number of words stored in the boot-memory (see register bench description, table 5).

When the manual-boot is chosen (AUTO = Low) data have to be provided by using the handshaking signals (RD/READY). In this way it is possible to update only a portion of the database or change the processor configuration.

The time required from the manual boot depends on the efficiency of the communication handled with the handshaking signals.

Figure 4. Off-Line phase: Auto-Boot

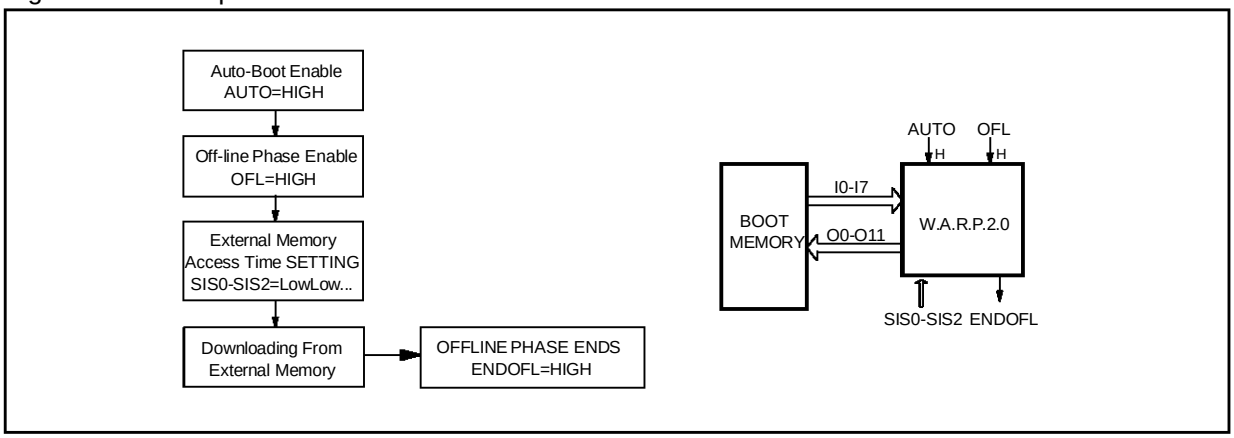
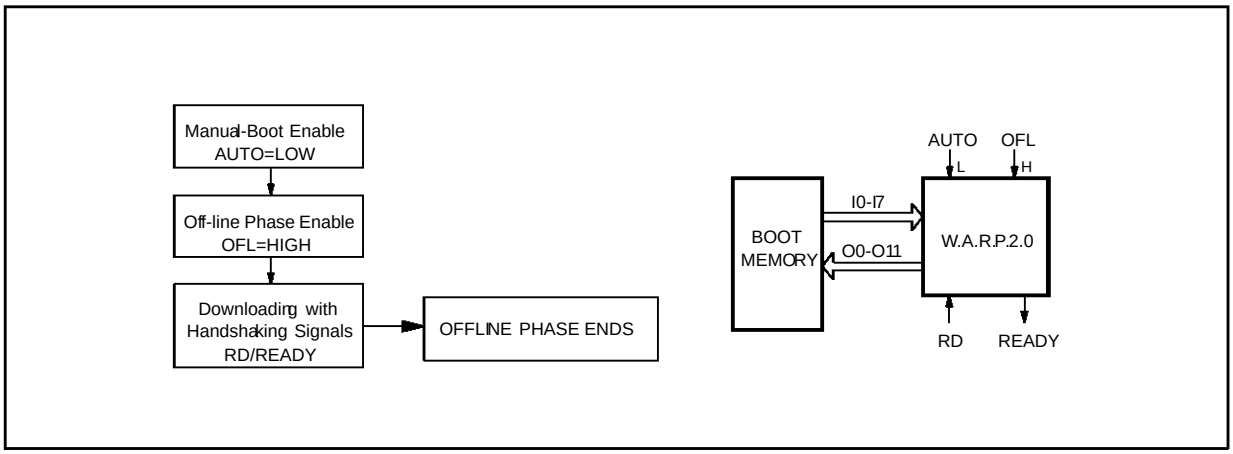


Figure 5. Off-Line Phase: Slave Downloading



ON-LINE MODE

In On-line mode (see figure 7) W.A.R.P.2.0 is enabled to elaborate input values and calculate outputs according to the fuzzy rules stored into the microprogram. W.A.R.P.2.0 reads the input values one a time in the input data bus using the RD/READY signals. If the processor is working in SLAVE mode (see register bench description in table 5) the user has to provide the inputs with their identification numbers (by means of SIS0-SIS2), so it is possible to provide inputs in any order. In SLAVE mode it is also possible to force W.A.R.P.2.0 to start the elaboration phase (by means of LASTIN) without providing all inputs, for instance when input variables change with different speed. In this case the outputs that have not be provided in this cycle, but sampled in the previous ones, are recovered from the internal buffers.

When all inputs are given or a LASTIN signal is given, the elaboration phase starts. The elaboration phase is divided in two main parts. During the first one the input values are read and the corresponding ALPHA values (activation levels) are calculated. In the second part the computation of the fuzzy rules and the defuzzification are implemented.

W.A.R.P.2.0 acquires each input in 8 clock pulses (min). Since the acquisition phase is performed by the user by means of the handshaking signals, 8 clock pulses per input are referred to the most efficient case. In figure 6 are shown the performances in case of 8 inputs. If you are using less inputs you have to subtract 8 clock pulses for each of them. The elaboration time for rule requires 32 clock pulses.

For instance if W.A.R.P.2.0 is working at a frequency of 40 MHz (25ns period) with 8 inputs and 128 rules globally (for all outputs) the time required to provide all outputs is 4000clkp*25ns = 100µs.

Figure 6. W.A.R.P.2.0 performances

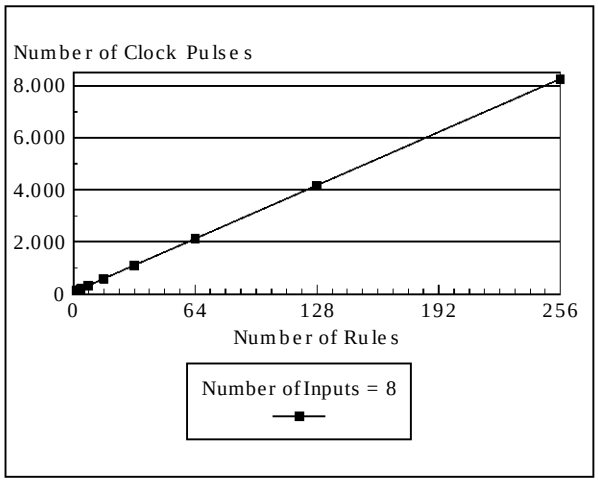


Figure 7. On-Line phase

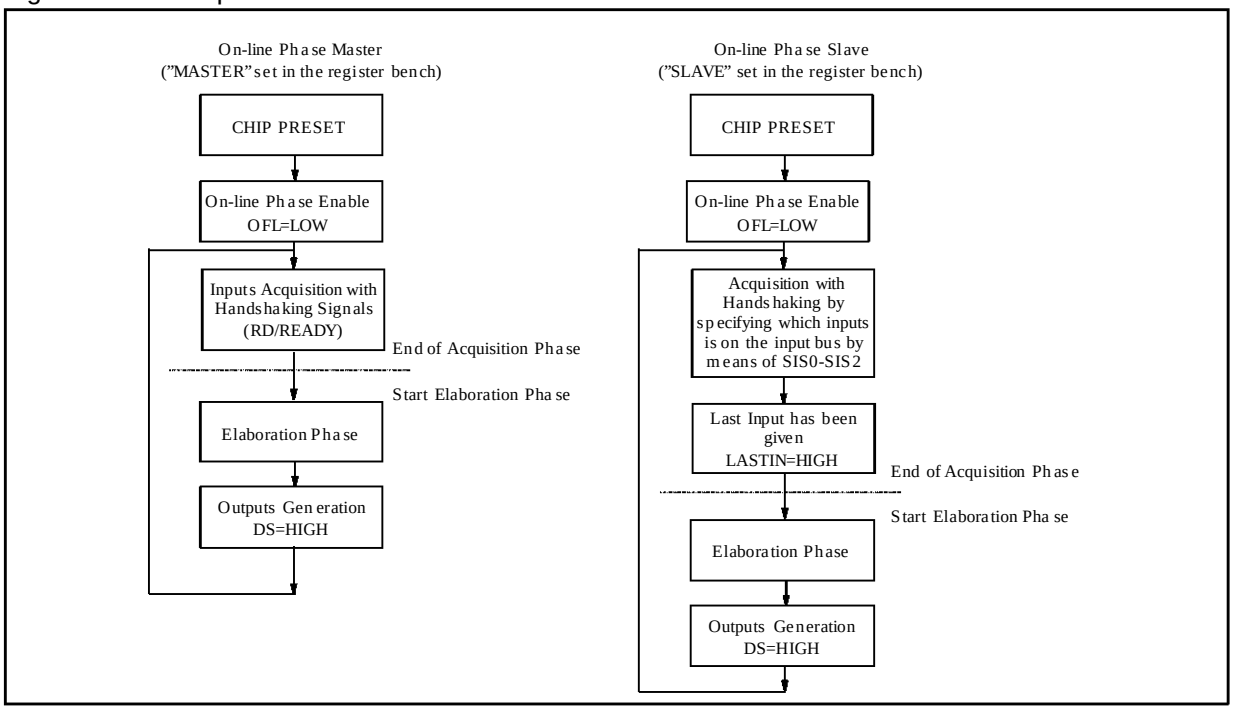
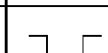


Table 3. Operating Modes (1)

Mode	$\overline{PRESET}$	OFL	AUTO	$\overline{OE}$	I0-I7	RD	SIS0-SIS2	O0-O7	O8-O10	O11	OC0-OC1
Off-Line Slave	V_{IH}	V_{IH}	V_{IL}	X	Data In		X	X	X	X	X
Off-Line Autoboot	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Data In	X	Clock Rate Selection Code	External Memory Addresses			X
On-Line Master(2)	V_{IH}	V_{IL}	X(2)	V_{IH}	Data In		X	Data Out	Next Input	 (2)	Output Selection
On-Line Slave(3)	V_{IH}	V_{IL}	X(2)	V_{IH}	Data In		Input Selection	Data Out	X	 (2)	Output Selection
Output Disable	V_{IH}	X	X	V_{IL}	X	X	X	Hi-Z			X
Reset(4)		X	X	X	X	X	X	V_{OL}	V_{OL}	V_{OL}	V_{OL}

Notes: 1. This table uses default active handshaking signal polarity (see table 6), X = don't care.

2. If AUTO is High pulse in O11 is absent.

3. LASTIN and WAIT pulses are optional.

4. Same operation is obtained when positive and negative OFL transactions occour.

INTERNAL STRUCTURE

The block diagram shown in figure 2 describes the structure of W.A.R.P.2.0 (a more detailed block diagram is shown in fig. 11).

Input Port. This internal block performs the input data routing. Data are read one byte a time from the input data bus, internally stored, and sent to the ALPHA calculator following the rules loaded in the Program Memory. Input data resolution is 8 bit.
The cycle starts when all inputs or a LASTIN High have been provided and continues until BUSY is active or a $\overline{PRESET}$ signal is given. When BUSY becomes inactive a new acquisition phase can start.

Alpha Calculator. This block calculates the intersection (ALPHA weight) between an Antecedent Membership Function and the corresponding crisp input (see figure 8).

Inference Unit. Thanks to the Theta Operator, the Inference Unit generates the THETA weights which are used to manipulate the consequent MFs.

This is a calculation of the maximum and/or minimum performed on ALPHA values according to the logical connectives of fuzzy rules. It is possible to utilize the AND/OR connectives and to directly exploit ALPHA weights or the negated values. The number of THETA weights depends on the number of rules.

The rules can have at maximum four ALPHA weights (however they are connected). Two or more rules can be only joined with the OR connective. Inference Unit structure is shown in figure 9.

Defuzzifier. It generates the output crisp values implementing the consequent part of the rules.

In this method consequent MFs are multiplied by a weight value Ω (OMEGA), which is calculated on the basis of antecedent MFs and logical operators.

The processing of fuzzy rules produces, for each output variable, a resulting membership function. Each MF related to the processed output variable is firstly modified by a rule weight.

Output value (Y) is deduced from the centroids (X_i) and the modified MFs (Ω_i) by using the formula:

$$Y = \frac{\sum_{1}^{n} \Omega_i * X_i}{\sum_{1}^{n} \Omega_i}$$

n = number of MFs of the Output Variable.

X_i =absciss of the MF_i centroid.

Ω_i =membership degree of the output MF_i.

Two parallel blocks calculate the numerator and denominator values to implement the centroids formula. A final division block calculates the output values (see figure 10).

Output Port. This block provides the output data supported by handshaking signals. Ouput data resolution is 8 bit.
An output ready on the bus O0-O7 is indicated by a DS pulse and by its identification number (OC0-OC1). WAIT active temporarily stops the elaboration phase allowing the synchronization with slower devices.

Programmable A/D output pulse. This block allows to program the width of the pulse provided on O11 (only in On-Line mode) that can be used as a Start Conversion for an external A/D. The width of this pulse can be configured by means of the related register (see register bench description) following the table 4.

Table 4. Start Conversion Pulse (O11) Width Setting.

Start conversion Pulse Register	Pulse Width (T_{CLK} = MCLK Period)
Low, Low, Low	$128xT_{CLK}$
Low, Low, High	$256xT_{CLK}$
Low, High, Low	$2040xT_{CLK}$
Low, High, High	$4080xT_{CLK}$
High, Low, Low	$8160xT_{CLK}$
High, Low, High	$16320xT_{CLK}$
High, High, Low	$32000xT_{CLK}$
High, High, High	$65520xT_{CLK}$

Figure 8. ALPHA Calculator Structure

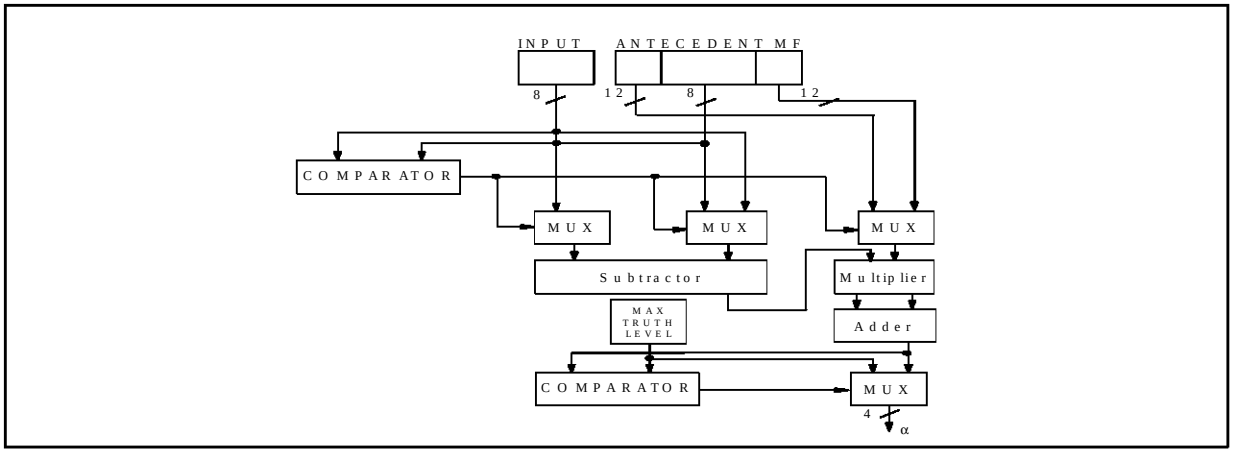


Figure 9. Inference Unit Structure

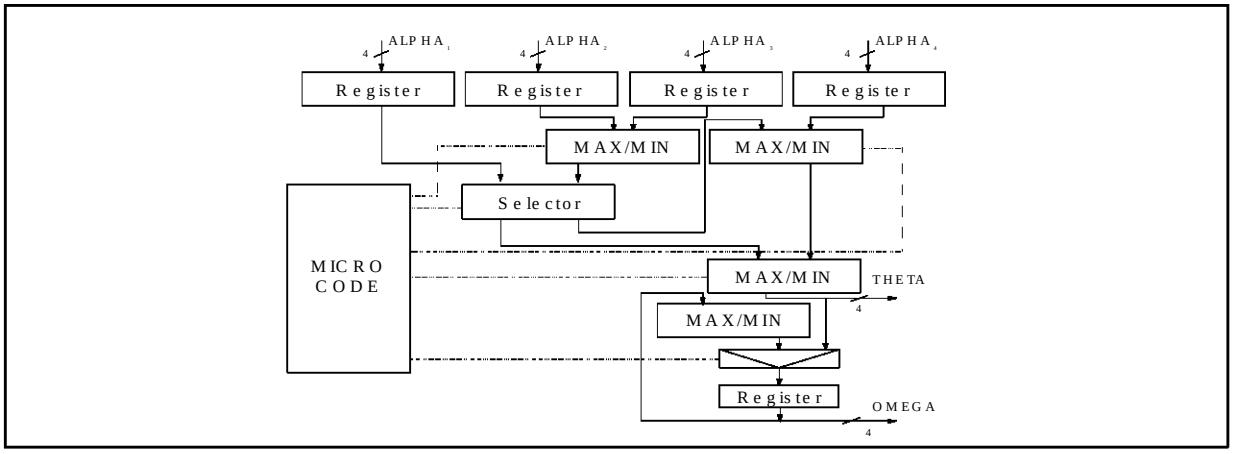


Figure 10. Defuzzifier Structure.

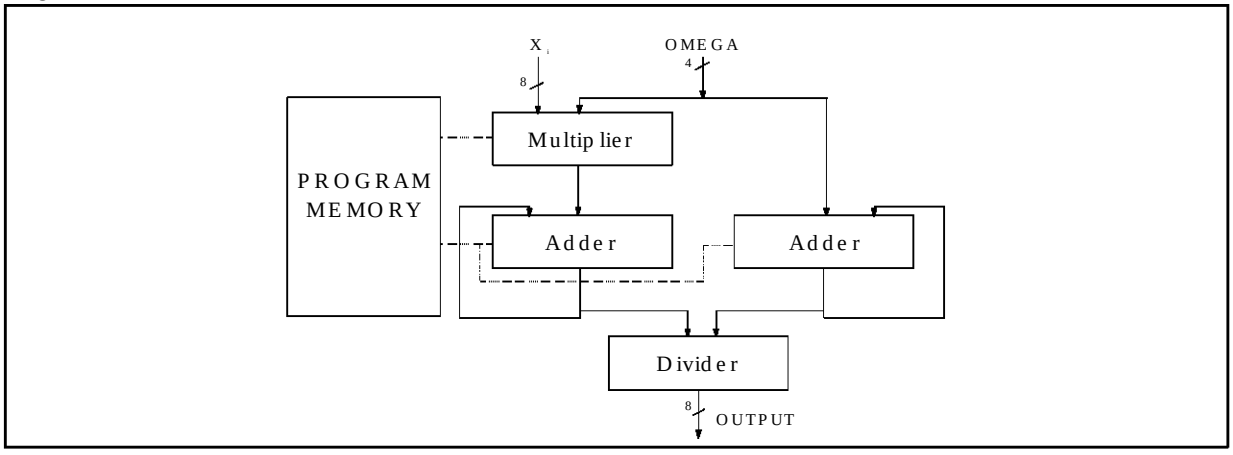
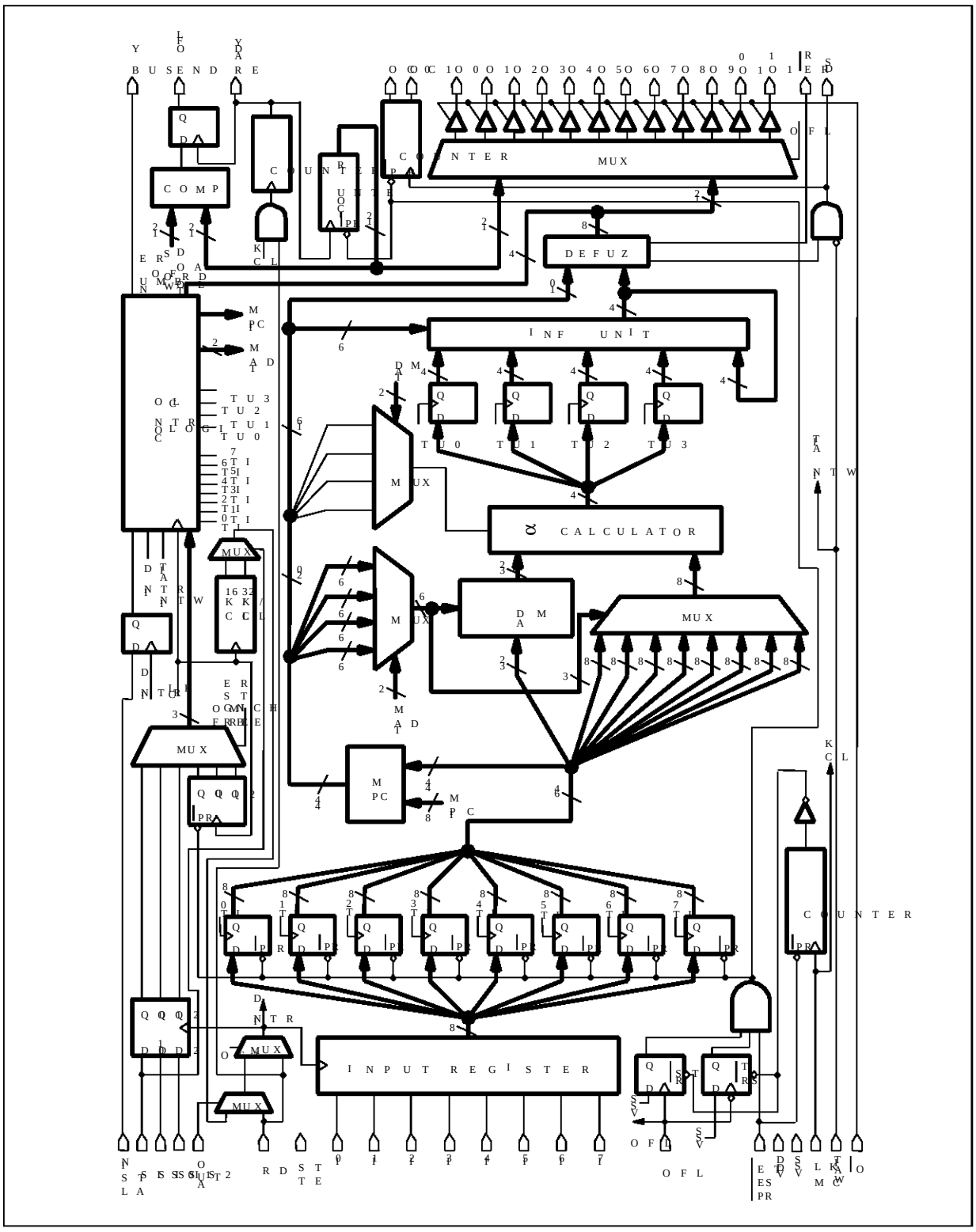


Figure 11. Detailed Block Diagram



MEMORY

There are three memories in W.A.R.P.2.0, the Antecedent Memory (AM), The Program/Consequent Memory (PCM) and the Register Bench (RB).
The AM is divided in 4 spaces, each having a maximum of 64 bytes. It is also possible to divide the AM in 8 parts, each having a maximum of 32 bytes.

It is possible to configure the AM in the following modes (see fig. 12):

a) up to 4 inputs, each with 16 Antecedent MFs (MAX);

b) up to 8 inputs, each with 8 Antecedent MFs (MAX);

Each word (4 byte) of the AM contains the data of a single MF related to an input. If W.A.R.P.2.0 has been configured to accept up to 4 inputs it is possible to have up to 16 MFs for each input. If W.A.R.P.2.0 has been configured to accept up to 8 inputs it is possible to have up to 8 MFs for each input. Each MF of the AM contains 3 (or 2) bit indicating to which input variable the MF is correlated.

The PCM is composed by 256 words (see fig. 13).

Each row (word) is related to a single rule and contains 36 bit of microcode and 8 bit indicating the consequent MF (crisp) related to this rule.

The RB contains data for the configuration of the processor that can be set by software.
It is possible to fix:
the number of inputs, the number of outputs, the address of the last word to load from the external memory, the number of MF per input, the width of the start A/D conversion pulse, the handshaking signals polarity and the functioning mode of the processor (Master/Slave).

Figure 12. Antecedent Memory Spaces.

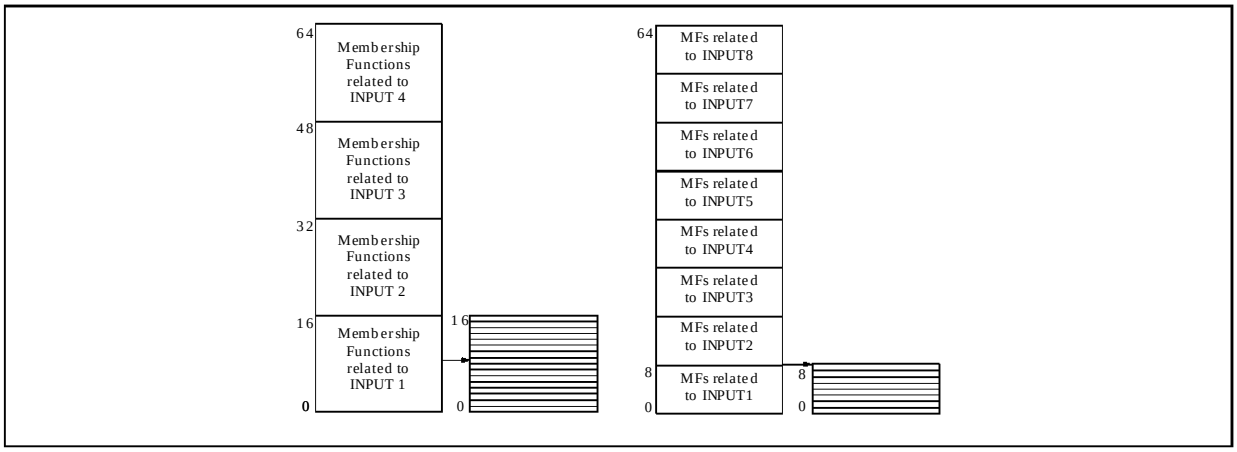


Figure 13. Program/Consequent Memory and Register Bench.

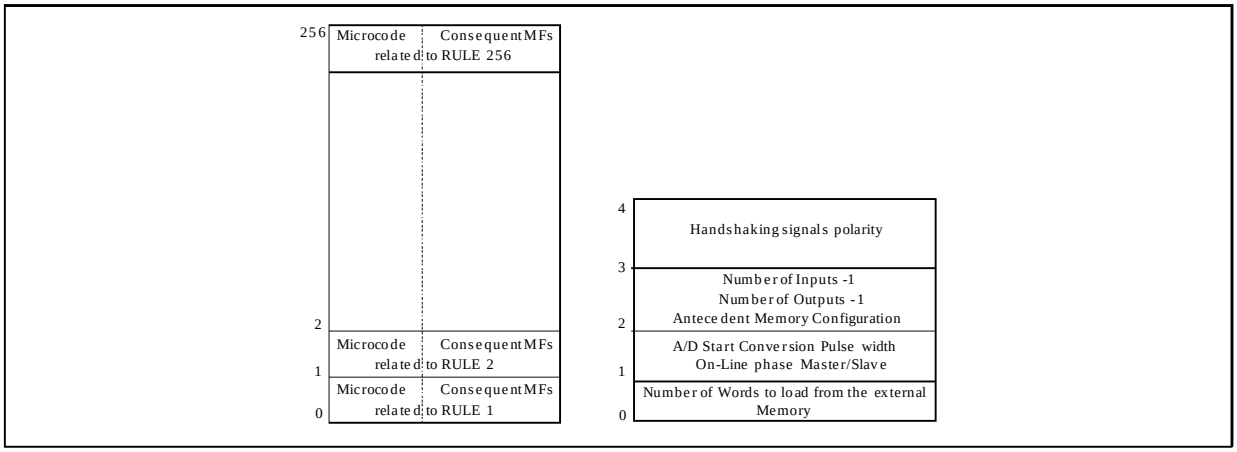


Table 5. Register Bench Description.

Register Name	Resolution	Function
Handshaking Signal Polarity (ONLY during the On-Line Phase)	8	0 active Low, 1 active High (default) bit 0 READY bit 1 RD bit 2 WAIT bit 3 DS bit 4 BUSY bit 5 LASTIN bit 6 not connected bit 7 START CONVERSION
Number of Inputs - 1	3	000-111 = 1 to 8 Inputs
Number of Outputs - 1	2	00 - 11 = 1 to 4 Outputs
Antecedent Memory Configuration	1	0 = 8 Inputs, 8 MFs per Input 1 = 4 Inputs, 16 MFs per Input
A/D Conversion Pulse Width	3	see table 4
On-Line Phase Master/Slave	1	0 = Slave Functioning 1 = Master Functioning
Number of Words to load from the External Memory	12	0000000000000-100110000100 from 0 to 2436 words to read

Note: These Registers are configurable by means of the FUZZYSTUDIO™ 2.0.

Table 6. Default Active Handshaking Signal Polarity

READY	RD	WAIT	DS	BUSY	LASTIN	START C ONVERSION (O11)
High	High	High	High	High	High	High

Note: Default polarities are used in the following timing diagrams

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to 7	V
I_{DD}	Supply Current	50	mA
I_{OL}	Output Sink Peak Current	+24	mA
I_{OH}	Output Source Peak Current	-12	mA
T_{OPT}	Operating Temperature	0 to +70	°C

Note: Stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 7. Recommended Operation Conditions (1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
V_I	Input Voltage	0		V_{DD}	V
V_O	Ouput Voltage	0		V_{DD}	V
t_{IR} (2)	Input Rise Time			40	ns
t_{IF} (2)	Input Fall Time			40	ns

Notes: 1. Operating Condition: V_{DD}=5V±5%-T_A=0 °C to 70 °C, unless otherwise specified.
2. See fig. 22.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V±5% T_A = 0 to +70 °C unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage			0.2	0.4	V
V_{OH}	High Level Output Voltage		2.4	3.4		V
V_{T+}	Schmitt trig. +ve Threshold	see fig. 14		0.8		V
V_{T-}	Schmitt trig. - ve Threshold	see fig. 14		2.0		V
I_{IL} (1)	Low Level Leakage Input Current	V_I=V_{SS} (3)		-1	-2	nA
I_{IH} (1)	High Level Leakage Input Current	V_I=V_{DD} (3)		+4		nA
I_{IL} (2)	Low Level Input Current	V_I=V_{SS} (3)			100	nA
I_{IH} (2)	High Level Input Current	V_I=V_{DD} (3)			160	µA
I_{OL}	Tri-State Output Leakage Current	V_O=V_{SS} or V_{DD}			±10	µA

Notes: 1. All inputs with the except of $\overline{OE}$ and TEST.
2. Only $\overline{OE}$ and TEST inputs.
3. I_{OH} = -400µA, I_{OL} = +16mA, T = +25°C.

Figure 14. TTL-level input Schmitt trigger characteristic.

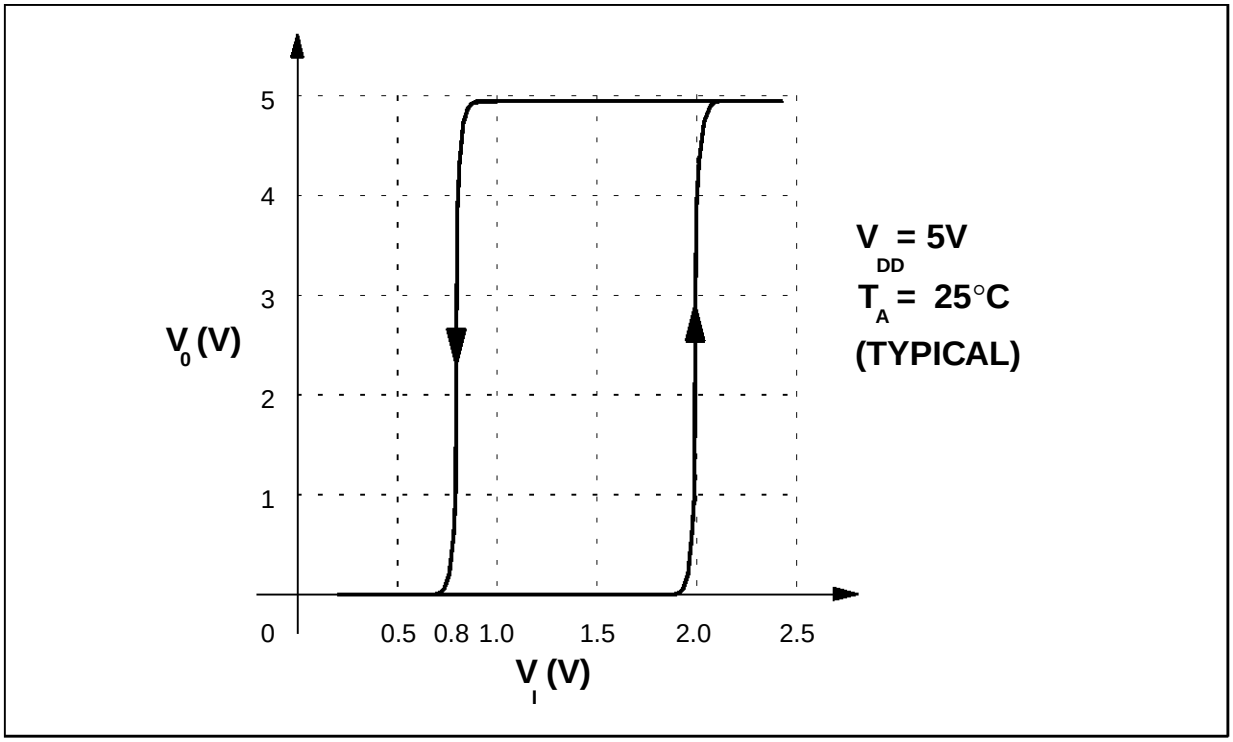
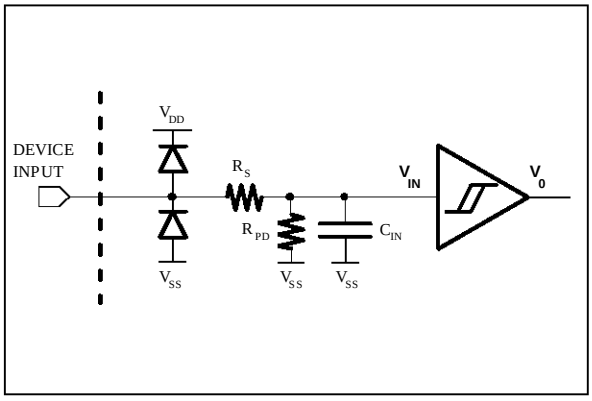
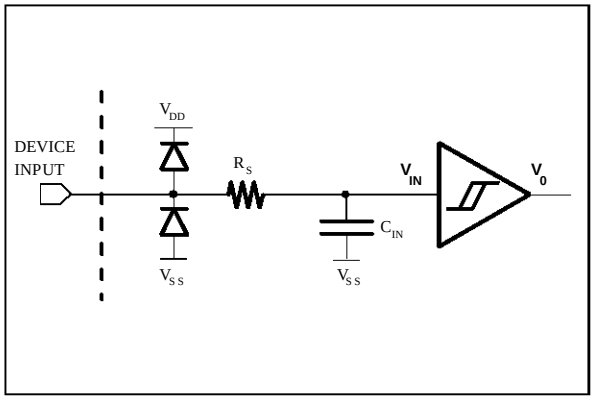


Figure 15. Input Pin Equivalent Circuit (1) Pull Down



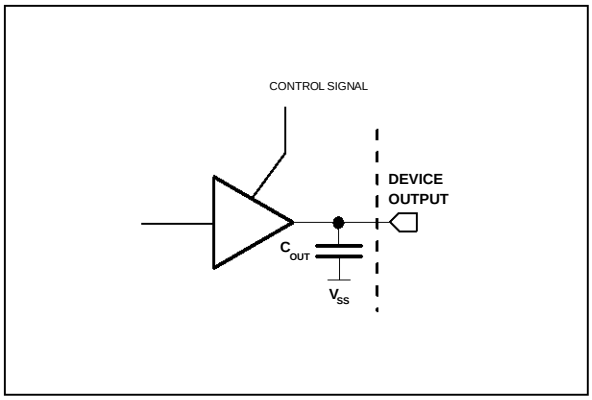
Note: 1. Only $\overline{OE}$ and TEST pins.

Figure 16. Input Pin Equivalent Circuit (2)



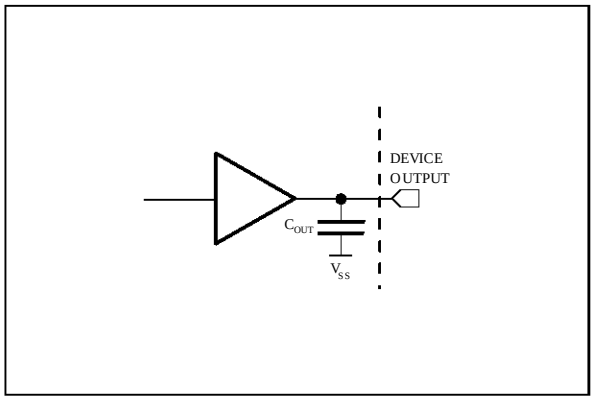
Note: 1. All input pins except for $\overline{OE}$ and TEST.

Figure 17. Equivalent Tristate Output Circuit (1)



Note: 1. Only O0-O11 pins.

Figure 18. Equivalent Output Circuit (1)

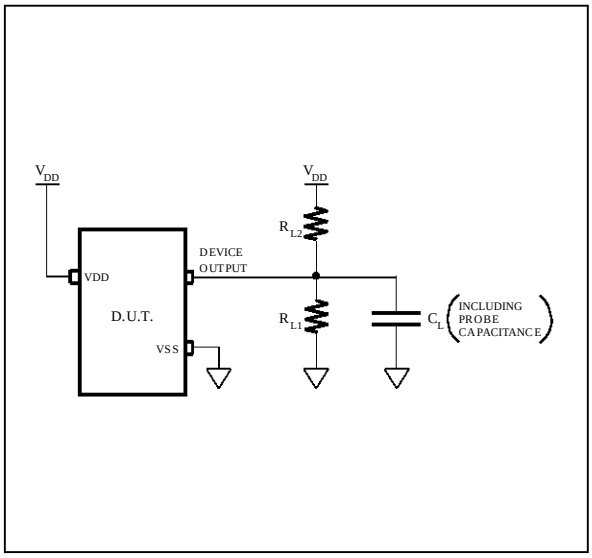


Note: 1. All output pins except for O0-O11.

Table 8. Equivalent Circuit Parameters

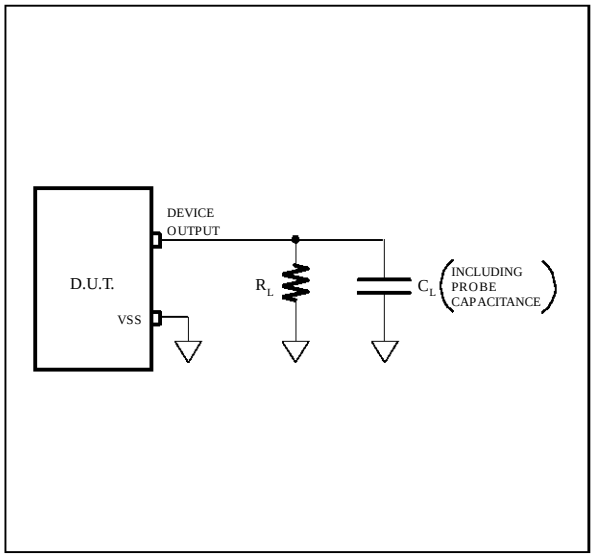
Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_I = 0V f = 1.0 MHz			15	pF
C_{OUT}	Output Capacitance	VO = 0V f = 1.0 MHz			15	pF
R_S	Stray Resistor			20		Ohm
R_{PD}	Pull Down Resistor	V_I = 2V, V_{DD} = 5V V_I = 0.8V, V_{DD} = 5V		16K 13.6K		Ohm

Figure 19. AC Test Circuit (1)



Note: 1. Only O0-O11pins.

Figure 20. AC Test Circuit (1)



Note: 1. All output pins except for O0-O11.

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V±5% T_A = 0 to +70 °C unless otherwise specified.

Figure 21. Data Input Timing

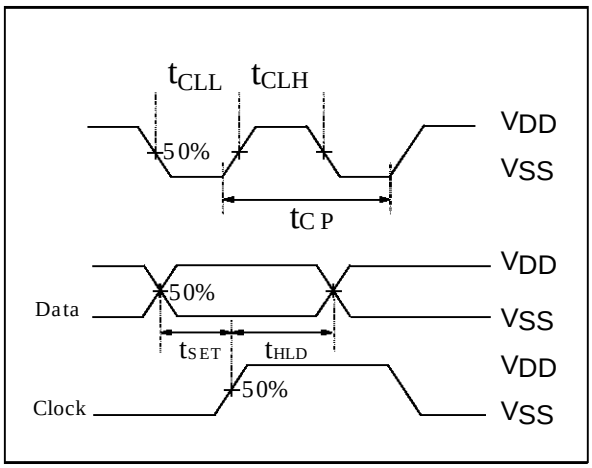


Figure 22. Input/Output Rise & Fall Times

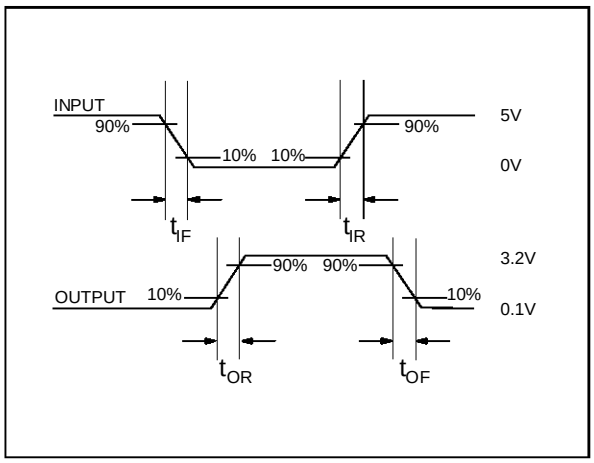


Table 9. Timing Parameters

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
t_{CLH}	Clock High			10		ns
t_{CLL}	Clock Low			15		ns
t_{SET}	Setup			15		ns
t_{HLD}	Hold			15		ns
t_{OR}	Output Rise	see fig.22		3		ns
t_{OF}	Output Fall	see fig.22		3		ns

Test Conditions MCLK frequency = 40MHz, T = +25°C.

OFF-LINE SLAVE DOWNLOADING PHASE TIMING

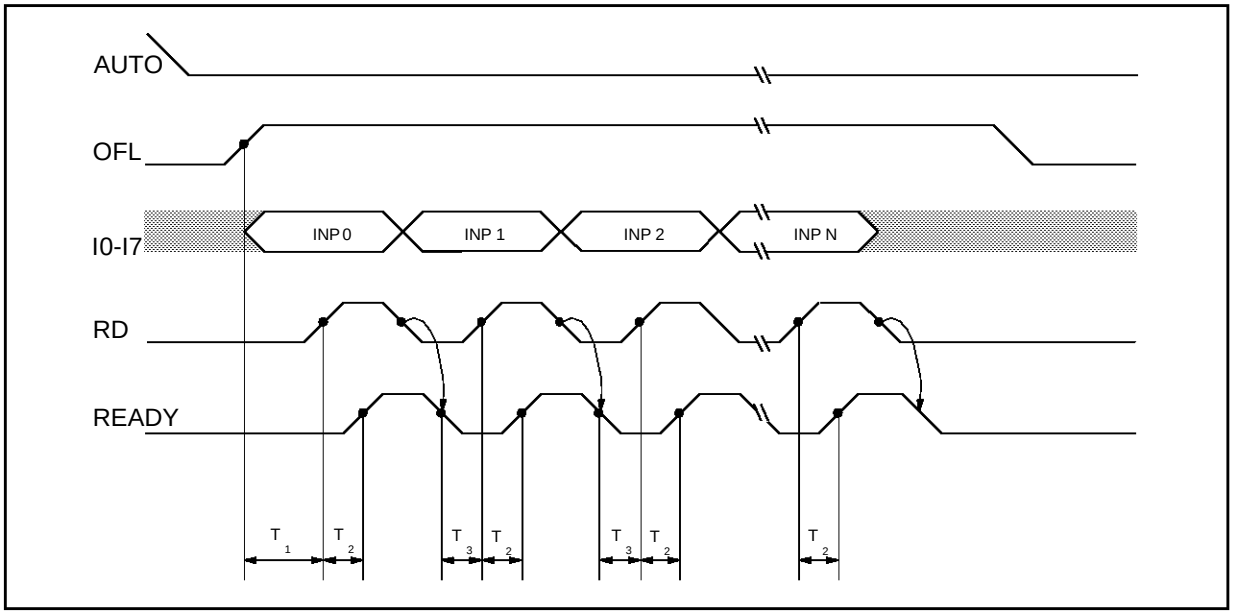
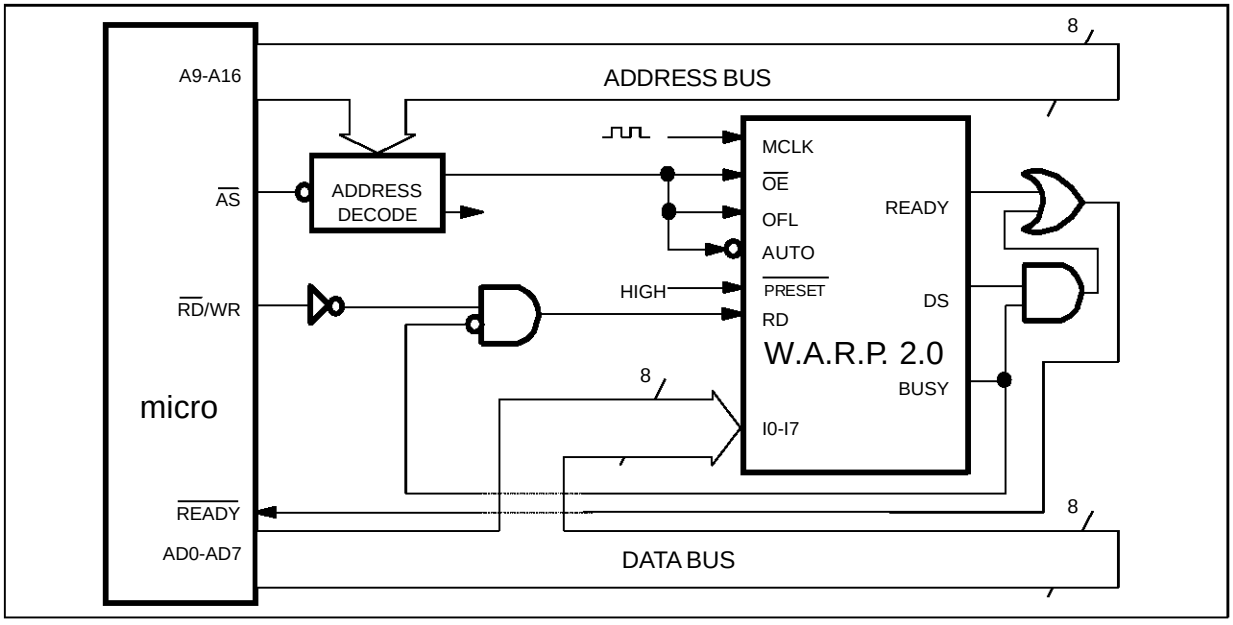


Table 10. Off-Line Slave Timing Parameters

Symbol	Mode	Parameter	Min	Typ	Max	Unit
T_1	Off-Line Slave	OFL High to first RD High	3			Clock Pulses
T_2	Off-Line Slave	RD High to READY High		4		Clock Pulses
T_3	Off-Line Slave	READY Low to RD High	3			Clock Pulses

Figure 23. Off-Line Slave Typical Application



OFF-LINE AUTO-BOOT PHASE TIMING

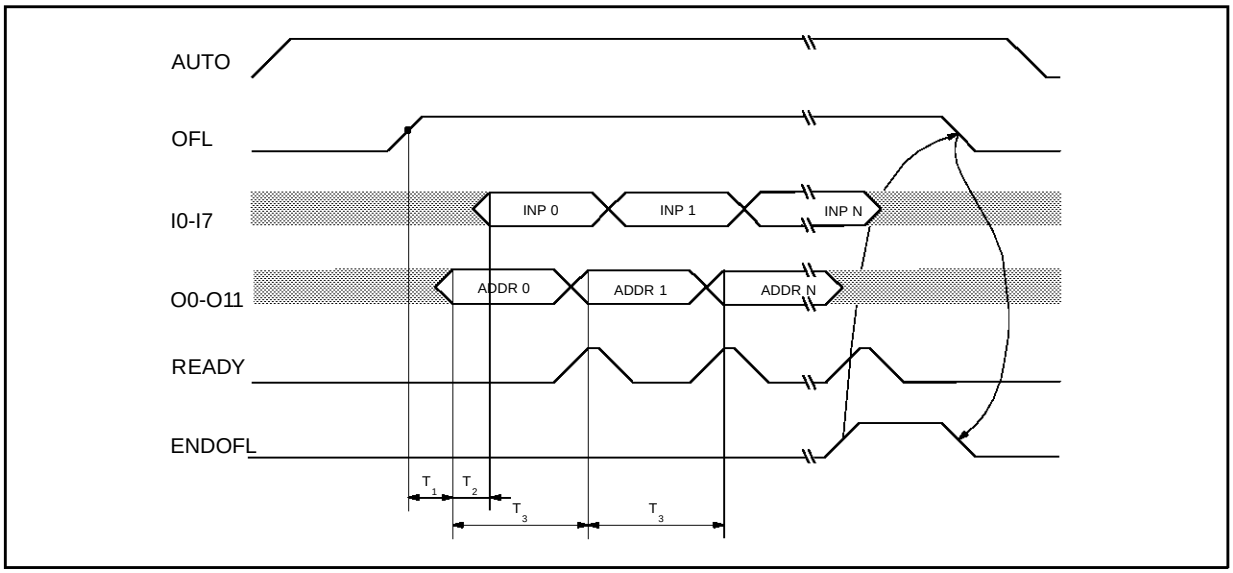
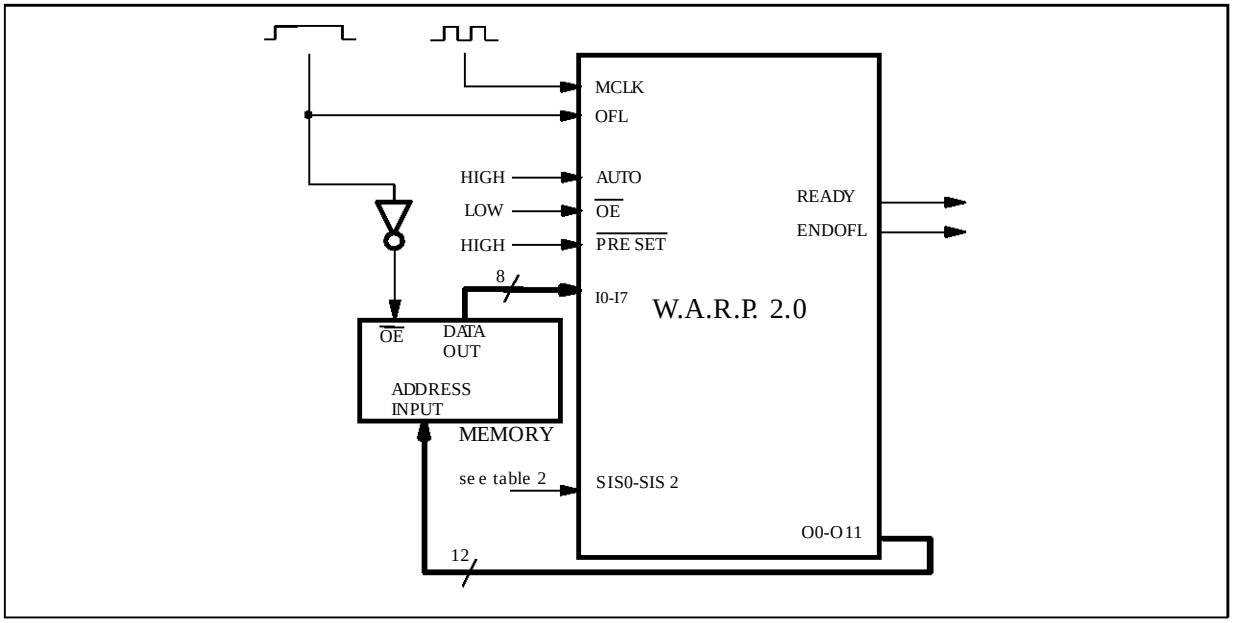


Table 11. Off-Line Auto-Boot Timing Parameters

Symbol	Mode	Parameter	Min	Typ	Max	Unit
T_1	Off-Line Auto-Boot	OFL High to Address Valid	3			Clock Pulses
T_2	Off-Line Auto-Boot	Address Valid to Input Sampling			8	Clock Pulses
T_3(1)	Off-Line Auto-Boot	Address Valid to next Address Valid	16		32	Clock Pulses

Note: 1. see Table 2.

Figure 24. Off-Line Auto-Boot typical Application



ON-LINE SLAVE PHASE TIMING

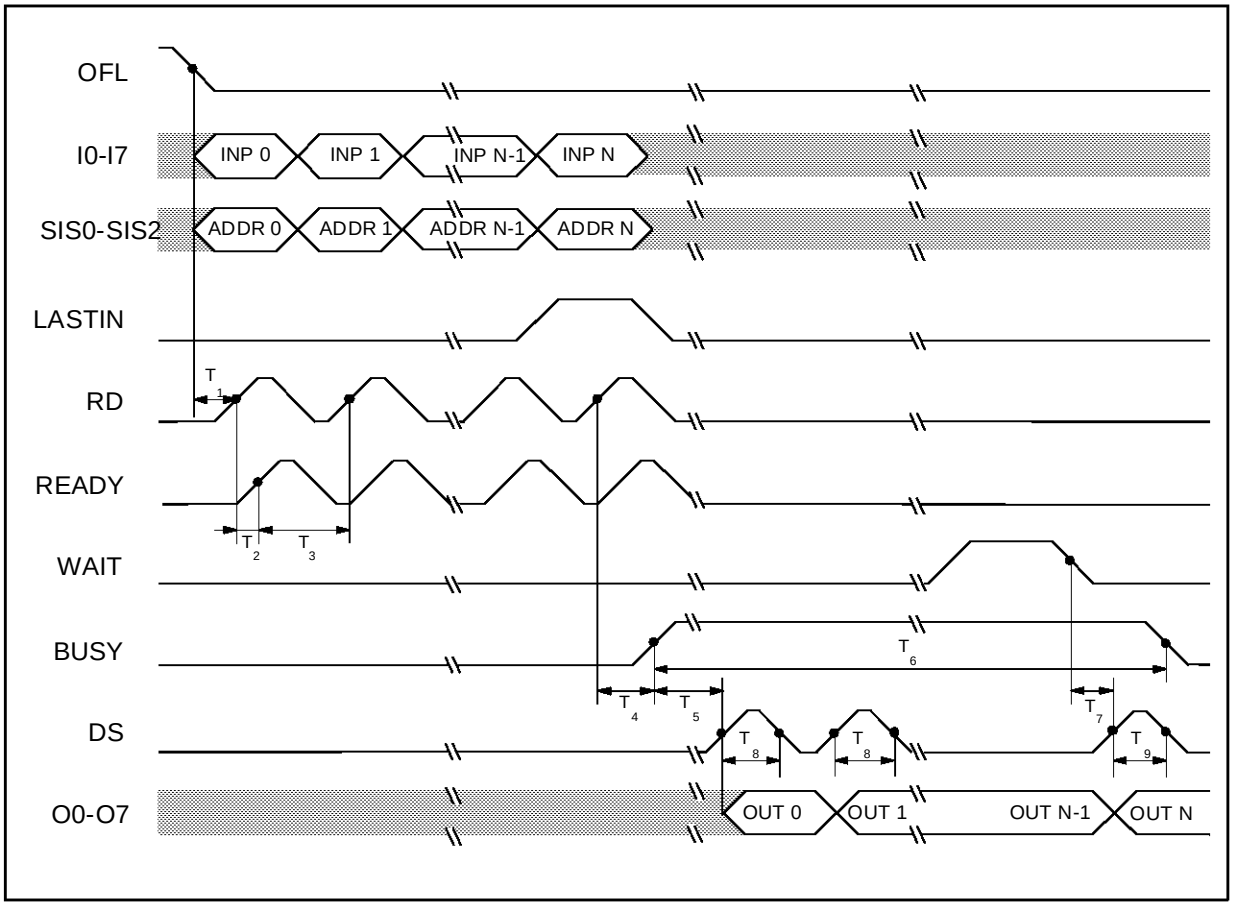
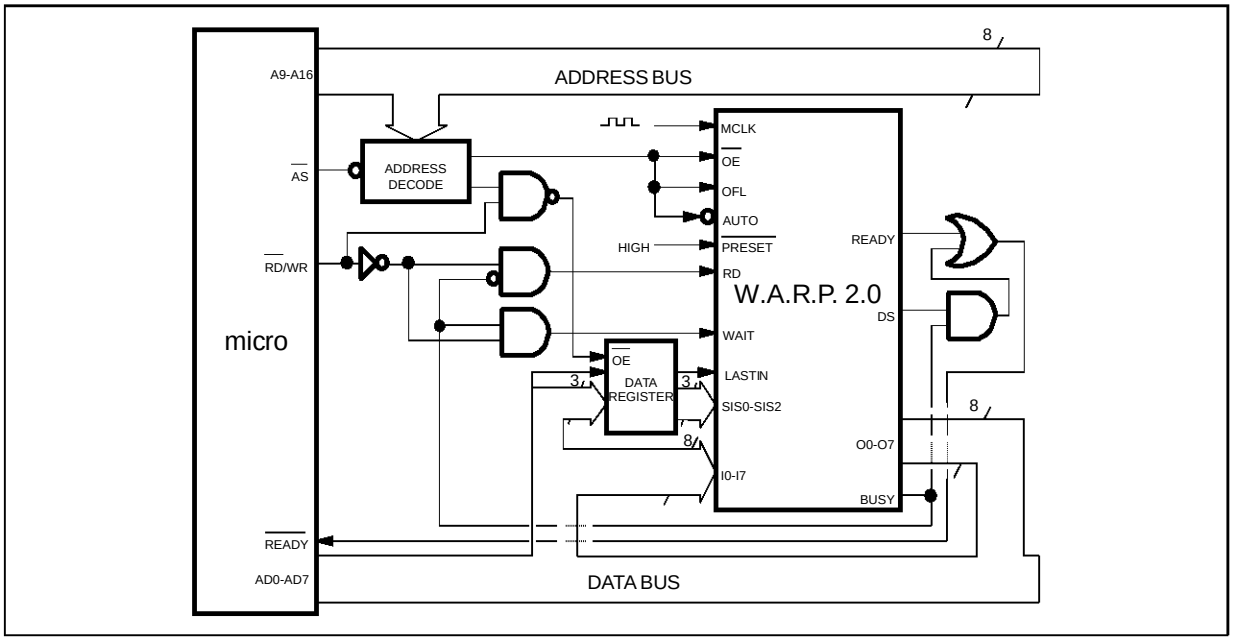


Table 12. On-Line Slave Timing Parameters

Symbol	Mode	Parameter	Min	Typ	Max	Unit
T_1	On-Line Slave	OFL Low to first RD High	3			Clock Pulses
T_2	On-Line Slave	RD High to READY High		2		Clock Pulses
T_3	On-Line Slave	READY High to next RD High	5			Clock Pulses
T_4	On-Line Slave	Last RD High to BUSY High		10		Clock Pulses
T_5(1)	On-Line Slave	BUSY High to first Output Ready	64			Clock Pulses
T_6	On-Line Slave	Elaboration Time		see fig.6		Clock Pulses
T_7	On-Line Slave	Wait Low to next Output Valid			32	Clock Pulses
T_8	On-Line Slave	DS Pulse Width		5		Clock Pulses
T_9	On-Line Slave	LAST DS Pulse Width		1		Clock Pulses

Note 1. T7 depends on the number of rules related to the current output variable. Each output variable needs at least two rules and each rule requires 32 clock pulses.

ON-LINE SLAVE TYPICAL APPLICATION



ON-LINE MASTER PHASE TIMING

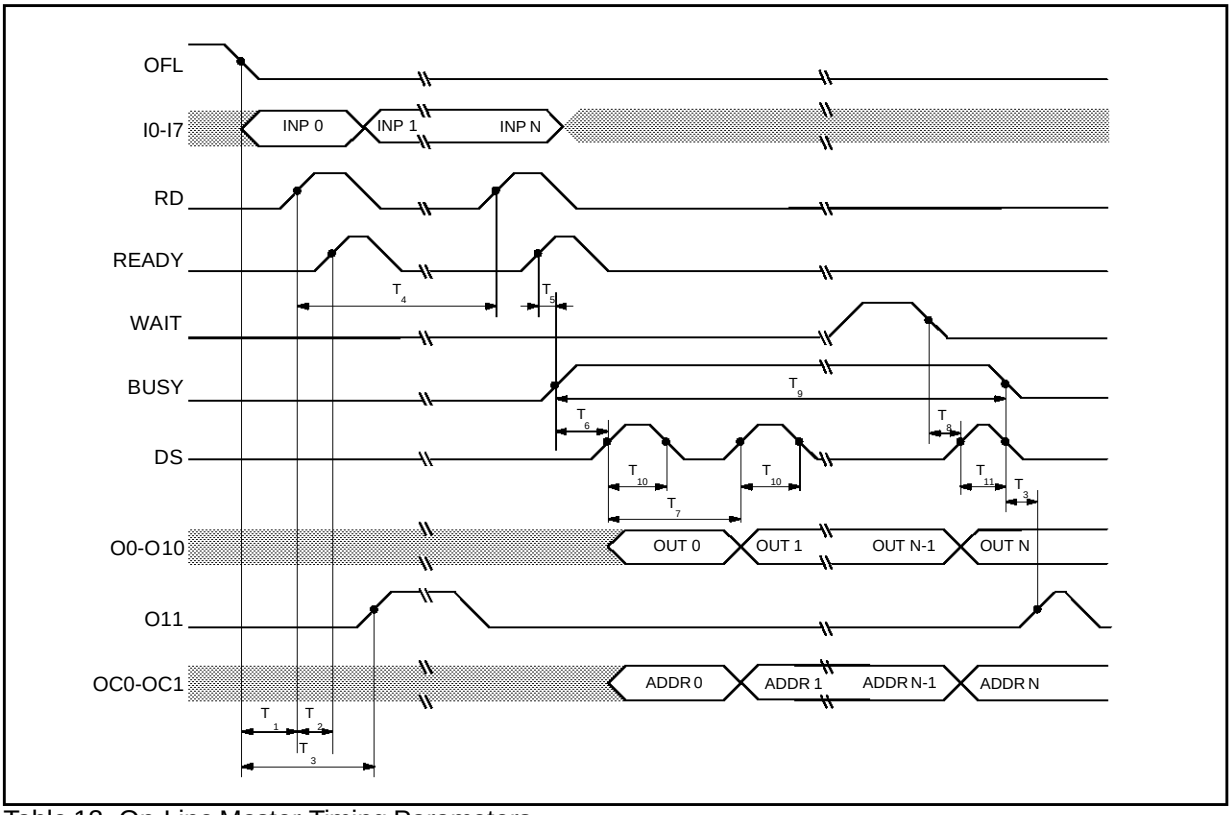
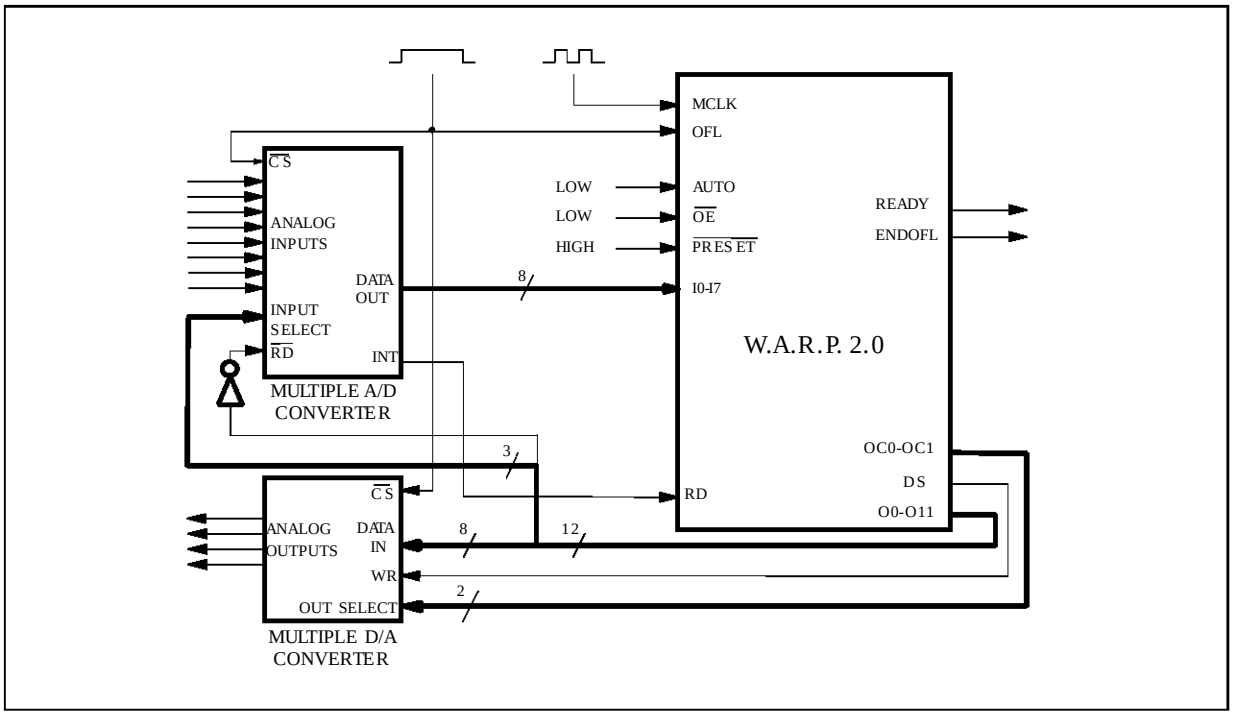


Table 13. On-Line Master Timing Parameters

Symbol	Mode	Parameter	Min	Typ	Max	Unit
T_1	On-Line Master	OFL Low to first RD High	3			Clock Pulses
T_2	On-Line Master	RD High to READY High		2		Clock Pulses
T_3	On-Line Master	OFL/BUSY Low to O11 Pulse		10		Clock Pulses
T_4	On-Line Master	RD High to next RD High		10		Clock Pulses
T_5	On-Line Master	READY High to BUSY High		1		Clock Pulses
T_6(1)	On-Line Master	BUSY High to first Output Ready	64			Clock Pulses
T_7(1)	On-Line Master	DS High to next DS High	64			Clock Pulses
T_8	On-Line Master	WAIT Low to next Output Valid			32	Clock Pulses
T_9	On-Line Master	Elaboration Time		see fig.6		Clock Pulses
T_{10}	On-Line Master	DS Pulse Width		5		Clock Pulses
T_{11}	On-Line Master	LAST DS Pulse Width		1		Clock Pulses

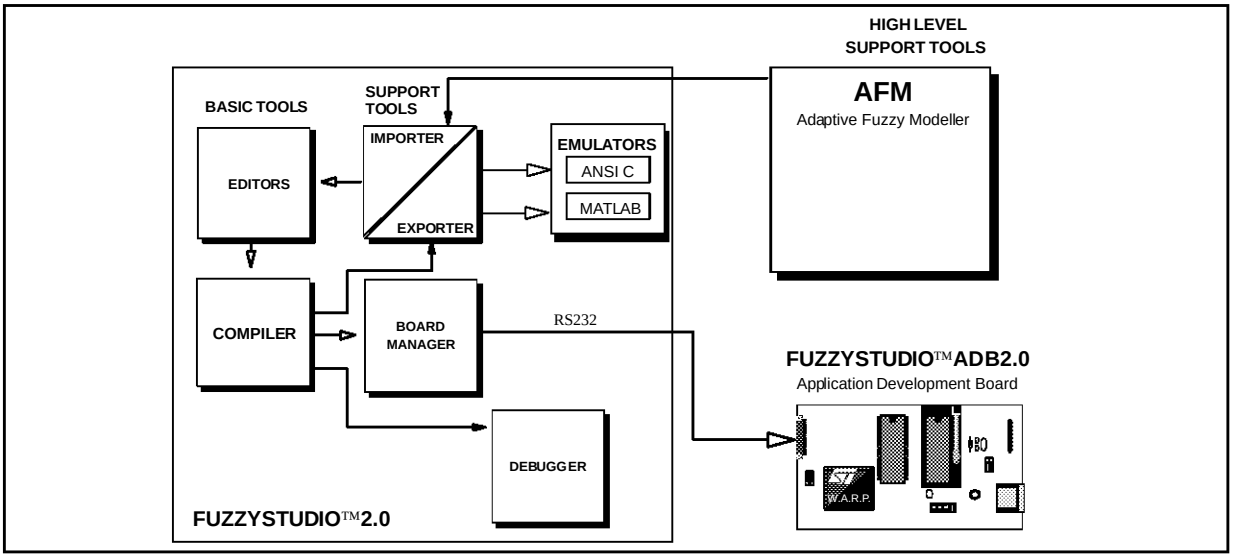
Note 1. It depends on the number of rules related to the current output variable. Each output variable needs at least two rules and each rule requires 32 clock pulses.

ON-LINE MASTER TYPICAL APPLICATION



PROGRAMMING TOOLS

Figure 25. FUZZYSTUDIO™ 2.0 Block Diagram



FUZZYSTUDIO™ 2.0

SGS-THOMSON has developed a software tools to support the use of W.A.R.P.2.0 allowing easy configurating and loading of the memories and functional simulations.
It has been designed in order to be used with the following hardware/software requirements:

- 80386 (or higher) processor
- VGA / SVGA screen
- Windows Version 3.0 or Higher

The constituting blocks are:

Editors

it is a tool to define the fuzzy controller with a User-Friendly Interface.
It is composed by:

- Variables Editor: to define the I/O variables, and to draw relatedmembership functions.
- Rule Editor (to define the base of knowledge)

Compiler

it generates the code to be loaded in W.A.R.P.2.0 memories according to the data defined through the editor. It also generates the data base for Debugger, Exporter and Simulator.

Debugger

it allows the user to examine step-by-step the fuzzy computation for a defined application. It also allows to check the results of the entire control process by using a list of patterns stored into a file.

Exporter

it generates files to be imported in different environments in order to develop W.A.R.P.2.0 based simulations exploiting user-developed models.
It addresses the following environments:
Standard C: the exporter generates C functions that can be recalled by an user program
MATLAB: the exporter generates a '.M' file that can be used to perform simulations in MATLAB environments

Importer

It allows to use a fuzzy project edited by a development system of a different hardware device, i.e. W.A.R.P.3 family, or by the AFM.

Board Manager

It allows the W.A.R.P.2.0 and ZEROPOWER programming, board testing and project debugging directly on the silicon.

FUZZYSTUDIO™ ADB2.0 DESCRIPTION

The board has been designed to be connected to the RS232 port of an IBM PC 386 (or higher), but it can also work stand alone.

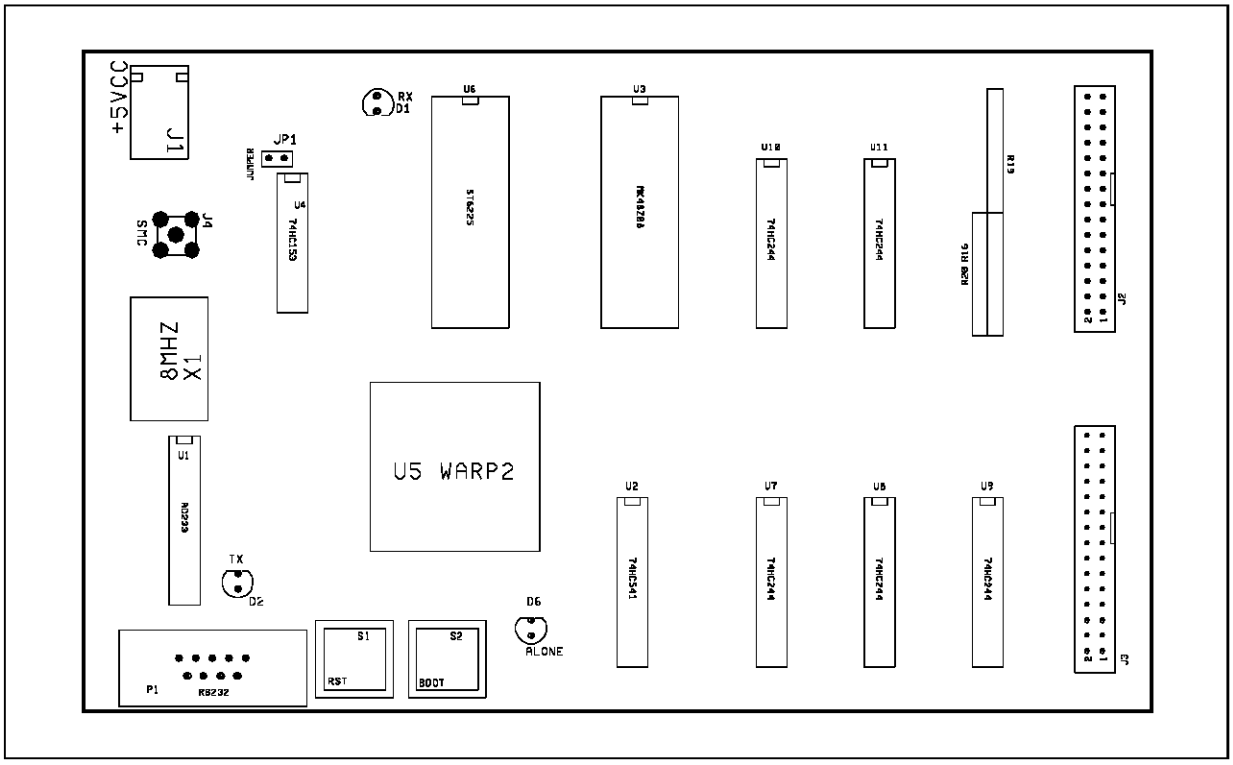
It can manage up to 8 digital inputs and 4 digital outputs.

Inputs and outputs are provided at TTL compatible level. The board allows the user to charge the rules and the membership functions (see FUZZYSTUDIO™ 2.0 User Manual) into the W.A.R.P.2.0 memories.

The clock generator frequency on board is 8 MHz. An automatic trigger is used to synchronize W.A.R.P.2.0 with the external environment (working connected with a PC).

When the board is used deconnected from a PC all the fuzzy data (membership functions and rules) are stored in a ZEROPOWER SRAM.

Figure 26. FUZZYSTUDIO™ ADB2.0 Board Layout



Tab. 14 Ordering Information

Order Code	Device	Development Tools	
		FUZZYSTUDIO™ ADB2.0	SW Tools
STFLSTUDIO2/KIT	STFLWARP20/PL	W.A.R.P.2.0 W.A.R.P.2.0 programmer ZEROPOWER programmer RS-232 communication handler Internal Clock	Variables and Rules Editor W.A.R.P.2.0 Compiler/Debugger Exporter for ANSI C and MATLAB® Importer from AFM

Adaptive Fuzzy Modeller

Adaptive Fuzzy Modeller (AFM) is a tool that easily allows to obtain a model of a system based on Fuzzy Logic data structure, starting from the sampling of a process/function expressed in terms of Input\Output values pairs (patterns).

Its primary capability is the automatic generation of a database containing the inference rules and the parameters describing the membership functions. The generated Fuzzy Logic knowledge base represents an optimized approximation of the process/function provided as input.

The AFM has the capability to translate its project files to FUZZYSTUDIO™ project files, MATLAB and C code, in order to use this environment as a support for simulation and control .

The block diagram illustrates the AFMdesign flow.

SUPPORTED TARGETS

The supported environment are:

- W.A.R.P. 1.1 using FUZZYSTUDIO™ 1.0
- W.A.R.P.2.0 using FUZZYSTUDIO™ 2.0
- MATLAB
- C Language
- Fu.L.L. (Fuzzy Logic Language).

SYSTEM REQUIREMENTS

MS-DOS version 3.1or higher

Microsoft Windows 3.0 or compatible later version

486, PENTIUM compatible processor chip

8 MBytes RAM (16 Mbytes recommended)

Hard Disk with at least 1MBytes free space

Figure 27. AFM Design Flow

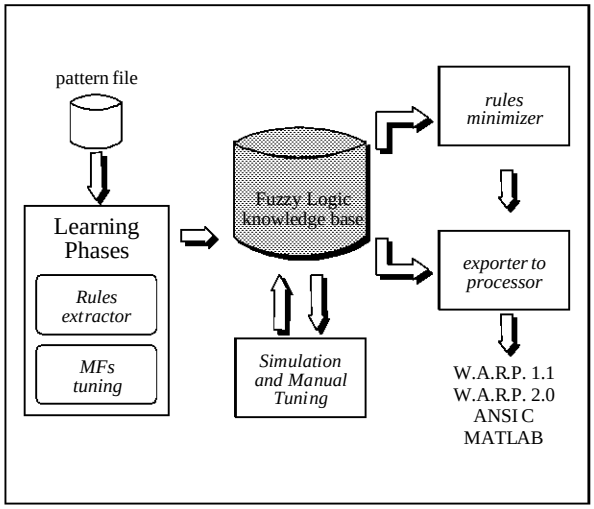


Table 15. Ordering Information

Order Code	Description	Supported Target	Functionalities	System Requirement
STFLAFM10/SW	WTA-FAM for Building Rules BACK-FAM for Building MFs	STFLWARP11/PG STFLWARP11/PL STFLWARP20/PL ANSI C MATLAB®	Rules Minimizer Step-by-Step Simulation Simulation from File Local Tuning	MS-DOS 3.1or higher Windows 3.0 or later 486, PENTIUM compatible 8 MB RAM

PACKAGE DIMENSIONS

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	

Figure 28. W.A.R.P.2.0 PLCC68 Package

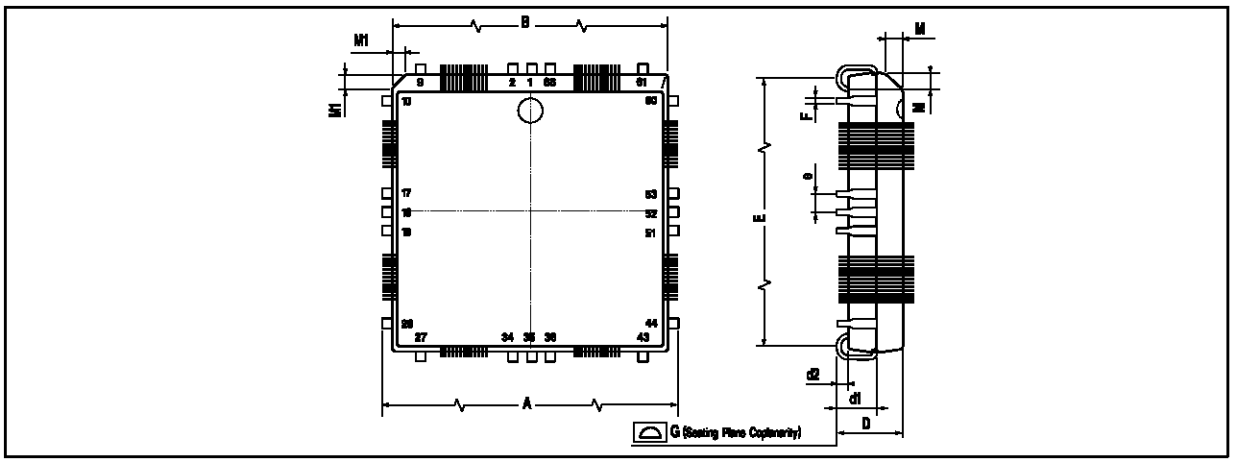


Table 16. Ordering Information

Part Number	Maximum Frequency	Supply Voltage	Temperature Range	Package
STFLWARP20/PL	40 MHz	5±5%	0 °C to 70 °C	PLCC68