Preliminary **8Mb (256Kx36 & 512x18) and 4Mb (128Kx36 & 256Kx18) SRAM**

Features

- 256K x 36 or 512K x 18 organizations
- 128K x 36 or 256K x 18 organizations
- 0.25 Micron CMOS technology
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write
- Single Differential Extended HSTL Clock
- +3.3V Power Supply, Ground, 1.5V V_{DDQ}, and 0.75V V_{REF}
- HSTL Input AND Outputs..
- Registered Addresses, Write Enables, Synchronous Select, and Data Ins.
- Registered Outputs
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability and Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers

Description

The 4Mb and 8Mb SRAMs—IBM0436A41QLAB, IBM0418A41QLAB, IBM0418A81QLAB, and IBM0436A81QLAB—are Synchronous Pipeline Mode, high-performance CMOS Static Random Access Memories that are versatile, have wide I/O, and can achieve 3ns cycle times. Differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K clock, all Addresses, Write-Enables, Sync Select, and Data Ins are registered internally. Data Outs are updated from output registers off the next rising edge of the K clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with HSTL I/O interfaces.

x36 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC,SA(8Mb)	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQ19	DQ18	V_{SS}	ZQ	V_{SS}	DQ9	DQ10
E	DQ22	DQ20	V_{SS}	$\overline{SS}$	V_{SS}	DQ11	DQb13
F	V_{DDQ}	DQ21	V_{SS}	$\overline{G}$	V_{SS}	DQ12	V_{DDQ}
G	DQ24	DQ23	$\overline{SBWc}$	NC	$\overline{SBWb}$	DQ14	DQb15
H	DQ25	DQ26	V_{SS}	NC	V_{SS}	DQ17	DQb16
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQ34	DQ35	V_{SS}	K	V_{SS}	DQ8	DQ7
L	DQ33	DQ32	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ5	DQ6
M	V_{DDQ}	DQ30	V_{SS}	$\overline{SW}$	V_{SS}	DQ3	V_{DDQ}
N	DQ31	DQ29	V_{SS}	SA	V_{SS}	DQ2	DQ4
P	DQ28	DQ27	V_{SS}	SA	V_{SS}	DQ0	DQ1
R	NC	SA	M1*	V_{DD}	M2*	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD} respectively.

x18 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	SA	NC	SA	NC,SA(8Mb)	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQ14	NC	V_{SS}	ZQ	V_{SS}	DQ0	NC
E	NC	DQ15	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQ1
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ2	V_{DDQ}
G	NC	DQ16	$\overline{SBWb}$	NC	NC	NC	DQ3
H	DQ17	NC	V_{SS}	NC	V_{SS}	DQ4	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQ13	V_{SS}	K	V_{SS}	NC	DQ8
L	DQ12	NC	NC	$\overline{K}$	$\overline{SBWa}$	DQ7	NC
M	V_{DDQ}	DQ10	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQ11	NC	V_{SS}	SA	V_{SS}	DQ6	NC
P	NC	DQ9	V_{SS}	SA	V_{SS}	NC	DQ5
R	NC	SA	M1	V_{DD}	M2	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD} respectively.

Pin Description

SA0-SA18	Address Input SA0-SA18 for 512Kx18 SA0-SA17 for 256Kx36 SA0-SA17 for 256Kx18 SA0-SA16 for 128Kx36	$\overline{G}$	Asynchronous Output Enable
DQ0-DQ35	Data I/O DQ0-DQ17 for 512Kx18 DQ0-DQ35 for 256Kx36	$\overline{SS}$	Synchronous Select
K, $\overline{K}$	Differential Input Register Clocks	M1, M2	Clock Mode Inputs- Selects Single or Dual Clock Operation.
$\overline{SW}$	Write Enable, Global	V_{REF}(2)	HSTL Input Reference Voltage
$\overline{SBWa}$	Write Enable, Byte a (DQ0-DQ8)	V_{DD}	Power Supply (+3.3V)
$\overline{SBWb}$	Write Enable, Byte b (DQ9-DQ17)	V_{SS}	Ground
$\overline{SBWc}$	Write Enable, Byte c (DQ18-DQ26)	V_{DDQ}	Output Power Supply
$\overline{SBWd}$	Write Enable, Byte d (DQ27-DQ35)	ZZ	Asynchronous Sleep Mode
TMS,TDI,TCK	IEEE 1149.1 Test Inputs (LVTTL levels)	ZQ	Output Driver Impedance Control
TDO	IEEE 1149.1 Test Output (LVTTL level)	NC	No Connect

Ordering Information

Part Number	Organization	Speed	Leads
IBM0418A41QLAB - 3	256K x 18	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0418A41QLAB - 4	256K x 18	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0418A41QLAB - 5	256K x 18	2.25ns Access /5.0ns Cycle	7 x 17 BGA
IBM0436A41QLAB - 3	128K x 36	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0436A41QLAB - 4	128K x 36	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0436A41QLAB - 5	128K x 36	2.25ns Access /5.0ns Cycle	7 x 17 BGA
IBM0418A81QLAB - 3	512K x 18	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0418A81QLAB - 4	512K x 18	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0418A81QLAB - 5	512K x 18	2.25ns Access /5.0ns Cycle	7 x 17 BGA
IBM0436A81QLAB -3	256K x 36	1.7ns Access / 3.0ns Cycle	7 x 17 BGA
IBM0436A81QLAB -4	256K x 36	2.0ns Access / 4.0ns Cycle	7 x 17 BGA
IBM0436A81QLAB -5	256K x 36	2.25ns Access /5.0ns Cycle	7 x 17 BGA

Revision Log

Revision	Contents of Modification
9/98	Initial Release
11/98	Changed part numbers from Rev A to B. Input levels adjusted.

For a complete datasheet, please contact your IBM sales representative.

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visit us on World Wide Web at http://www.chips.ibm.com

IBM Microelectronics manufacturing is ISO 9000 compliant.

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