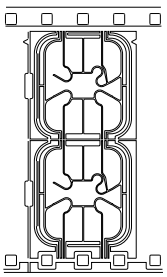
M14256
M14128

Memory Card IC
256/128 Kbit Serial I^2C Bus EEPROM

DATA BRIEFING

- Compatible with I^2C Extended Addressing
- Two Wire I^2C Serial Interface Supports 400 kHz Protocol
- Single Supply Voltage (2.5 V to 5.5 V)
- Hardware Write Control
- BYTE and PAGE WRITE (up to 64 Bytes)
- BYTE, RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behaviour
- 100,000 Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)
- 5 ms Programming Time (typical)



Micromodule (D22)

DESCRIPTION

Each device is an electrically erasable programmable memory (EEPROM) fabricated with STMicroelectronics's High Endurance, Double Polysilicon, CMOS technology. This guarantees an endurance typically well above 100,000 Erase/Write cycles, with a data retention of 40 years. The memory operates with a power supply as low as 2.5 V for the M14xxx-W version.

The M14256 and M14128 are available in micromodule form only. For availability of the M14256 or

Figure 1. Logic Diagram

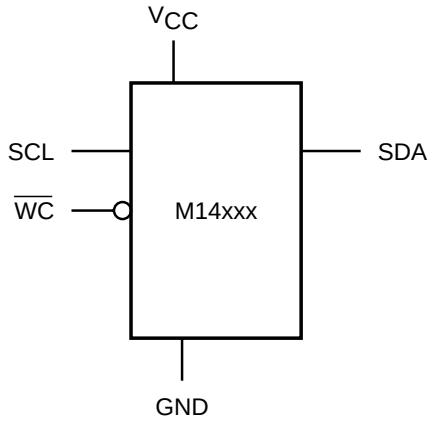


Table 1. Signal Names

SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
GND	Ground

M14128 in wafer form, please contact your ST sales office.

Each memory is compatible with the I^2C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 7-bit unique Device Type Identifier code (1010000) in accordance with the I^2C bus definition. Only one memory can be attached to each I^2C bus.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition, generated by the bus master. The START condition is followed by the Device Select Code which is composed of a stream of 7 bits (1010000), plus one read/write bit (R/$\overline{W}$) and is terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Figure 2. D22 Contact Connections

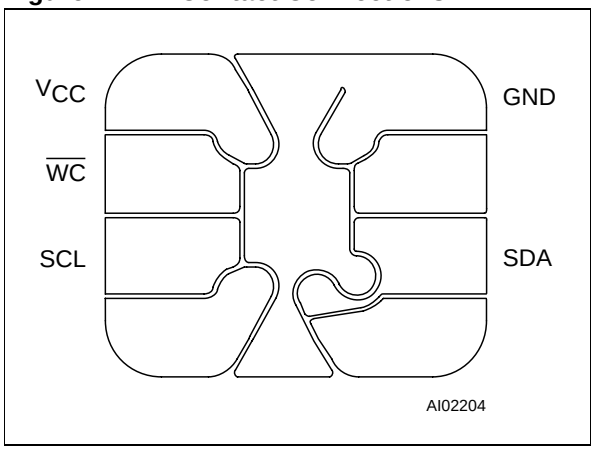


Table 2. Ordering Information Scheme

Example: M14256 - W D22

Memory Capacity

256	256 Kbit
128	128 Kbit

Delivery Form

D22	Module on Super 35 mm film

Operating Voltage

W	2.5 V to 5.5 V

Devices are shipped from the factory with the memory content set at all '1's (FFh).

For a list of available options (speed, package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.