56855

Data Sheet

Technical Data

56800E
16-bit Digital Signal Controllers

DSP56855
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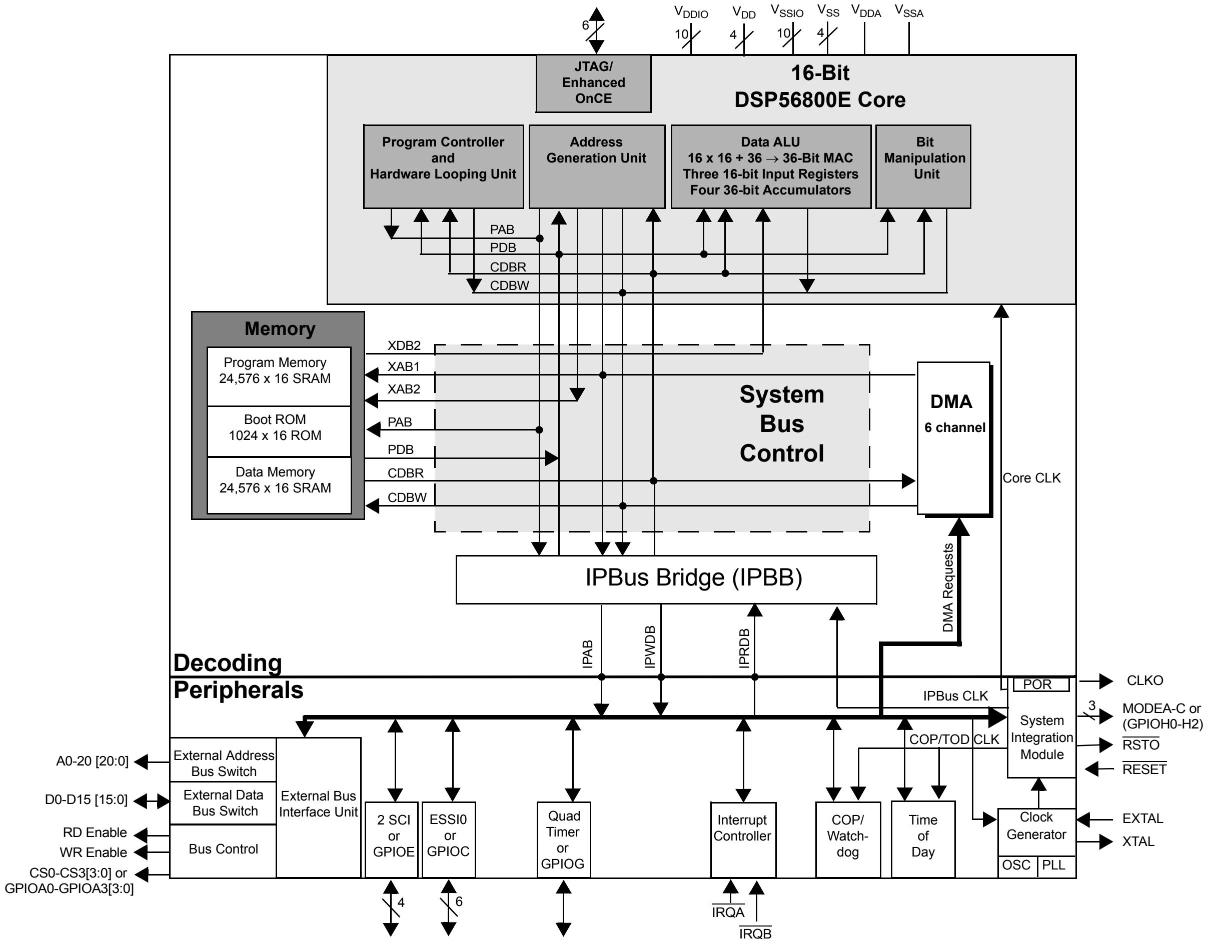
56855 General Description

- 120 MIPS at 120MHz
- 24K x 16-bit Program SRAM
- 24K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Access up to 2M words of program memory or 8M words of data memory
- Chip Select Logic for glueless interface to ROM and SRAM
- Six (6) independent channels of DMA
- Enhanced Synchronous Serial Interface (ESSI)
- Two (2) Serial Communication Interfaces (SCI)
- General Purpose 16-bit Quad Timer with 1 external pin
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time-of-Day (TOD)
- 100 LQFP package
- Up to 18 GPIO



56855 Block Diagram

Part 1 Overview

1.1 56855 Features

1.1.1 Core

- Efficient 16-bit engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
  - 24K × 16-bit Program SRAM
  - 24K × 16-bit Data SRAM
  - 1K × 16-bit Boot ROM
- Off-Chip Memory Expansion (EMI)
  - Access up to 2M words of program memory or 8M words of data memory
  - Chip Select Logic for glue-less interface to ROM and SRAM

1.1.3 Peripheral Circuits for 56855

- General Purpose 16-bit Quad Timer with 1 external pin*
- Two (2) Serial Communication Interfaces (SCI)*
- Enhanced Synchronous Serial Interface (ESSI) module*
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging

- Six (6) independent channels of DMA
- Time-of-Day (TOD)
- Up to 18 GPIO

* Each peripheral I/O can be used alternately as a General Purpose I/O if not needed

1.1.4 Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

1.2 56855 Description

The 56855 is a member of the 56800E core-based family of controllers. It combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals, creating an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56855 is well-suited for many applications. The 56855 includes many peripherals that are especially useful for low-end Internet appliance applications and low-end client applications such as telephony; portable devices; Internet audio; and point-of-sale systems, such as noise suppression; ID tag readers; sonic/subsonic detectors; security access devices; remote metering; sonic alarms.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications.

The 56855 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56855 also provides two external dedicated interrupt lines, and up to 18 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56855 controller includes 24K words of Program RAM, 24K words of Data RAM and 1K of Boot ROM. It also supports program execution from external memory.

This controller also provides a full set of standard programmable peripherals that include one Enhanced Synchronous Serial Interface (ESSI), two Serial Communications Interfaces (SCI), and one Quad Timer. The ESSI, SCIs, four chip selects and Quad Timer external output can be used as General Purpose Input/Outputs when its primary function is not required.

1.3 State of the Art Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description of and proper design with the 56855. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56855 Chip Documentation

Topic	Description	Order Number
56800E Reference Manual	Detailed description of the 56800E architecture, and 16-bit core processor and the instruction set	56800ERM
DSP56855 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56855	DSP5685xUM
56855 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	56855
DSP56855 Errata	Details any chip issues that might be present	DSP56855E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$ This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.

"asserted" A high true (active high) signal is high or a low true (active low) signal is low.

"deasserted" A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56855 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 3-1** each table row describes the package pin and the signal or signals present.

Table 2-1 56855 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD}, V_{DDIO}, or V_{DDA})	(4, 10, 1)[1]
Ground (V_{SS}, V_{SSIO}, or V_{SSA})	(4, 10, 1)[1]
PLL and Clock	3
External Bus Signals	39
External Chip Select*	4
Interrupt and Program Control	7[2]
Enhanced Synchronous Serial Interface (ESSI0) Port*	6
Serial Communications Interface (SCI0) Ports*	2
Serial Communications Interface (SCI1) Ports*	2
Quad Timer Module Port*	1
JTAG/Enhanced On-Chip Emulation (EOnCE)	6

*Alternately, GPIO pins

1. $V_{DD} = V_{DD\ CORE}$, $V_{SS} = V_{SS\ CORE}$, $V_{DDIO} = V_{DD\ IO}$, $V_{SSIO} = V_{SS\ IO}$, $V_{DDA} = V_{DD\ ANA}$, $V_{SSA} = V_{SS\ ANA}$
2. MODA, MODB and MODC can be used as GPIO after the bootstrap process has completed.

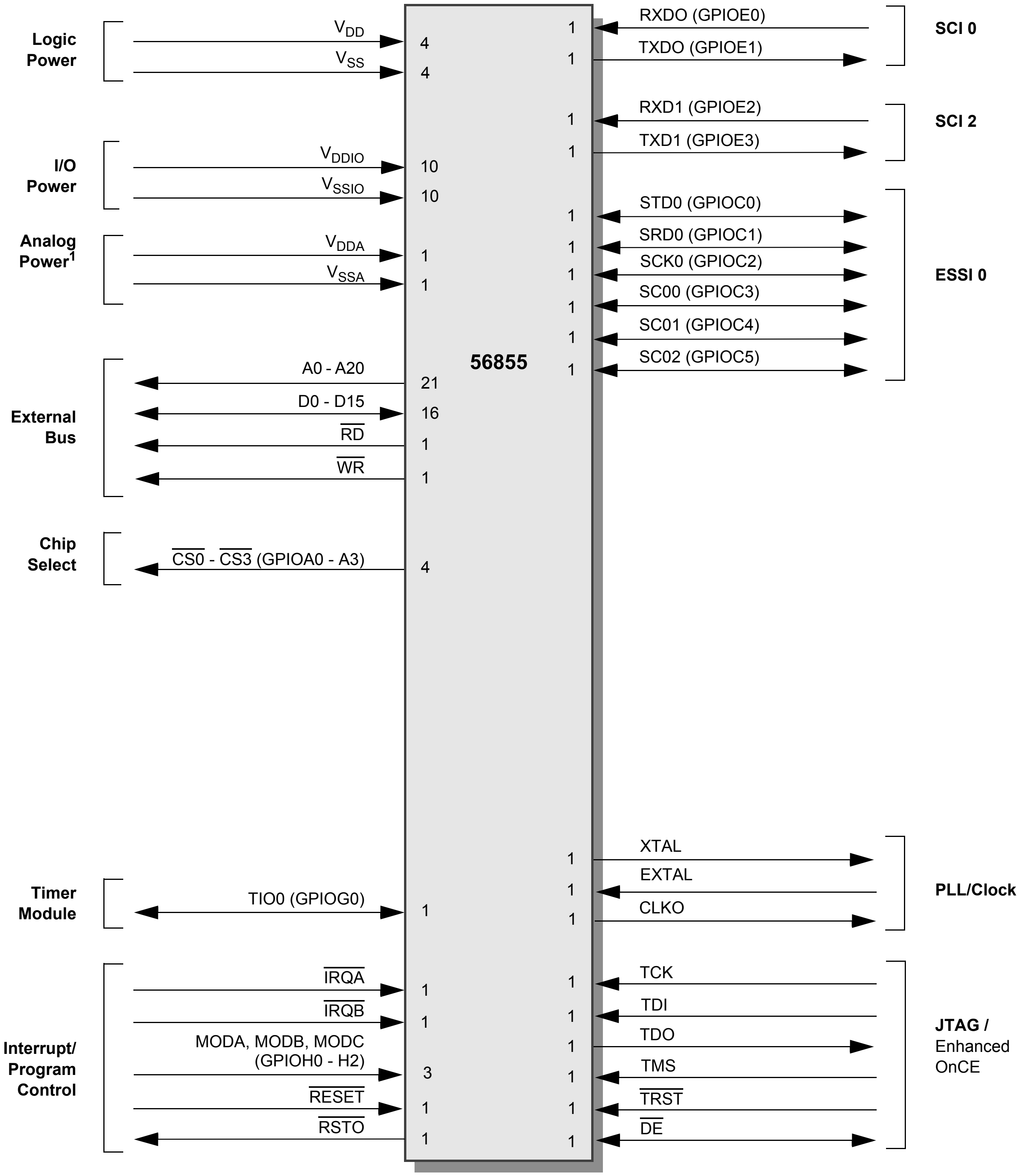


Figure 2-1 56855 Signals Identified by Functional Group[2]

1. Specifically for PLL, OSC, and POR.
2. Alternate pin functions are shown in parentheses.

Part 3 Signals and Package Information

All digital inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are enabled by default. Exceptions:

1. When a pin has GPIO functionality, the pull-up may be disabled under software control.
2. MODE A, MODE B and MODE C pins have no pull-up.
3. TCK has a weak pull-down circuit always active.
4. Bidirectional I/O pullups automatically disable when the output is enabled.

This table is presented consistently with the *Signals Identified by Functional Group* figure.

1. **BOLD** entries in the *Type* column represents the state of the pin just out of reset.
2. Output(Z) means an output in a High-Z condition.

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP

Pin No.	Signal Name	Type	Description
9	V_{DD}	V_{DD}	**Power (V_{DD})**—These pins provide power to the internal structures of the chip, and should all be attached to $V_{DD.}$
35	V_{DD}		
65	V_{DD}		
84	V_{DD}		
10	V_{SS}	V_{SS}	**Ground (V_{SS})**—These pins provide grounding for the internal structures of the chip and should all be attached to $V_{SS.}$
36	V_{SS}		
66	V_{SS}		
85	V_{SS}		

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
1	V_{DDIO}	V_{DDIO}	**Power (V_{DDIO})**—These pins provide power for all I/O and ESD structures of the chip, and should all be attached to V_{DDIO} (3.3V).
14	V_{DDIO}		
29	V_{DDIO}		
43	V_{DDIO}		
49	V_{DDIO}		
58	V_{DDIO}		
72	V_{DDIO}		
76	V_{DDIO}		
86	V_{DDIO}		
96	V_{DDIO}		
2	V_{SSIO}	V_{SSIO}	**Ground (V_{SSIO})**—These pins provide grounding for all I/O and ESD structures of the chip and should all be attached to $V_{SS.}$
15	V_{SSIO}		
30	V_{SSIO}		
44	V_{SSIO}		
50	V_{SSIO}		
60	V_{SSIO}		
73	V_{SSIO}		
78	V_{SSIO}		
87	V_{SSIO}		
97	V_{SSIO}		
2	V_{SSIO}		
18	V_{DDA}	V_{DDA}	**Analog Power (V_{DDA})**—These pins supply an analog power source.
19	V_{SSA}	V_{SSA}	**Analog Ground (V_{SSA})**—This pin supplies an analog ground.

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
5	A0	Output(Z)	**Address Bus (A0-A20)**—These signals specify a word address for external program or data memory access.
6	A1		
7	A2		
8	A3		
22	A4		
23	A5		
24	A6		
25	A7		
31	A8		
32	A9		
33	A10		
34	A11		
45	A12		
46	A13		
47	A14		
48	A15		
53	A16		
54	A17		
55	A18		
56	A19		
57	A20		

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
59	D0	**Input**/Output(Z)	**Data Bus (D0-D15)**—These pins provide the bidirectional data for external program or data memory accesses.
67	D1		
68	D2		
69	D3		
70	D4		
71	D5		
79	D6		
80	D7		
81	D8		
82	D9		
83	D10		
94	D11		
95	D12		
98	D13		
99	D14		
3	$\overline{\text{RD}}$	Output	**Read Enable ($\overline{\text{RD}}$)**— is asserted during external memory read cycles. This signal is pulled high during reset.
4	$\overline{\text{WR}}$	Output	**Write Enable ($\overline{\text{WR}}$)** — is asserted during external memory write cycles. This signal is pulled high during reset.
61	$\overline{\text{CS0}}$ GPIOA0	**Output** **Input**/Output	**External Chip Select ($\overline{\text{CS0}}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (0**) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
62	$\overline{\text{CS1}}$ GPIOA1	**Output** **Input**/Output	**External Chip Select ($\overline{\text{CS1}}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (1)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
63	$\overline{\text{CS2}}$ GPIOA2	**Output** **Input**/Output	**External Chip Select ($\overline{\text{CS2}}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (2)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
64	CS3	**Output**	**External Chip Select (CS3)**—This pin is used as a dedicated GPIO.
	GPIOA3	**Input**/Output	**Port A GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
77	TIO0	**Input**/Output	**Timer Input/Output (TIO0)**—This pin can be independently configured to be either timer input source or output flag.
	GPIOG0	Input/Output	**Port G GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
16	IRQA	Input	**External Interrupt Request A and B**—The IRQA and IRQB inputs are asynchronized external interrupt requests that indicate that an external device is requesting service. A Schmitt trigger input is used for noise immunity. They can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for Wired-OR operation.
17	IRQB		
11	MODA	**Input**	**Mode Select (MODA)**—During the bootstrap process MODA selects one of the eight bootstrap modes.
	GPIOH0	Input/Output	**Port H GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
12	MODB	**Input**	**Mode Select (MODB)**—During the bootstrap process MODB selects one of the eight bootstrap modes.
	GPIOH1	Input/Output	**Port H GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
13	MODC	**Input**	**Mode Select (MODC)**—During the bootstrap process MODC selects one of the eight bootstrap modes.
	GPIOH2	Input/Output	**Port H GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
28	RESET	Input	**Reset (RESET)**—This input is a direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the RESET pin is deasserted, the initial chip operating mode is latched from the MODA, MODB, and MODC pins. To ensure complete hardware reset, RESET and TRST should be asserted together. The only exception occurs in a debugging environment when a hardware reset is required and it is necessary not to reset the JTAG/Enhanced OnCE module. In this case, assert RESET, but do not assert TRST.
27	RSTO	Output	**Reset Output (RSTO)**—This output is asserted on any reset condition (external reset, low voltage, software or COP).

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
51	RXD0	**Input**	**Serial Receive Data 0 (RXD0)**—This input receives byte-oriented serial data and transfers it to the SCI 0 receive shift register.
	GPIOE0	Input/Output	**Port E GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
52	TXD0	**Output(Z)**	**Serial Transmit Data 0 (TXD0)**—This signal transmits data from the SCI 0 transmit data register.
	GPIOE1	Input/Output	**Port E GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
74	RXD1	**Input**	**Serial Receive Data 1 (RXD1)**—This input receives byte-oriented serial data and transfers it to the SCI 1 receive shift register.
	GPIOE2	Input/Output	**Port E GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
75	TXD1	**Output(Z)**	**Serial Transmit Data 1 (TXD1)**—This signal transmits data from the SCI 1 transmit data register.
	GPIOE3	Input/Output	**Port E GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
88	STD0	**Output**	**ESSI Transmit Data (STD0)**—This output pin transmits serial data from the ESSI Transmitter Shift Register.
	GPIOC0	Input/Output	**Port C GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
89	SRD0	**Input**	**ESSI Receive Data (SRD0)**—This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
	GPIOC1	Input/Output	**Port C GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
90	SCK0	**Input**/Output	**ESSI Serial Clock (SCK0)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
	GPIOC2	Input/Output	**Port C GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
91	SC00	**Input**/Output	**ESSI Serial Control Pin 0 (SC00)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
	GPIOC3	Input/Output	**Port C GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
92	SC01	**Input**/Output	**ESSI Serial Control Pin 1 (SC01)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
	GPIOC4	Input/Output	**Port C GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
93	SC02	**Input**/Output	**ESSI Serial Control Pin 2 (SC02)**—This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
	GPIOC5	Input or Output	**Port C GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
20	XTAL	Input/**Output**	**Crystal Oscillator Output (XTAL)**—This output connects the internal crystal oscillator output to an external crystal. If an external clock source other than a crystal oscillator is used, XTAL must be used as the input.
21	EXTAL	Input	**External Crystal Oscillator Input (EXTAL)**—This input should be connected to an external crystal. If an external clock source other than a crystal oscillator is used, EXTAL must be tied off. See Section 4.5.2
26	CLKO	Output	**Clock Output (CLKO)**—This pin outputs a buffered clock signal. When enabled, this signal is the system clock divided by four.
42	TCK	Input	**Test Clock Input (TCK)**—This input pin provides a gated clock to synchronize the test logic and to shift serial data to the JTAG/Enhanced OnCE port. The pin is connected internally to a pull-down resistor.
40	TDI	Input	**Test Data Input (TDI)**—This input pin provides a serial input data stream to the JTAG/Enhanced OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
39	TDO	Output (Z)	**Test Data Output (TDO)**—This tri-statable output pin provides a serial output data stream from the JTAG/Enhanced OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.

Table 3-1. 56855 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
41	TMS	Input	**Test Mode Select Input (TMS)**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
38	TRST	Input	**Test Reset (TRST)**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, TRST should be asserted whenever RESET is asserted. The only exception occurs in a debugging environment, since the Enhanced OnCE/JTAG module is under the control of the debugger. In this case it is not necessary to assert TRST when asserting RESET. Outside of a debugging environment RESET should be permanently asserted by grounding the signal, thus disabling the Enhanced OnCE/JTAG module on the device. **Note:** For normal operation, connect TRST directly to V_{SS}. If the design is to be used in a debugging environment, TRST may be tied to V_{SS} through a 1K resistor.
37	DE	**Input**/Output	**Debug Event (DE)**—This is an open-drain, bidirectional, active low signal. As an input, it is a means of entering debug mode of operation from an external command controller. As an output, it is a means of acknowledging that the chip has entered debug mode. This pin is connected internally to a weak pull-up resistor.

Part 4 Specifications

4.1 General Characteristics

The 56855 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term "5-volt tolerant" refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V- compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 4-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56855 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 4-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}[1]	V_{SS} – 0.3	V_{SS} + 2.0	V
Supply voltage, IO Supply voltage, analog	V_{DDIO}[2] V_{DDIO}[2]	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 4.0 V_{DDA} + 4.0	V
Digital input voltages Analog input voltages (XTAL, EXTAL)	V_{IN} V_{INA}	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 5.5 V_{DDA} + 0.3	V
Current drain per pin excluding V_{DD}, GND	I	—	8	mA
Junction temperature	T_J	-40	120	°C
Storage temperature range	T_{STG}	-55	150	°C

1. V_{DD} must not exceed V_{DDIO}
2. V_{DDIO} and V_{DDA} must not differ by more that 0.5V

Table 4-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage for Logic Power	V_{DD}	1.62	1.98	V
Supply voltage for I/O Power	V_{DDIO}	3.0	3.6	V
Supply voltage for Analog Power	V_{DDA}	3.0	3.6	V

Table 4-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Ambient operating temperature	T_A	-40	85	°C
PLL clock frequency[1]	f_{pll}	—	240	MHz
Operating Frequency[2]	f_{op}	—	120	MHz
Frequency of peripheral bus	f_{ipb}	—	60	MHz
Frequency of external clock	f_{clk}	—	240	MHz
Frequency of oscillator	f_{osc}	2	4	MHz
Frequency of clock via XTAL	f_{xtal}	—	240	MHz
Frequency of clock via EXTAL	f_{extal}	2	4	MHz

1. Assumes clock source is direct clock to EXTAL or crystal oscillator running 2-4MHz. PLL must be enabled, locked, and selected. The actual frequency depends on the source clock frequency and programming of the CGM module.
2. Master clock is derived from on of the following four sources:
   $f_{clk} = f_{xtal}$ when the source clock is the direct clock to EXTAL
   $f_{clk} = f_{pll}$ when PLL is selected
   $f_{clk} = f_{osc}$ when the source clock is the crystal oscillator and PLL is not selected
   $f_{clk} = f_{extal}$ when the source clock is the direct clock to EXTAL and PLL is not selected

Table 4-3 Thermal Characteristics[1]

Characteristic	100-pin LQFP		
	Symbol	Value	Unit
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	41.2	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined	W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$	W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / R\theta_{JA}$ [2]	°C

1. See **Section 6.1** for more detail.
2. TJ = Junction Temperature
   TA = Ambient Temperature

4.2 DC Electrical Characteristics

Table 4-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	V_{DDA} – 0.8	V_{DDA}	V_{DDA} + 0.3	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V
Input low voltage	V_{IL}	-0.3	—	0.8	V
Input current low (pullups disabled)	I_{IL}	-1	—	1	μA
Input current high (pullups disabled)	I_{IH}	-1	—	1	μA
Output tri-state current low	I_{OZL}	-10	—	10	μA
Output tri-state current high	I_{OZH}	-10	—	10	μA
Output High Voltage	V_{OH}	V_{DDIO} – 0.7	—	—	V
Output Low Voltage	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	8	—	16	mA
Output Low Current	I_{OL}	8	—	16	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current (Core logic, memories, peripherals) Run [1] Deep Stop[2] Light Stop[3]	I_{DD}[4]	 — — —	 70 0.05 5	 110 10 14	 mA mA mA
V_{DDIO} supply current (I/O circuity) Run[5] Deep Stop[2]	I_{DDIO}	 —	 40 0	 50 1.5	 mA mA
V_{DDA} supply current (analog circuity) Deep Stop[2]	I_{DDA}	 —	 60	 120	 μA
Low Voltage Interrupt[6]	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[7]	POR	—	1.5	2.0	V

Note: Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out.

1. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator and time of day module operating.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator and time of day module operating.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.

5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.8V no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.

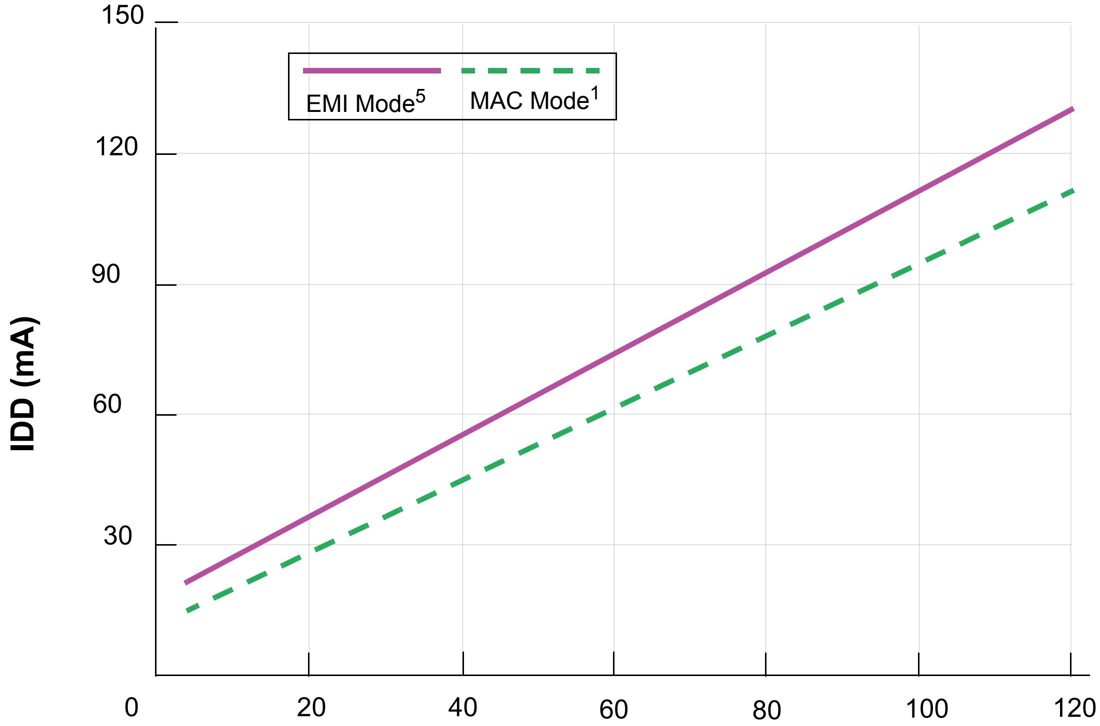
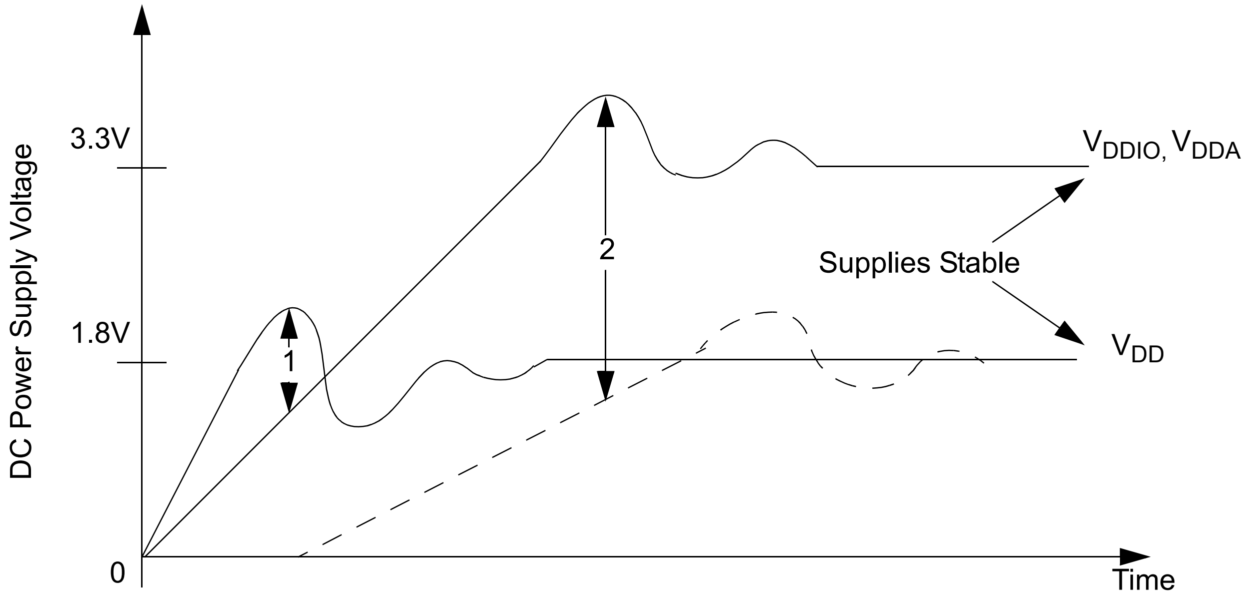


Figure 4-1 Maximum Run $I_{DDTOTAL}$ vs. Frequency (see Notes 1. and 5. in Table 4-4)

4.3 Supply Voltage Sequencing and Separation Cautions

Figure 4-2 shows two situations to avoid in sequencing the V_{DD} and V_{DDIO}, V_{DDA} supplies.



Notes: 1. V_{DD} rising before V_{DDIO}, V_{DDA}
2. V_{DDIO}, V_{DDA} rising much faster than V_{DD}

Figure 4-2 Supply Voltage Sequencing and Separation Cautions

V_{DD} should not be allowed to rise early (1). This is usually avoided by running the regulator for the V_{DD} supply (1.8V) from the voltage generated by the 3.3V V_{DDIO} supply, see **Figure 4-3**. This keeps V_{DD} from rising faster than V_{DDIO}.

V_{DD} should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies, as shown in **Figure 4-3**. The series diodes forward bias when the difference between V_{DDIO} and V_{DD} reaches approximately 2.1, causing V_{DD} to rise as V_{DDIO} ramps up. When the V_{DD} regulator begins proper operation, the difference between supplies will typically be 0.8V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to:

$V_{DDIO} \geq V_{DD} \geq (V_{DDIO} - 2.1V)$

In practice, V_{DDA} is typically connected directly to V_{DDIO} with some filtering.

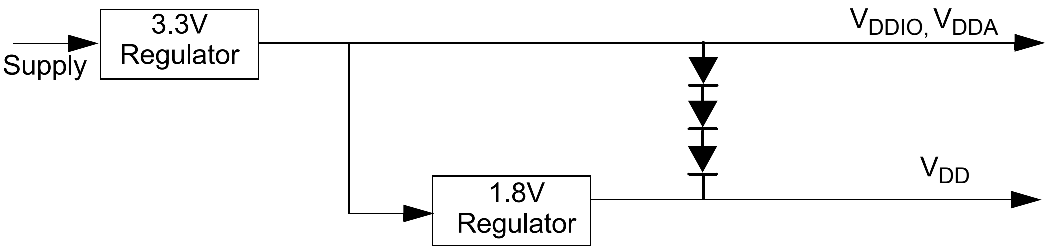
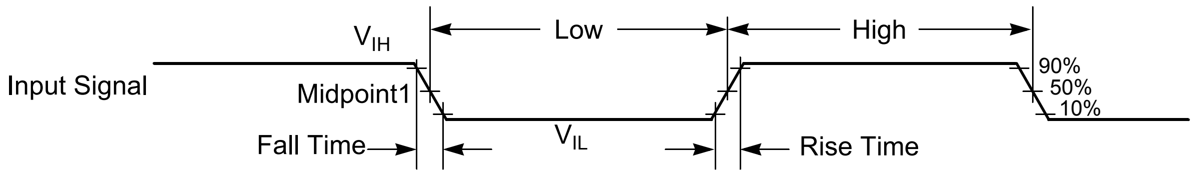


Figure 4-3 Example Circuit to Control Supply Sequencing

4.4 AC Electrical Characteristics

Timing waveforms in **Section 4.2** are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins except XTAL, which is tested using the input levels in **Section 4.2**. In **Figure 4-4** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 4-4 Input Signal Measurement References

Figure 4-5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state.
- Tri-stated, when a bus or signal is placed in a high impedance state.
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}.
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}.

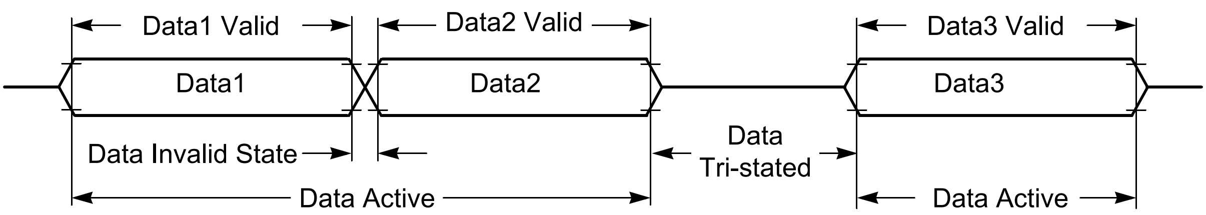


Figure 4-5 Signal State

4.5 External Clock Operation

The 56855 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

4.5.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 4-5**. In **Figure 4-6** a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

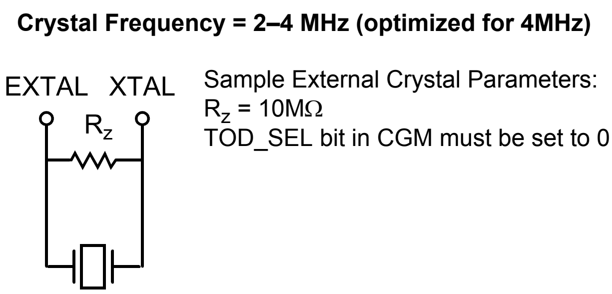


Figure 4-6 Crystal Oscillator

4.5.2 High Speed External Clock Source (> 4MHz)

The recommended method of connecting an external clock is given in **Figure 4-7.** The external clock source is connected to XTAL and the EXTAL pin is held at ground, V_{DDA}, or $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

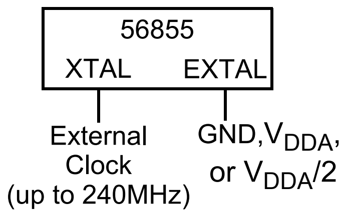


Figure 4-7 Connecting a High Speed External Clock Signal using XTAL

4.5.3 Low Speed External Clock Source (2-4MHz)

The recommended method of connecting an external clock is given in **Figure 4-8**. The external clock source is connected to XTAL and the EXTAL pin is held at $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

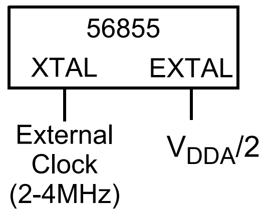


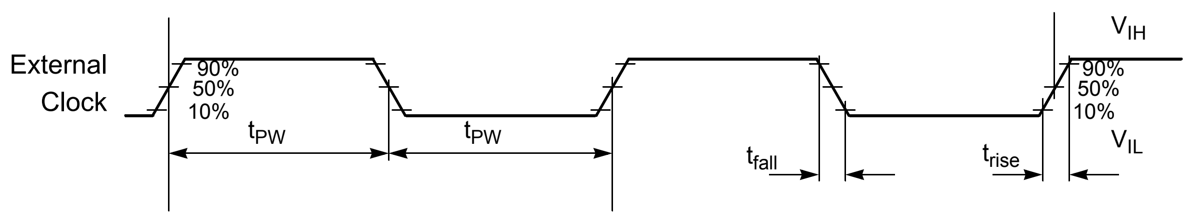
Figure 4-8 Connecting a Low Speed External Clock Signal using XTAL

Table 4-5 External Clock Operation Timing Requirements[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	240	MHz
Clock Pulse Width[4]	t_{PW}	6.25	—	—	ns
External clock input rise time[2, 4]	t_{rise}	—	—	TBD	ns
External clock input fall time[3, 4]	t_{fall}	—	—	TBD	ns

1. See **Figure 4-7** for details on using the recommended connection of an external clock driver.
2. External clock input rise time is measured from 10% to 90%.
3. External clock input fall time is measured from 90% to 10%.
4. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 4-9 External Clock Timing

Table 4-6 PLL Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = –40°$ to +120°C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	4	MHz
PLL output frequency	f_{clk}	40	—	240	MHz
PLL stabilization time [2]	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

4.6 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. **Figure 4-10** shows sample timing and parameters that are detailed in **Table 4-7**.

The timing of each parameter consists of both a fixed delay portion and a clock related portion; as well as user controlled wait states. The equation:

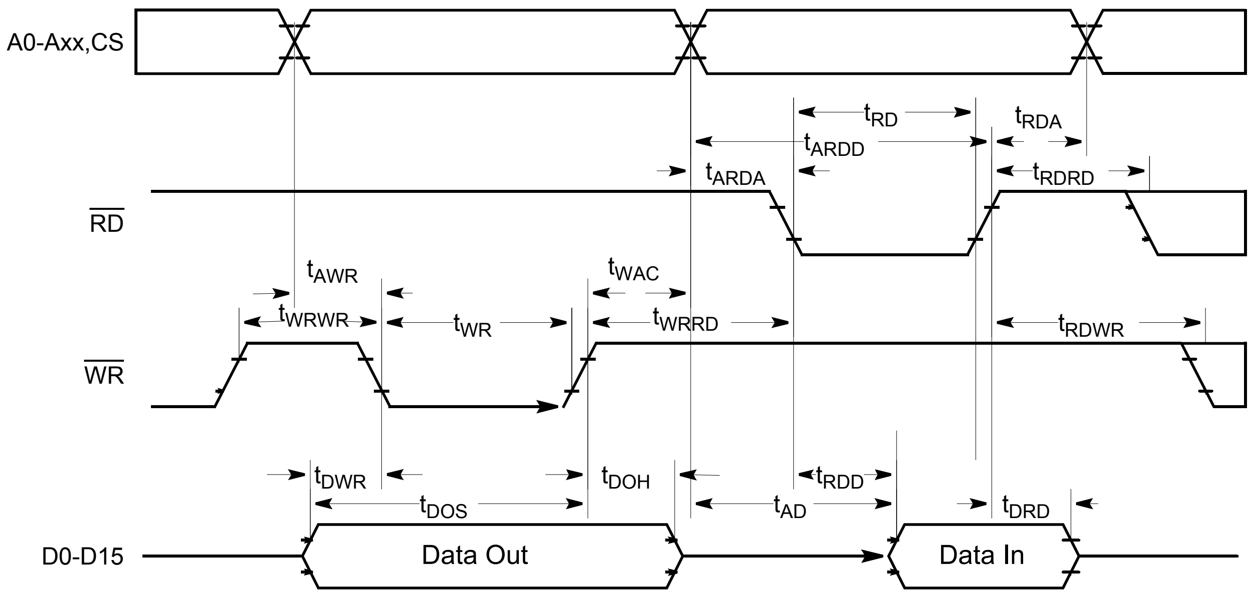
$$t = D + P * (M + W)$$

should be used to determine the actual time of each parameter. The terms in the above equation are defined as:

- t parameter delay time
- D fixed portion of the delay, due to on-chip path delays.
- P the period of the system clock, which determines the execution rate of the part (i.e. when the device is operating at 120 MHz, P = 8.33 ns).
- M Fixed portion of a clock period inherent in the design. This number is adjusted to account for possible clock duty cycle derating.
- W the sum of the applicable wait state controls. See the “Wait State Controls” column of **Table 4-7** for the applicable controls for each parameter. See the EMI chapter of the 83x Peripheral Manual for details of what each wait state field controls.

Some of the parameters contain two sets of numbers. These parameters have two different paths and clock edges that must be considered. Check both sets of numbers and use the smaller result. The appropriate entry may change if the operating frequency of the part changes.

The timing of write cycles is different when WWS = 0 than when WWS > 0. Therefore, some parameters contain two sets of numbers to account for this difference. The “Wait States Configuration” column of **Table 4-7** should be used to make the appropriate selection.



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 4-10 External Memory Interface Timing

Table 4-7 External Memory Interface Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98 V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40× to +120×C, C_L £ 50pF, P = 8.333ns

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	WWS=0	-0.79	0.50	WWSS	ns
		WWS>0	-1.98	0.69		
$\overline{WR}$ Width Asserted to $\overline{WR}$ Deasserted	t_{WR}	WWS=0	-0.86	0.19	WWS	ns
		WWS>0	-0.01	0.00		
Data Out Valid to $\overline{WR}$ Asserted	t_{DWR}	WWS=0	-1.52	0.00	WWSS	ns
		WWS=0	- 5.69	0.25		
		WWS>0	-2.10	0.19		
		WWS>0	-4.66	0.50		
Valid Data Out Hold Time after $\overline{WR}$ Deasserted	t_{DOH}		-1.47	0.25	WWSH	ns
Valid Data Out Set Up Time to $\overline{WR}$ Deasserted	t_{DOS}		-2.36	0.19	WWS,WWSS	ns
			-4.67	0.50		
Valid Address after $\overline{WR}$ Deasserted	t_{WAC}		-1.60	0.25	WWSH	
$\overline{RD}$ Deasserted to Address Invalid	t_{RDA}		- 0.44	0.00	RWSH	ns

Table 4-7 External Memory Interface Timing (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA}$ = 0 V, V_{DD} = 1.62-1.98 V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40× to +120×C, C_L £ 50pF, P = 8.333ns

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{RD}$ Deasserted	t_{ARDD}		-2.07	1.00	RWSS,RWS	ns
Valid Input Data Hold after $\overline{RD}$ Deasserted	t_{DRD}		0.00	N/A[1]	—	ns
$\overline{RD}$ Assertion Width	t_{RD}		-1.34	1.00	RWS	ns
Address Valid to Input Data Valid	t_{AD}		-10.27	1.00	RWSS,RWS	ns
			-13.5	1.19		
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}		- 0.94	0.00	RWSS	ns
$\overline{RD}$ Asserted to Input Data Valid	t_{RDD}		-9.53	1.00	RWSS,RWS	ns
			-12.64	1.19		
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}		-0.75	0.25	WWSH,RWSS	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}		-0.16[2]	0.00	RWSS,RWSH	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	WWS=0	-0.44	0.75	WWSS, WWSH	ns
		WWS>0	-0.11	1.00		
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}		0.14	0.50	MDAR, BMDAR, RWSH, WWSS	ns
			-0.57	0.69		

1. N/A since device captures data before it deasserts $\overline{RD}$
2. If RWSS = RWSH = 0, RD does not deassert during back-to-back reads and D=0.00 should be used.

4.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 1. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA}$ = 0 V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{RESET}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	11	ns	4-11
Minimum $\overline{RESET}$ Assertion Duration[3]	t_{RA}	30	—	ns	4-11
$\overline{RESET}$ Deassertion to First External Address Output	t_{RDA}	—	120T	ns	4-11
Edge-sensitive Interrupt Request Width	t_{IRW}	1T + 3	—	ns	4-12

Table 1. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 2] (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	18T	—	ns	4-13
	$t_{IDM\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	4-13
	$t_{IG\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[4]	t_{IRI}	22T	—	ns	4-14
	$t_{IRI\ -FAST}$	18T	—		
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Stop) to External Data Memory[5]	t_{IW}	1.5T	—	ns	4-15
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Wait) to External Data Memory Fast[6] Normal[7]	t_{IF}	 18T 22ET	 — —	 ns ns	4-15
$\overline{\text{RSTO}}$ pulse width[8] normal operation internal reset mode	t_{RSTO}	 128ET 8ET	 — —	 — —	4-16

1. In the formulas, T = clock cycle. For f_{op} = 120MHz operation and f_{ipb} = 60MHz, T = 8.33ns.
2. Parameters listed are guaranteed by design.
3. At reset, the PLL is disabled and bypassed. The part is then put into Run mode and t_{clk} assumes the period of the source clock, t_{xtal}, t_{extal} or t_{osc}.
4. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
5. The interrupt instruction fetch is visible on the pins only in Mode 3.
6. Fast stop mode:

   Fast stop recovery applies when external clocking is in use (direct clocking to XTAL) or when fast stop mode recovery is requested (OMR bit 6 is set to 1). In both cases the PLL and the master clock are unaffected by stop mode entry. Recovery takes one less cycle and t_{clk} will continue same value it had before stop mode was entered.
7. Normal stop mode:

   As a power saving feature, normal stop mode disables and bypasses the PLL. Stop mode will then shut down the master clock, recovery will take an extra cycle (to restart the clock), and t_{clk} will resume at the input clock source rate.
8. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125 ns.

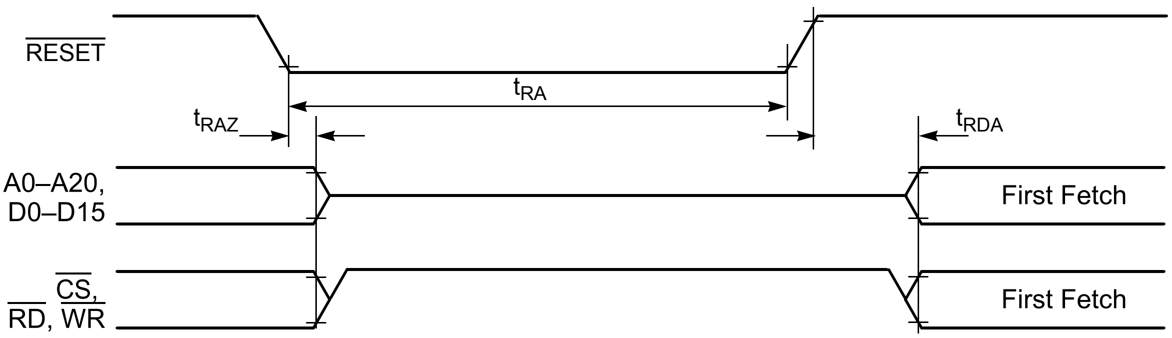


Figure 4-11 Asynchronous Reset Timing

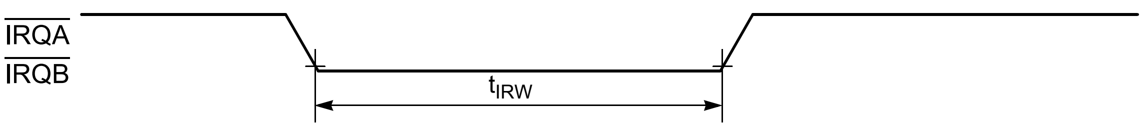


Figure 4-12 External Interrupt Timing (Negative-Edge-Sensitive)

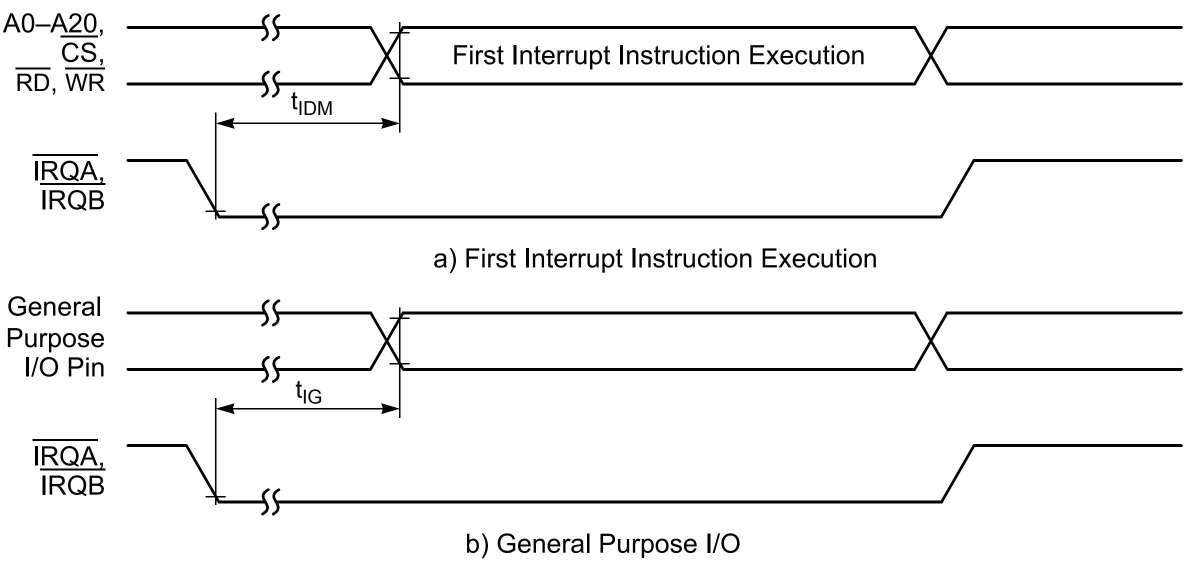


Figure 4-13 External Level-Sensitive Interrupt Timing

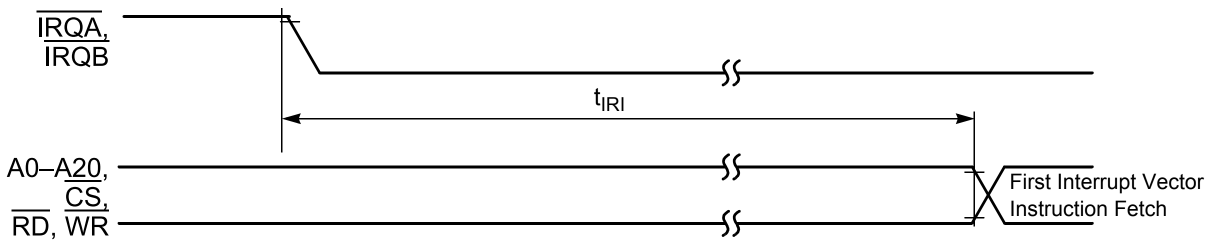


Figure 4-14 Interrupt from Wait State Timing

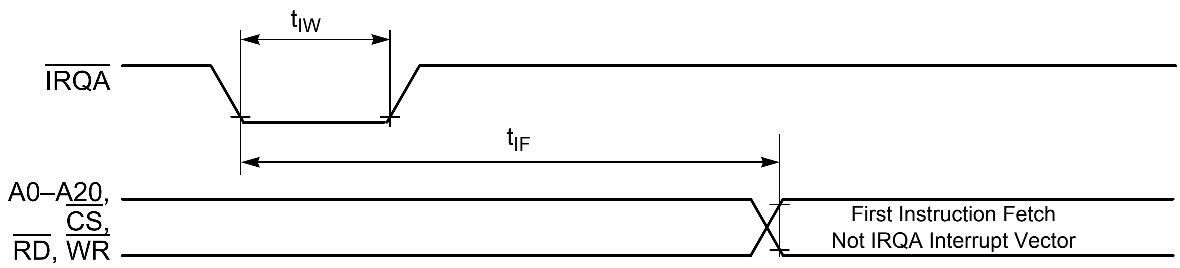


Figure 4-15 Recovery from Stop State Using Asynchronous Interrupt Timing

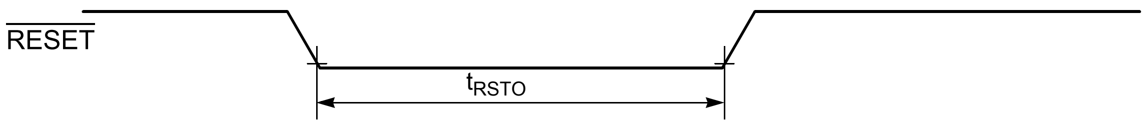


Figure 4-16 Reset Output Timing

4.8 Host Interface Port

Table 4-8 Host Interface Port Timing[1]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Access time	TACKDV	—	13	ns	4-17
Disable time	TACKDZ	3	—	ns	4-17
Time to disassert	TACKREQH	3.5	9	ns	4-17 4-20
Lead time	TREQACKL	0	—	ns	4-17 4-20

Table 4-8 Host Interface Port Timing[1] (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to +120°C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Access time	TRADV	—	13	ns	4-18 4-19
Disable time	TRADX	5	—	ns	4-18 4-19
Disable time	TRADZ	3	—	ns	4-18 4-19
Setup time	TDACKS	3	—	ns	4-20
Hold time	TACKDH	1	—	ns	4-20
Setup time	TADSS	3	—	ns	4-21 4-23
Hold time	TDSAH	1	—	ns	4-21 4-22
Pulse width	TWDS	5	—	ns	4-21 4-22
Time to re-assert 1. After second write in 16-bit mode 2. After first write in 16-bit mode or after write in 8-bit mode	TACKREQL	4T + 5 5	5T + 9 13	ns ns	4-17 4-20

1. The formulas: T = clock cycle. f ipb = 60MHz, T = 16.7ns.

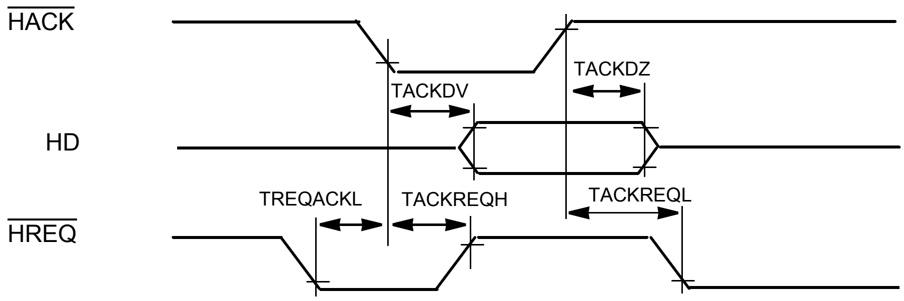


Figure 4-17 Controller-to-Host DMA Read Mode

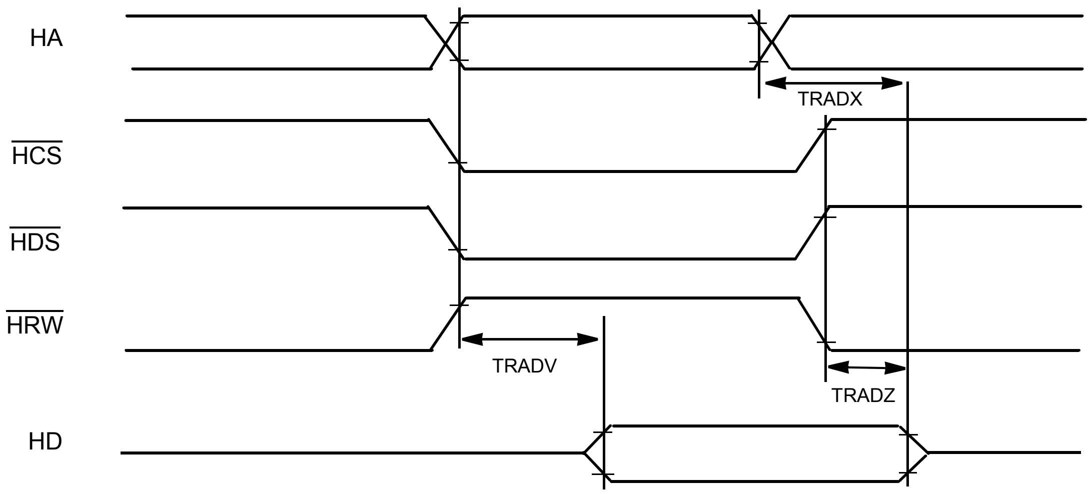


Figure 4-18 Single Strobe Read Mode

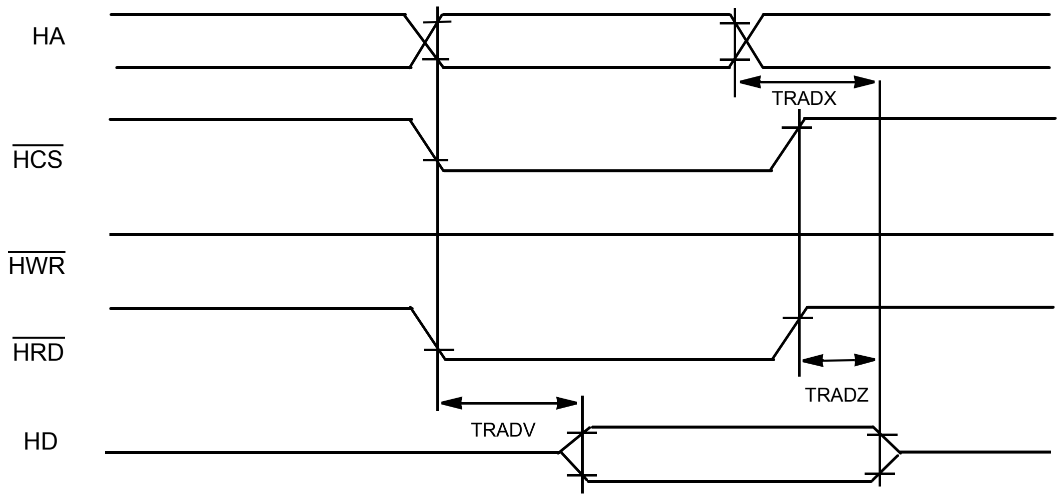


Figure 4-19 Dual Strobe Read Mode

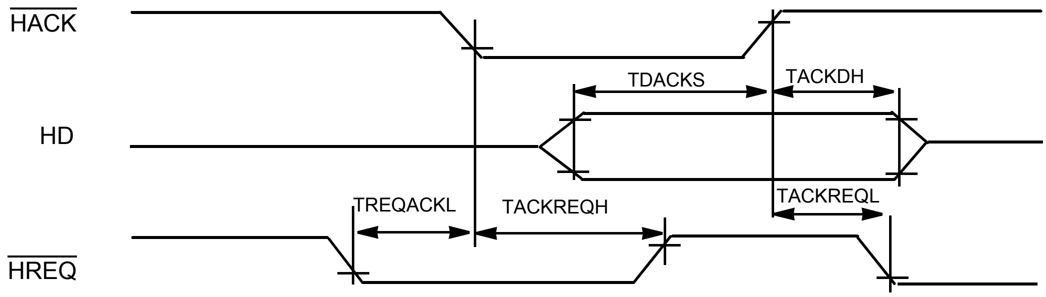


Figure 4-20 Host-to-Controller DMA Write Mode

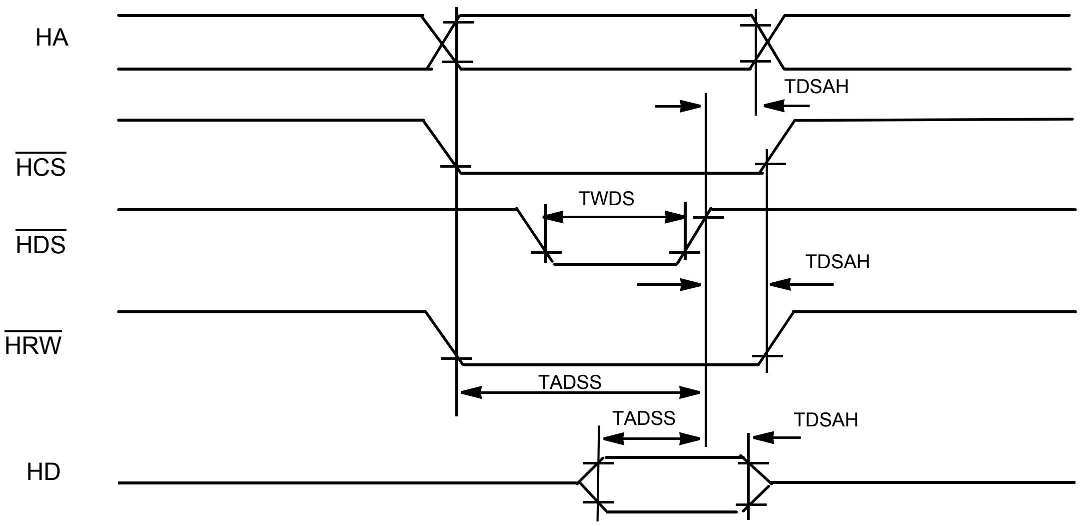


Figure 4-21 Single Strobe Write Mode

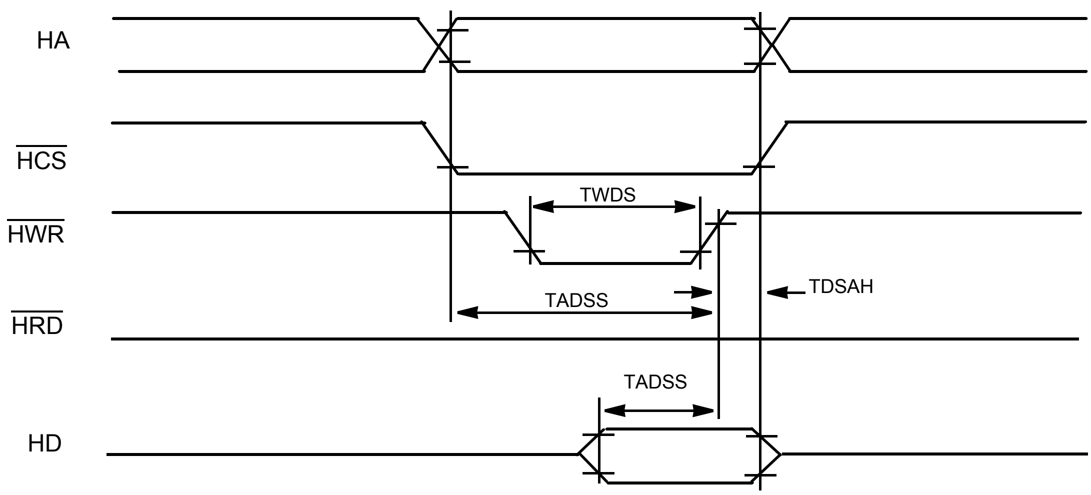


Figure 4-22 Dual Strobe Write Mode

4.9 Quad Timer Timing

Table 4-9 Quad Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	2T + 3	—	ns
Timer input high/low period	P_{INHL}	1T + 3	—	ns
Timer output period	P_{OUT}	2T - 3	—	ns
Timer output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For f_{op} = 120MHz operation and fipb = 60MHz, T = 8.33ns.
2. Parameters listed are guaranteed by design.

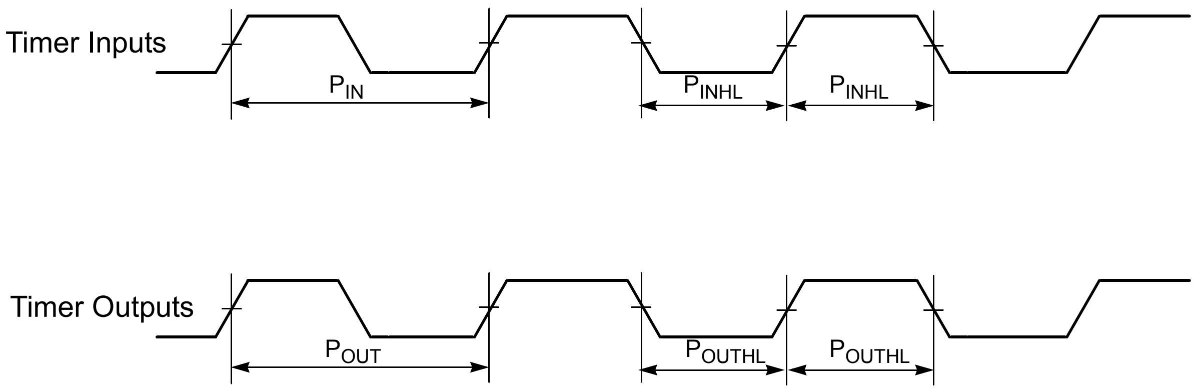


Figure 4-23 Timer Timing

4.10 Enhanced Synchronous Serial Interface (ESSI) Timing

Table 4-10 ESSI Master Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = –40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	fs	—	—	15[2]	MHz
SCK period[3]	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4[4]	—	—	ns
SCK low time	t_{SCKL}	33.4[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Master[5]	t_{TFSBHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) high - Master[5]	t_{TFSWHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) high - Master[5]	t_{RFSBHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) high - Master[5]	t_{RFSWHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (bl) low - Master[5]	t_{TFSBLM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) low - Master[5]	t_{TFSWLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) low - Master[5]	t_{RFSBLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) low - Master[5]	t_{RFSWLM}	-1.0	—	1.0	ns
SCK high to STD enable from high impedance - Master	t_{TXEM}	-0.1	—	2	ns
SCK high to STD valid - Master	t_{TXVM}	-0.1	—	2	ns
SCK high to STD not valid - Master	t_{TXNVM}	-0.1	—	—	ns
SCK high to STD high impedance - Master	t_{TXHIM}	-4	—	0	ns
SRD Setup time before SC0 low - Master	t_{SM}	4	—	—	ns
SRD Hold time after SC0 low - Master	t_{HM}	4	—	—	ns
Synchronous Operation (in addition to standard internal clock parameters)					
SRD Setup time before SCK low - Master	t_{TSM}	4	—	—	ns
SRD Hold time after SCK low - Master	t_{THM}	4	—	—	ns

1. Master mode is internally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for an 120MHz part.

3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.

4. 50 percent duty cycle

5. bl = bit length; wl = word length

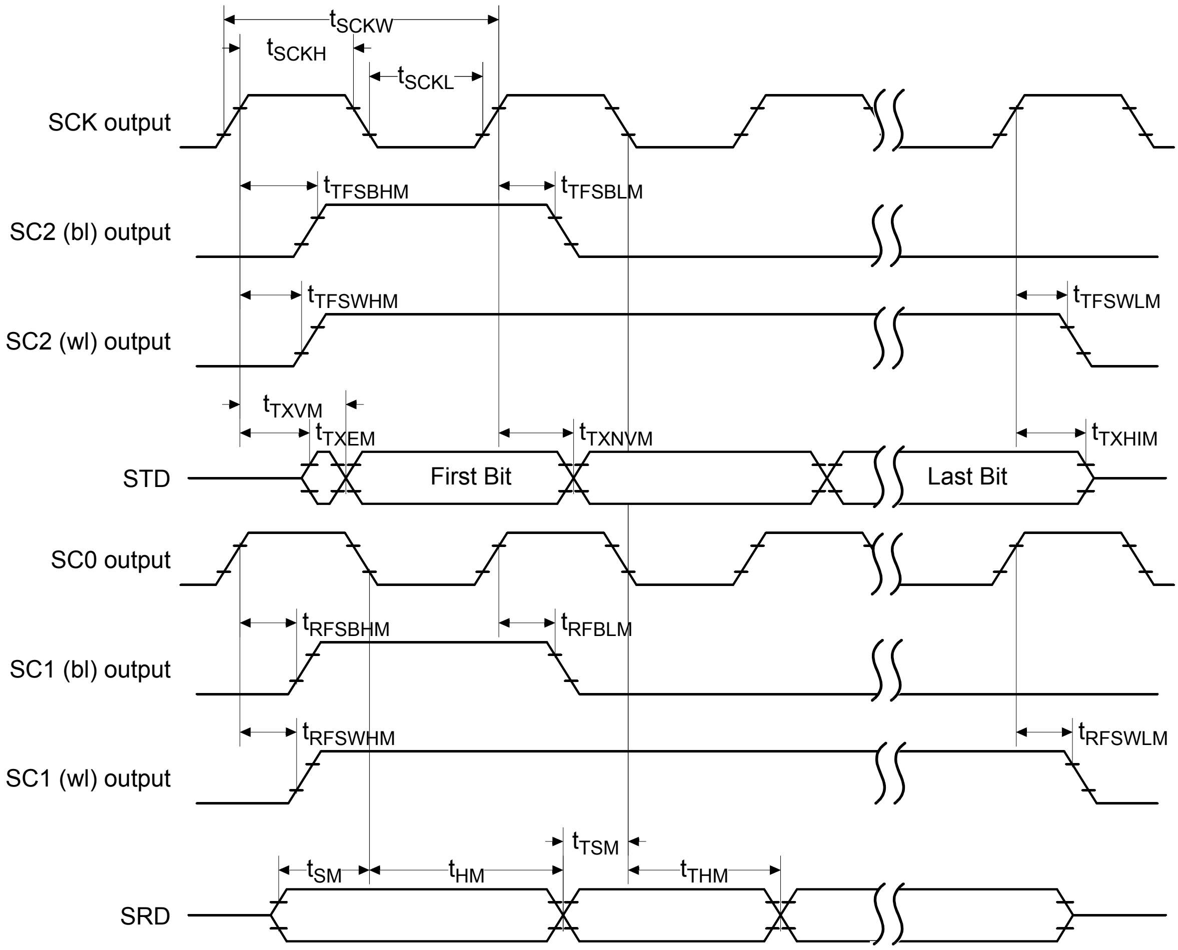


Figure 4-24 Master Mode Timing Diagram

Table 4-11 ESSI Slave Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	fs	—	—	15[2]	MHz
SCK period[3]	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4[4]	—	—	ns
SCK low time	t_{SCKL}	33.4[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Slave[5]	t_{TFSBHS}	-1	—	29	ns
Delay from SCK high to SC2 (wl) high - Slave[5]	t_{TFSWHS}	-1	—	29	ns
Delay from SC0 high to SC1 (bl) high - Slave[5]	t_{RFSBHS}	-1	—	29	ns
Delay from SC0 high to SC1 (wl) high - Slave[5]	t_{RFSWHS}	-1	—	29	ns
Delay from SCK high to SC2 (bl) low - Slave[5]	t_{TFSBLS}	-29	—	29	ns
Delay from SCK high to SC2 (wl) low - Slave[5]	t_{TFSWLS}	-29	—	29	ns
Delay from SC0 high to SC1 (bl) low - Slave[5]	t_{RFSBLS}	-29	—	29	ns
Delay from SC0 high to SC1 (wl) low - Slave[5]	t_{RFSWLS}	-29	—	29	ns
SCK high to STD enable from high impedance - Slave	t_{TXES}	—	—	15	ns
SCK high to STD valid - Slave	t_{TXVS}	4	—	15	ns
SC2 high to STD enable from high impedance (first bit) - Slave	t_{FTXES}	4	—	15	ns
SC2 high to STD valid (first bit) - Slave	t_{FTXVS}	4	—	15	ns
SCK high to STD not valid - Slave	t_{TXNVS}	4	—	15	ns
SCK high to STD high impedance - Slave	t_{TXHIS}	4	—	15	ns
SRD Setup time before SC0 low - Slave	t_{SS}	4	—	—	ns
SRD Hold time after SC0 low - Slave	t_{HS}	4	—	—	ns
Synchronous Operation (in addition to standard external clock parameters)					
SRD Setup time before SCK low - Slave	t_{TSS}	4	—	—	ns
SRD Hold time after SCK low - Slave	t_{THS}	4	—	—	ns

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for a 120MHz part.

3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.

4. 50 percent duty cycle

5. bl = bit length; wl = word length

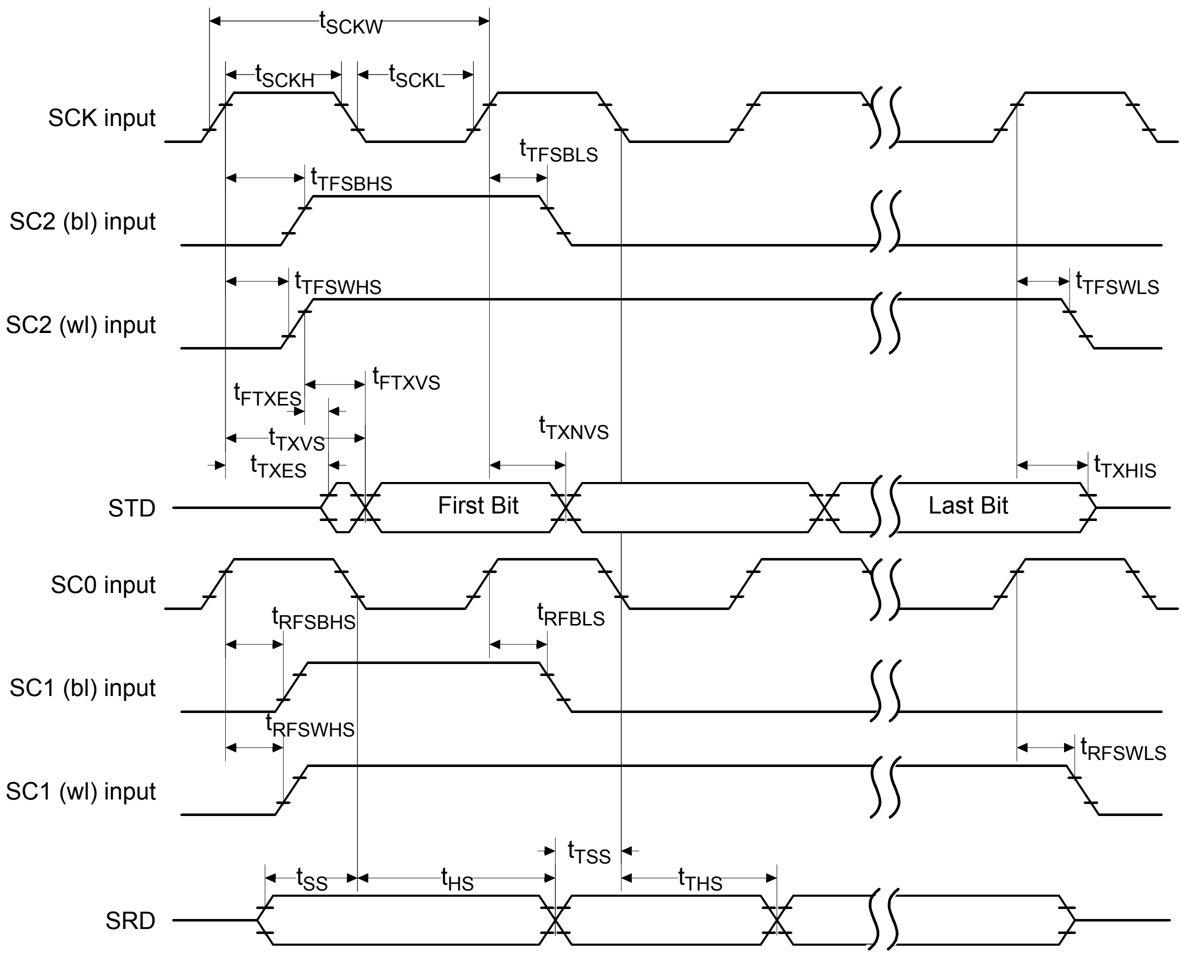


Figure 4-25 Slave Mode Clock Timing

4.11 Serial Communication Interface (SCI) Timing

Table 4-12 SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX})/(32)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

Figure 4-26 RXD Pulse Width

Figure 4-27 TXD Pulse Width

4.12 JTAG Timing

Table 4-13 JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	30	MHz
TCK cycle time	t_{CY}	33.3	—	ns
TCK clock pulse width	t_{PW}	16.6	—	ns
TMS, TDI data setup time	t_{DS}	3	—	ns
TMS, TDI data hold time	t_{DH}	3	—	ns
TCK low to TDO data valid	t_{DV}	—	12	ns
TCK low to TDO tri-state	t_{TS}	—	10	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	35	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 120MHz operation, T = 8.33ns.
2. TCK frequency of operation must be less than 1/4 the processor rate.
3. Parameters listed are guaranteed by design.

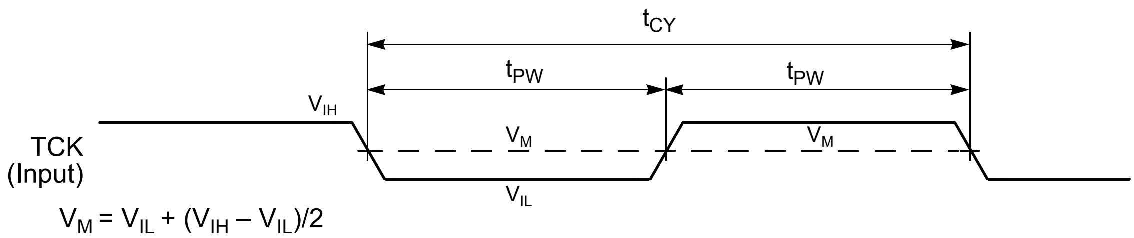


Figure 4-28 Test Clock Input Timing Diagram

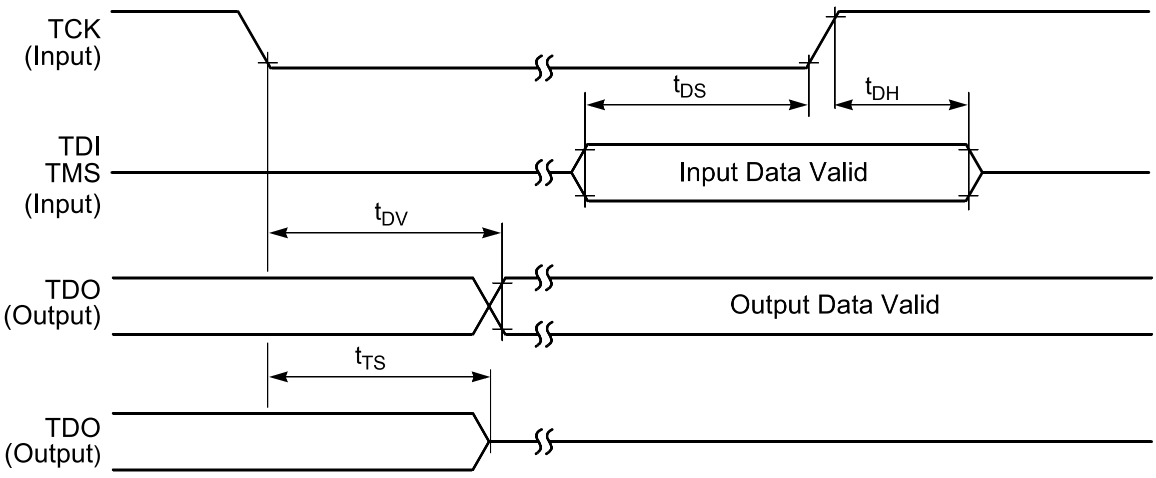


Figure 4-29 Test Access Port Timing Diagram

Figure 4-30 $\overline{\text{TRST}}$ Timing Diagram

Figure 4-31 Enhanced OnCE—Debug Event

4.13 GPIO Timing

Table 4-14 GPIO Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, V_{DD} = 1.62-1.98V, $V_{DDIO} = V_{DDA}$ = 3.0–3.6V, T_A = –40° to +120°C, $C_L \leq$ 50pF, f_{op} = 120MHz

Characteristic	Symbol	Min	Max	Unit
GPIO input period	P_{IN}	2T + 3	—	ns
GPIO input high/low period	P_{INHL}	1T + 3	—	ns
GPIO output period	P_{OUT}	2T - 3	—	ns
GPIO output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For f_{op} = 120MHz operation and fipb = 60MHz, T = 8.33ns
2. Parameters listed are guaranteed by design.

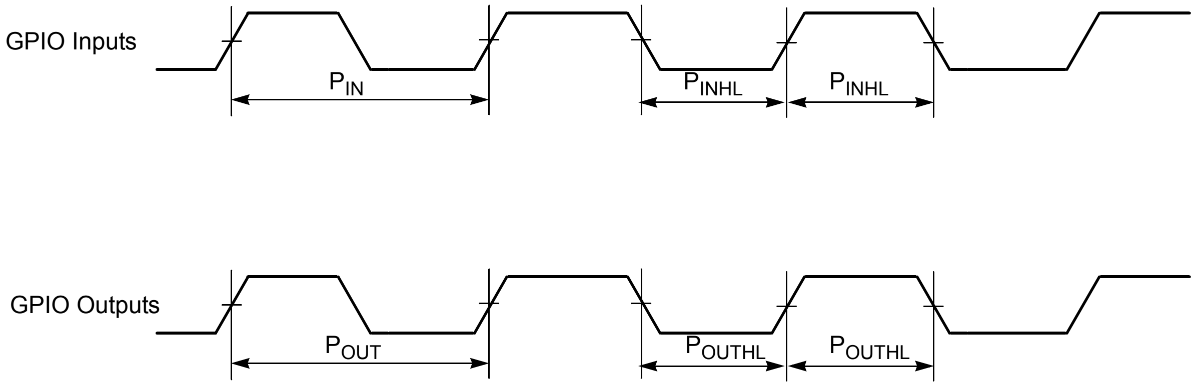


Figure 4-32 GPIO Timing

Part 5 Packaging

5.1 Package and Pin-Out Information 56855

This section contains package and pin-out information for the 100-pin LQFP configuration of the 56855.

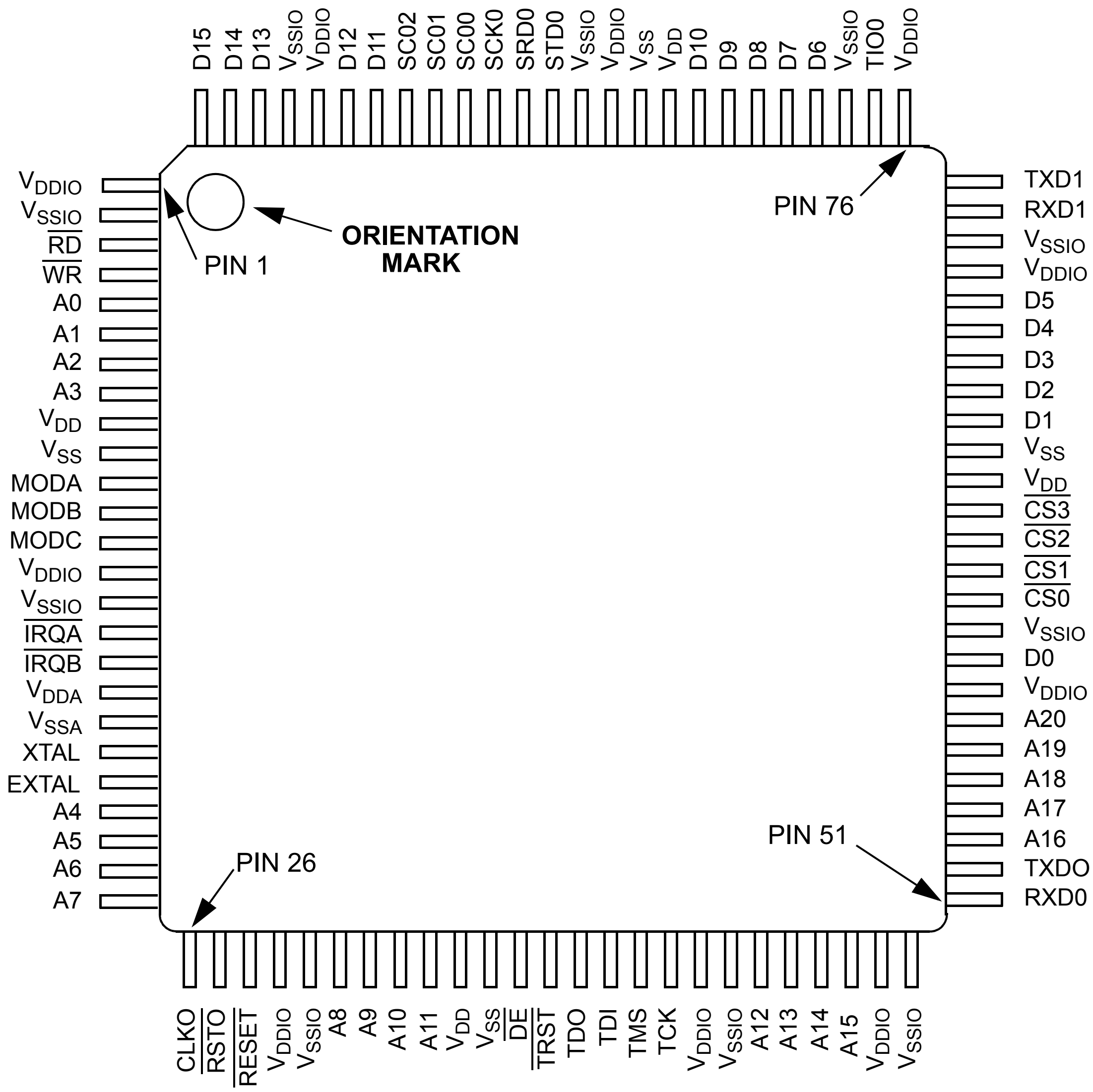
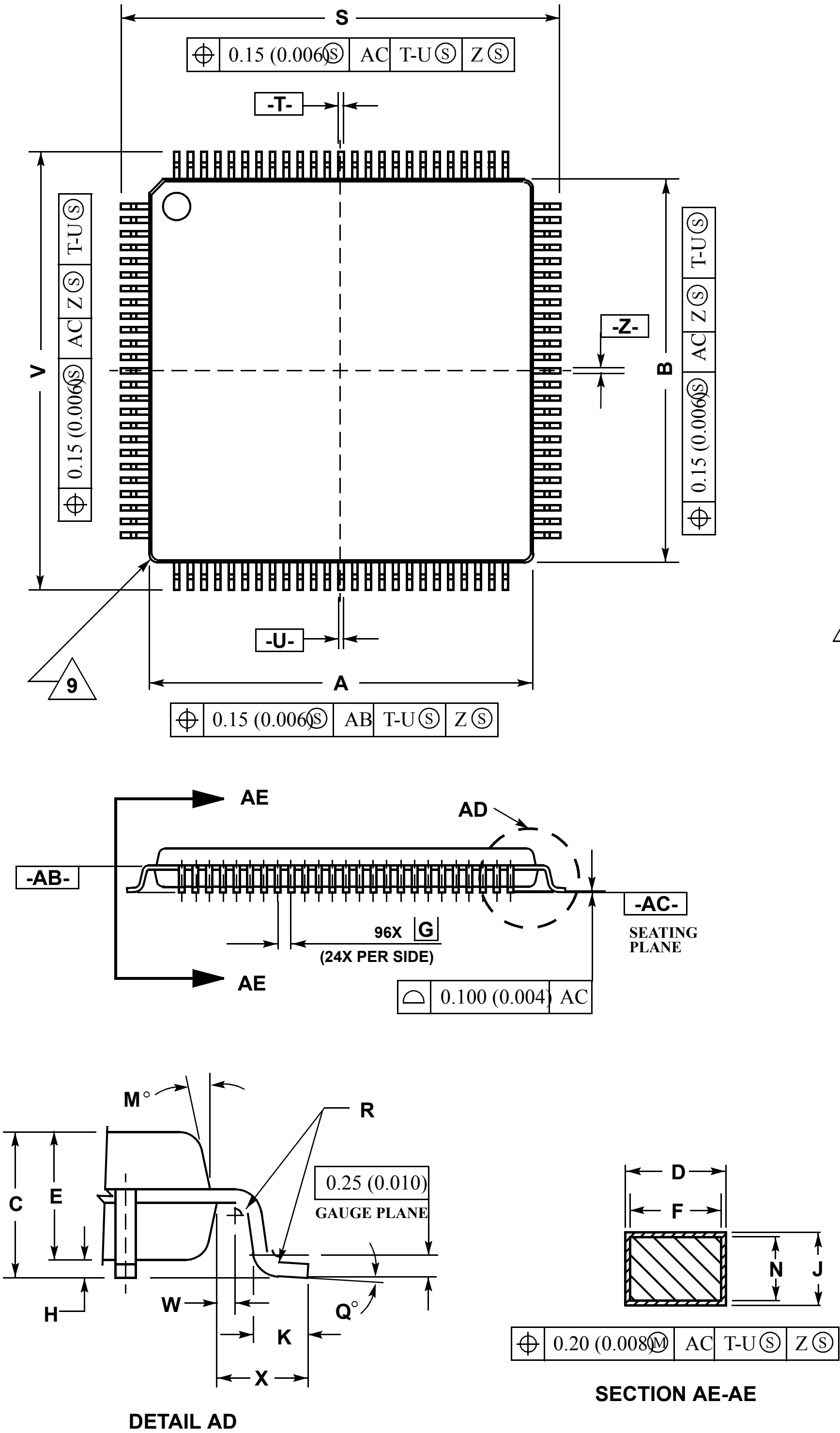


Figure 5-1 Top View, 56855 100-pin LQFP Package

Table 5-1 56855 Pin Identification By Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{DDIO}	26	CLKO	51	RXD0	76	V_{DDIO}
2	V_{SSIO}	27	$\overline{RSTO}$	52	TXD0	77	TIO0
3	$\overline{RD}$	28	$\overline{RESET}$	53	A16	78	V_{SSIO}
4	$\overline{WR}$	29	V_{DDIO}	54	A17	79	D6
5	A0	30	V_{SSIO}	55	A18	80	D7
6	A1	31	A8	56	A19	81	D8
7	A2	32	A9	57	A20	82	D9
8	A3	33	A10	58	V_{DDIO}	83	D10
9	V_{DD}	34	A11	59	D0	84	V_{DD}
10	V_{SS}	35	V_{DD}	60	V_{SSIO}	85	V_{SS}
11	MODA	36	V_{SS}	61	$\overline{CS0}$	86	V_{DDIO}
12	MODB	37	$\overline{DE}$	62	$\overline{CS1}$	87	V_{SSIO}
13	MODC	38	$\overline{TRST}$	63	$\overline{CS2}$	88	STD0
14	V_{DDIO}	39	TDO	64	$\overline{CS3}$	89	SRD0
15	V_{SSIO}	40	TDI	65	V_{DD}	90	SCK0
16	$\overline{IRQA}$	41	TMS	66	V_{SS}	91	SC00
17	$\overline{IRQB}$	42	TCK	67	D1	92	SC01
18	V_{DDA}	43	V_{DDIO}	68	D2	93	SC02
19	V_{SSA}	44	V_{SSIO}	69	D3	94	D11
20	XTAL	45	A12	70	D4	95	D12
21	EXTAL	46	A13	71	D5	96	V_{DDIO}
22	A4	47	A14	72	V_{DDIO}	97	V_{SSIO}
23	A5	48	A15	73	V_{SSIO}	98	D13
24	A6	49	V_{DDIO}	74	RXD1	99	D14
25	A7	50	V_{SSIO}	75	TXD1	100	D15



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014). DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.070 (0.003).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.950	14.050	0.549	0.553
B	13.950	14.050	0.549	0.553
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	15.950	16.050	0.628	0.632
V	15.950	16.050	0.628	0.632
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Figure 5-2 100-pin LQPF Mechanical Information

Please see **www.freescale.com** for the most current case outline.

Part 6 Design Considerations

6.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J – T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

6.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the controller, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1 μF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and GND.
- Bypass the V_{DD} and GND layers of the PCB with approximately 100 μF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the device’s output signals have fast rise and fall times, PCB trace lengths should be minimal.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the V_{DDA} and V_{SSA} pins.
- When using Wired-OR mode on the SPI or the $\overline{\text{IRQx}}$ pins, the user must provide an external pull-up device.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or Enhance OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- The internal POR (Power on Reset) will reset the part at power on with $\overline{\text{reset}}$ asserted or pulled high but requires that $\overline{\text{TRST}}$ be asserted at power on.

Part 7 Ordering Information

Table 7-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 7-1 56855 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56855	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	100	120	DSP56855BU120
DSP56855	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	100	120	DSP56855BUE *

*This package is RoHS compliant.

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