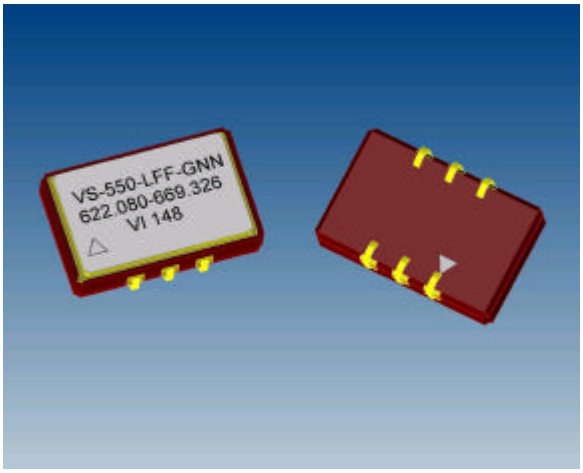
VECTRON INTERNATIONAL
A DOVER COMPANY

Preliminary Data Sheet

VS-550
Dual Frequency VCSO



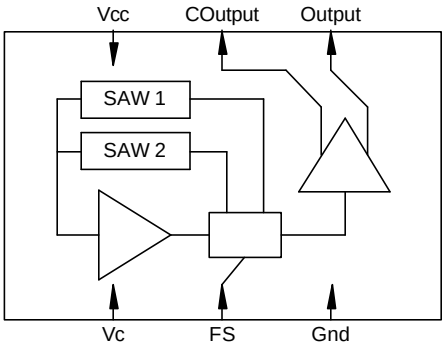
Features

- Industry Standard Package, 9 x 14 x 3.5 mm
- Output Frequencies from 500 MHz to 850 MHz
- 3.3 V Operation
- Low Jitter < 0.35 ps-rms across 50 kHz to 80 MHz
- LV-PECL Logic Levels with Fast Transition Times
- Complementary Outputs
- Frequency Select Feature

Applications

PLL circuits for Clock Smoothing and Frequency Translation

Description	Standard
• 10G Fibre Channel	INCITS/T11 Project 1413-D
• 10GbE LAN / WAN	IEEE 802.3ae
• OC-192	ITU-T G.709
• SONET / SDH	GR-253-CORE Issue3



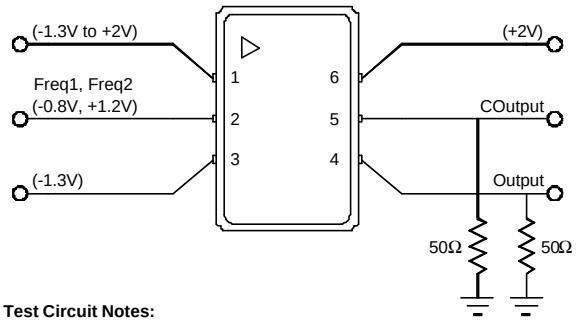
Description

The VS-550 is a SAW based voltage controlled oscillator that operates at the fundamental frequencies of the internal SAW filters. These SAW filters are high-Q quartz devices that enable the circuit to achieve low phase jitter performance over a wide operating temperature range. The dual oscillator is housed in a hermetically sealed J-lead surface mount package offered on tape and reel. It has a frequency select function that enables either “Frequency 1” or “Frequency 2.”

Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Nominal Frequency	f_N		500 - 850		MHz	1,2,3
Absolute Pull Range	APR	±50			ppm	1,2,3,8
Linearity	Lin		±5		%	2,4,8
Gain Transfer (See Pg 5)	K_V		+385		ppm/V	2,8
Temperature Stability	f_{STAB}		±100		ppm	1,6
Transition Time			4		µsec	6
Supply						
Voltage	V_{CC}	2.97	3.3	3.63	V	2,3
Current (No Load)	I_{CC}		55	70	mA	3
Outputs						
Mid Level		V_{CC}-1.5	V_{CC}-1.3	V_{CC}-1.1	V	2,3
Swing		500	650	800	mV-pp	2,3
Current	I_{OUT}			20	mA	6
Rise Time	t_R		250	400	ps	5,6
Fall Time	t_F		250	400	ps	5,6
Symmetry	SYM	45	50	55	%	2,3
Spurious Suppression		50	60		dBc	6
Jitter (See Pg 5)	ϕJ		0.300		ps-rms	6,7
Control Voltage						
Input Impedance	Z_c		100		kΩ	6
Modulation Bandwidth	BW		500		kHz	6
Operating Temperature	T_{OP}	-40		85	°C	1,3
Package Size		9.0 x 14.0 x 3.5			mm	

1. See Standard Frequencies and Ordering Information (Pg 7).
2. Parameters are tested with production test circuit below (Fig 1).
3. Parameters are tested at ambient temperature with test limits guardbanded for specified operating temperature.
4. Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5. Measured from 20% to 80% of a full output swing (Fig 2).
6. Not tested in production, guaranteed by design, verified at qualification.
7. Integrated across 50 kHz to 80 MHz, per GR-253-CORE Issue3.
8. Tested with Vc = 0.3V to 3.0V.



Test Circuit Notes:
1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
3) 50Ω Terminations are Within Test Equipment.

Figure 1. Test Circuit

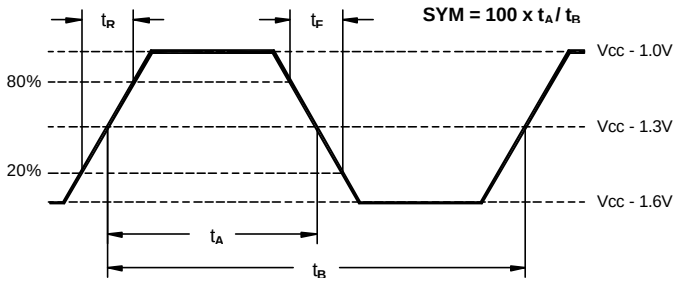
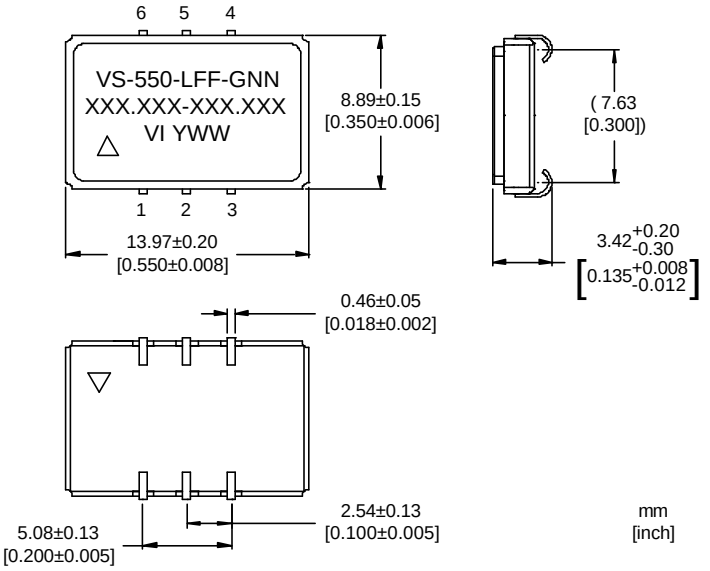
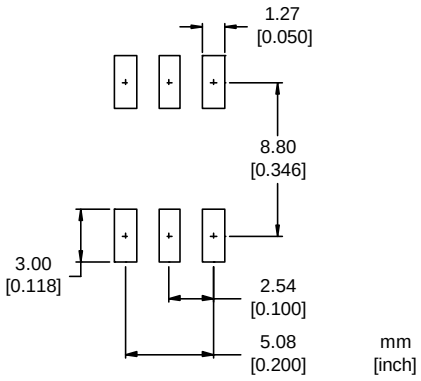


Figure 2. 100K LV-PECL Waveform

Outline Diagram



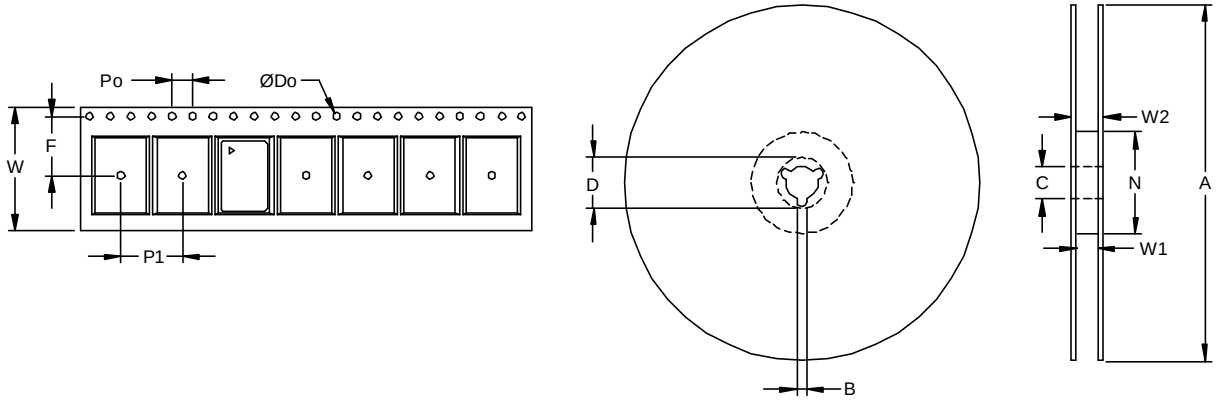
Pad Layout



Pin Out

Pin	Symbol	Function
1	V_C	VCSO Control Voltage
2	FS	Frequency Select Frequency 1 = 0.0 to 0.5 V Frequency 2 = 2.5 to 3.3 V
3	GND	Case and Electrical Ground
4	Output	VCSO Output
5	COutput	VCSO Complementary Output
6	V_{CC}	Power Supply Voltage (3.3 V ±10%)

Tape and Reel (EIA-481-2-A)



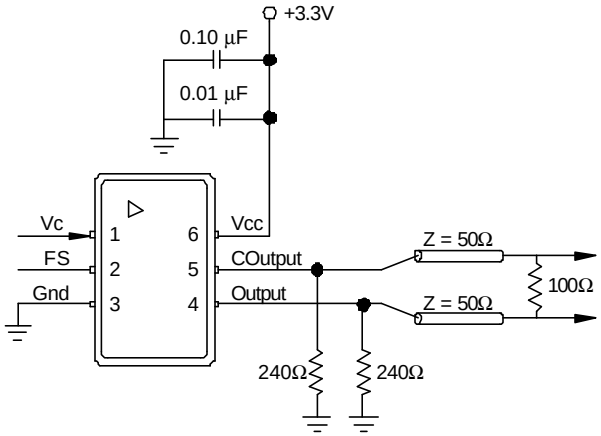
Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
VS-550	24	11.5	1.5	4	12	330	1.5	13	20.2	100	24.4	30.4	200

Absolute Maximum Ratings

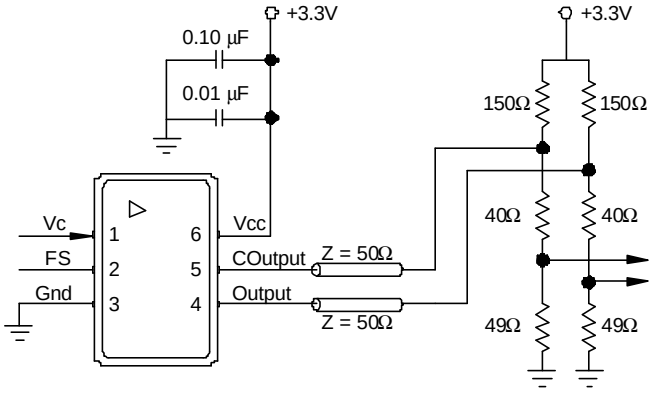
Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Output Current	Iout	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	220/10	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

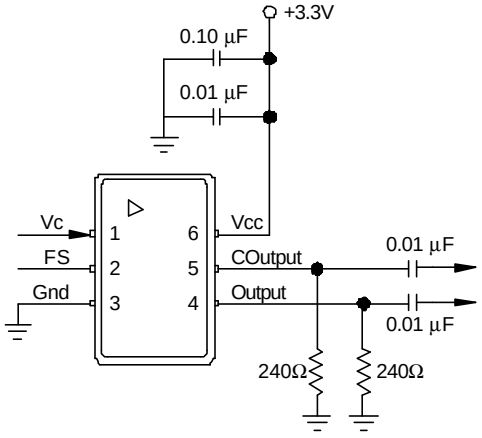
Suggested Output Load Configurations



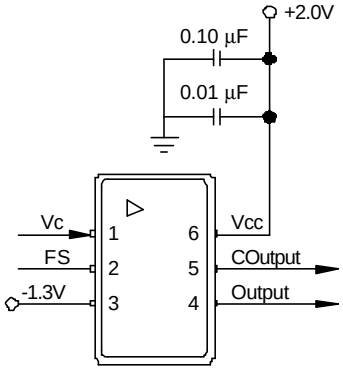
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.

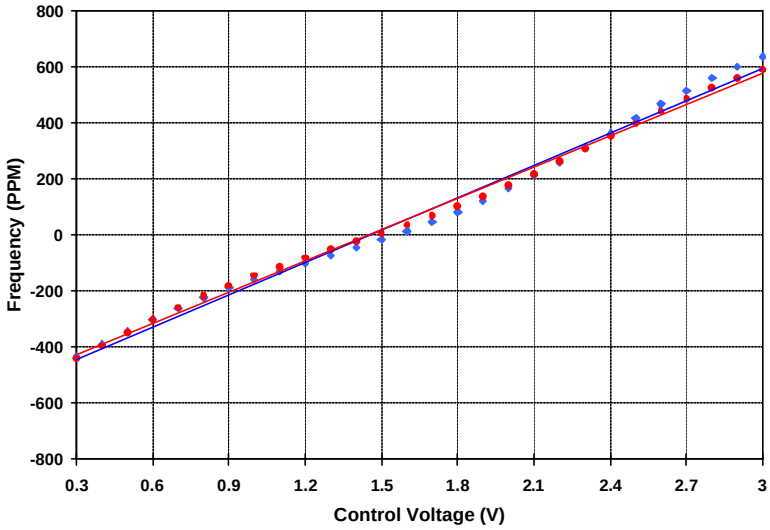


Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplies as shown. Similar to Figure 1.

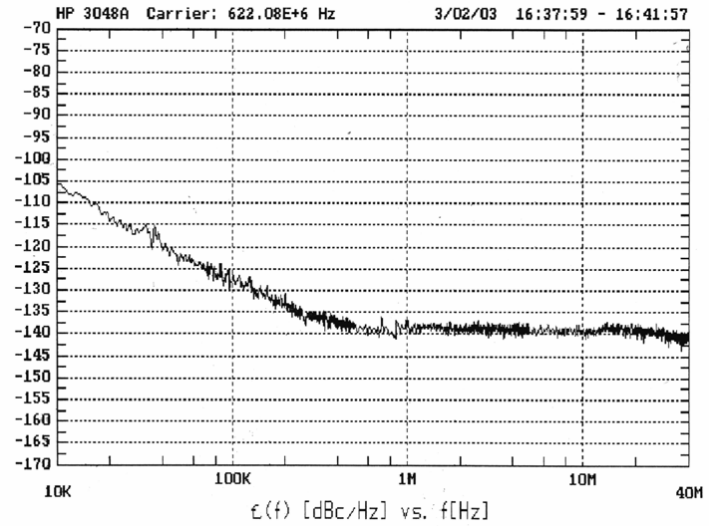
Typical Characteristics



At Ambient (22.5°C)

Typical Gain Transfer @ 622.0800 = +385 ppm/V

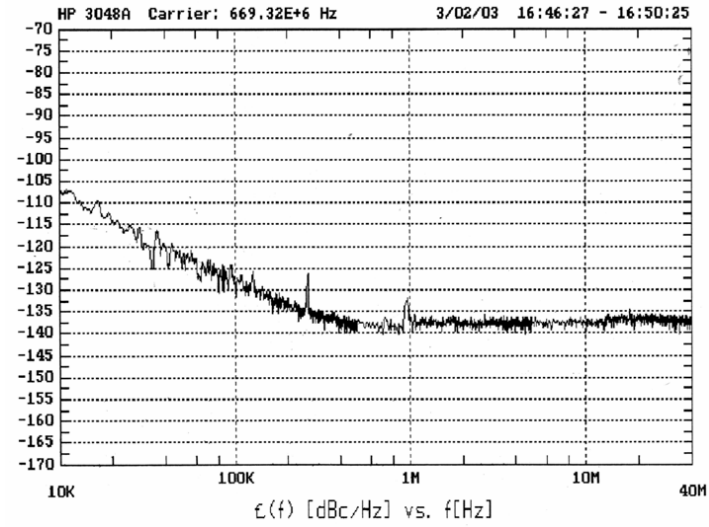
Typical Gain Transfer @ 669.3266 = +370 ppm/V



Typical Calculated Jitter @ 622.0800 MHz

SONET OC-48 (12kHz-20MHz) = 0.254 ps-rms; 1.78 ps-pp

SONET OC-192 (50kHz-80MHz) = 0.268 ps-rms; 1.88 ps-pp



Typical Calculated Jitter @ 669.3266 MHz

SONET OC-48 (12kHz-20MHz) = 0.323 ps-rms; 2.26 ps-pp

SONET OC-192 (50kHz-80MHz) = 0.308 ps-rms; 2.16 ps-pp

Reliability

The VS-550 family is capable of meeting the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

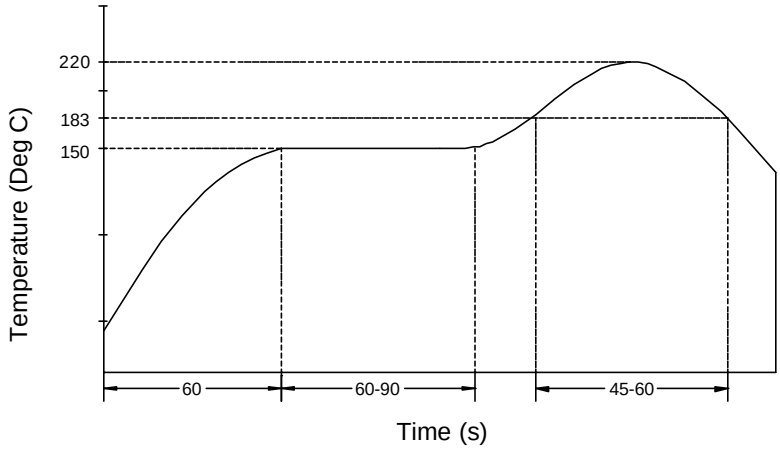
Handling Precautions

Although ESD protection circuitry has been designed into the VS-550 proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings

Model	Minimum	Conditions
Human Body Model	500	MIL-STD 883, Method 3015
Charged Device Model	500	JESD 22-C101

Recommended Solder Reflow Profile



VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The conditions a device can withstand are well understood and devices can be subjected to the profile above. This profile shows a ramp up condition to prevent thermal shock, a preheat period in which the flux is activated, a ramp up to 183°C which is the reflow temperature of Sn/Pb eutectic, and a gradual cool down. The time above 183°C should not exceed 60 seconds and the peak temperature should be no more than 220°C for 10 seconds. The VS-550's are hermetically sealed so an aqueous wash is not an issue.

Standard Frequencies (MHz)

Frequency 1			Frequency 2		
622.0800 **P2**	625.0000 **P3**	644.5313 **P4**	625.0000 **P3**	644.5313 **P4**	657.4219 **PB**
666.5143 **P5**	669.3266 **R3**		666.5143 **P5**	669.3266 **R3**	672.1627 **R5**
			690.5692 **R4**	693.4830 **R6**	

1. **Other frequencies available upon request, please contact VI for details.**
2. **Frequency 1 must be lower than Frequency 2. Not all combinations are available.**

Ordering Information

VS - 550 - L F F - G N N – P2 – R3

Product Family
VS: VCSO

Package
550: 9 x 14 x 3.5 mm

Input
L: 3.3 V

Output
F: LV-PECL

Operating Temperature
F: -40 to 85 °C

Absolute Pull Range
G: +/- 50 ppm
H: +/- 100 ppm

Other (Future Use)
N: N/A

Other (Future Use)
N: N/A

Frequency 1 (See Above)
P2 – R3

Frequency 2 (See Above)
P3 – R6

For Additional Information, Please Contact:

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