Product Brief
DAEDALUS
SDA 9410

Display Processor and Scan Rate Converter Using Embedded DRAM Technology Units

Potential Application

The SDA 9410 is a new component of the Infineon MEGAVISION IC set for building high end TV sets

- 100/120 Hz interlaced TV sets
- 50/60 Hz progressive scan TV sets

Features

New Application Modes

- High performance scan rate converter supporting true motion
- Double source input supporting high resolution frame based PIP and double window.

Two Input Channels with Two Data Formats

- Two input channels
- ITU-R 656 data format, 8 wires data only or 8 wires including sync information
- ITU-R 601 4:2:2 data format, luminance and chrominance parallel (2x8 wires)

Vertical peaking of the input signal

Noise Reduction

- Motion adaptive spatial and temporal noise reduction (3D-NR)
- Temporal noise reduction for luminance and chrominance, frame based or field based
- Flexible programming of the temporal noise reduction characteristics
- Automatic measurement of the noise level

3D Predictive Motion Estimation

- High performance motion estimation based on block matching algorithm
- Film mode and phase detector 25 Hz PAL and 30 Hz NTSC - 2-3 pull down
- Global motion flag; readable by I^2C Bus

Automatic detection of letter box formats (readable by I^2C Bus)

Embedded DRAM Core

- 6 MBit embedded DRAM core for field memories
- 1.1 MBit embedded DRAM core for line memories, vector memory, block-to-line converter, line-to-block converter
- 36 kBit SRAM for block matching

Flexible Clock and Synchronization Concept

- Decoupling of the input and output clock system possible (free run and locked modes)

Scan Rate Conversion

- Motion compensated 100/120 Hz interlaced scan conversion (Infineon VDU)
- Motion compensated 50/60 Hz progressive scan conversion (Infineon VDU) (Vector Driven Upconversion)
- Simple interlaced modes: ABAB, AABB, AAAA, BBBB
- True Motion: 50 (60) Hz motion resolution even for 25 (30) Hz film sources
- Large area and line flicker reduction

Flexible compression and expansion of the input signals

- Horizontal and vertical compression and expansion of both input channels individually
- Panorama mode
- Support of split-screen applications e.g. Text

High Performance Display Processing

- Digital colour transition improvement (DCTI)
- Digital luminance transition improvement (DLTI)
- Peaking (luminance only)
- Three 9-Bit D/A converters (two fold oversampling)

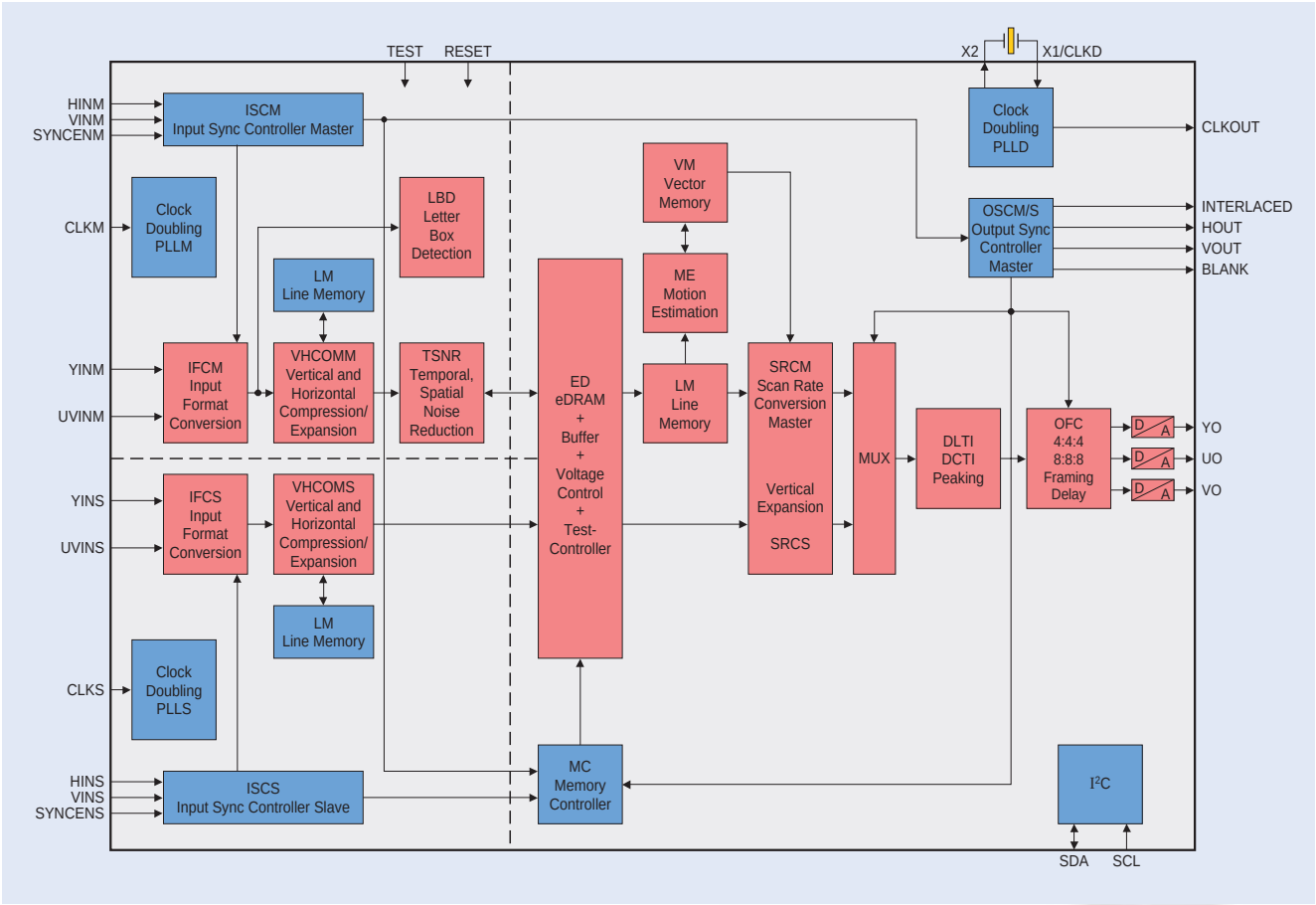
Flexible Output Sync Controller

- Flexible positioning of the two output channels in all application modes
- Flexible height and width of the two output pictures
- Flexible programming of the output sync raster

Signal Manipulations

- Still frame or field
- Insertion of coloured background
- Insertion of a selection border
- Adjustable delay between Y and UV signal at the in- and output

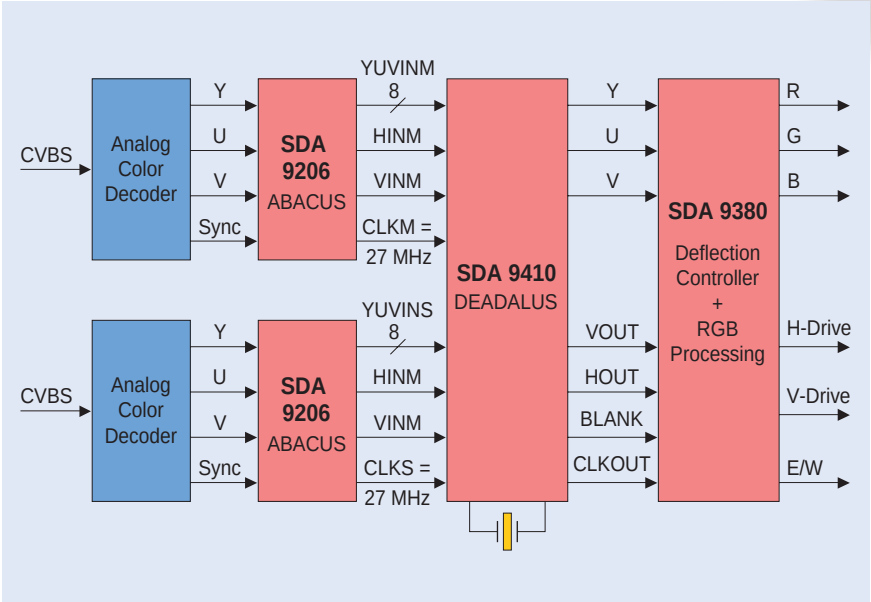
Block Diagram



Technical Data

- I²C-Bus control (400 kHz)
- P-MQFP-100 package
- 3.3 V (± 5%) supply voltage
- 4:2:2 input data format (internal 4:2:0 or 4:1:1 processing)
- 0.35 µm embedded DRAM technology
- Power consumption less than 1.8 W

Application Example



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