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STD5N95K3, STF5N95K3
STP5N95K3, STU5N95K3

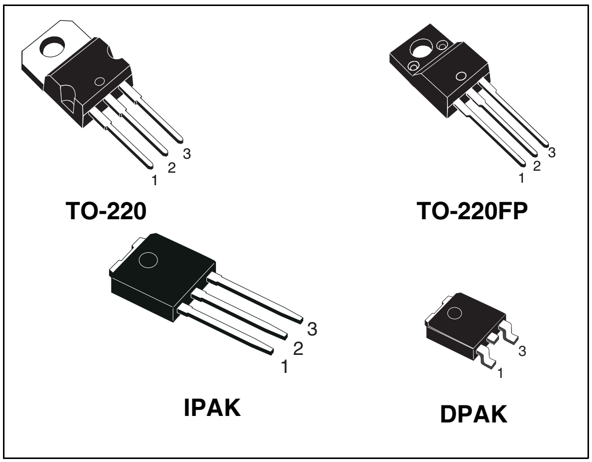
N-channel 950 V, 2.5 Ω, 3.5 A, DPAK, TO-220, TO-220FP, IPAK SuperMESH3™ Power MOSFET

Preliminary data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	P_w
STD5N95K3	950 V	< 3 Ω	3.5 A	90 W
STF5N95K3	950 V	< 3 Ω	3.5 A	25 W
STP5N95K3	950 V	< 3 Ω	3.5 A	90 W
STU5N95K3	950 V	< 3 Ω	3.5 A	90 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected



Application

- Switching applications

Description

The new SuperMESH3™ series of power MOSFETS is the result of the fine-tuning of ST's well-established strip-based PowerMESH™ layout with a new optimized vertical structure. The innovative design offer significantly reduced on-resistance, exceptional dynamic performance and very large avalanche capability, making the device suitable for the most demanding applications.

Figure 1. Internal schematic diagram

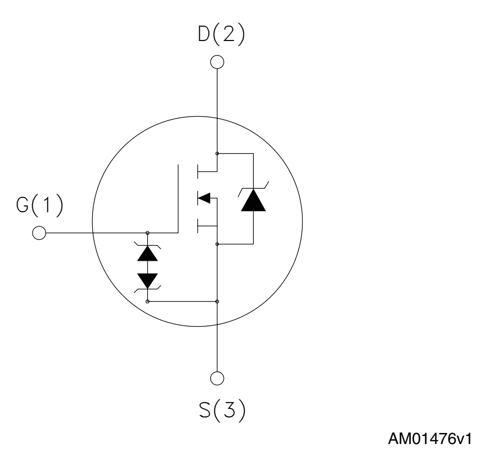


Table 1. Device summary

Order code	Marking	Package	Packaging
STD5N95K3	5N95K3	DPAK	Tape and reel
STF5N95K3	5N95K3	TO-220FP	Tube
STP5N95K3	5N95K3	TO-220	Tube
STU5N95K3	5N95K3	IPAK	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	TO-220FP	IPAK	DPAK	
V_{GS}	Gate- source voltage	30				V
I_D	Drain current (continuous) at T_C = 25 °C	3.5	3.5[1]	3.5		A
I_D	Drain current (continuous) at T_C = 100 °C	2.2	2.2[1]	2.2		A
I_{DM} [2]	Drain current (pulsed)	14	14[1]	14		A
P_{TOT}	Total dissipation at T_C = 25 °C	90	25	90		W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4.4				A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	TBD				mJ
dv/dt[3]	Peak diode recovery voltage slope	6				V/ns
V_{ISO}	Insulation withstand voltage (AC)		2500			
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150				°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 3.5$ A, di/dt $\leq$ 100 A/µs, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	TO-220FP	IPAK	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.39	5	1.39		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.50				°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max				50	°C/W
T_J	Maximum lead temperature for soldering purpose	300				°C/W

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2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	950			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V; V_{DS}=0			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.75 A		2.5	3	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} [1]	Forward transconductance	V_{DS} = 15 V, I_D = 1.75 A	-	TBD	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	455 48 1	-	pF pF pF
$C_{o(tr)}$ [2]	Equivalent capacitance time related	V_{DS} = 0 to 760 V, V_{GS} = 0	-	TBD	-	pF
$C_{o(er)}$ [3]	Equivalent capacitance energy related	V_{DS} = 0 to 760 V, V_{GS} = 0	-	TBD	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	4.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 760 V, I_D = 3.5 A, V_{GS} = 10 V *(see Figure 3)*	-	13 TBD TBD	-	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
3. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

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Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 475 V, I_D = 1.75 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 2)*	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		3.5 14	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 3.5 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 3.5 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 4)*	-	TBD TBD TBD		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 3.5 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 4)*	-	TBD TBD TBD		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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3 Test circuits

Figure 2. Switching times test circuit for resistive load

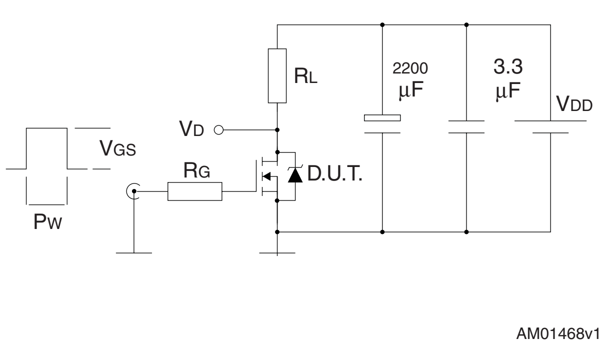


Figure 3. Gate charge test circuit

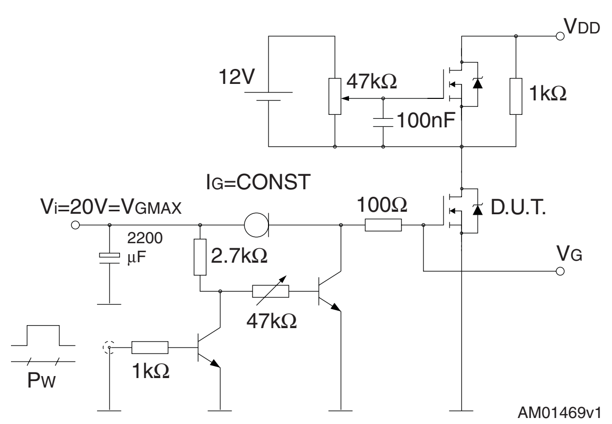


Figure 4. Test circuit for inductive load switching and diode recovery times

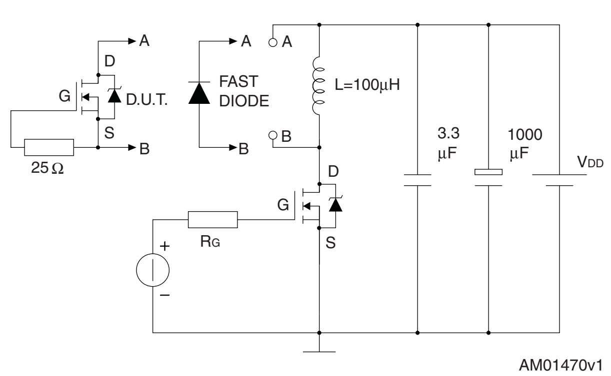


Figure 5. Unclamped inductive load test circuit

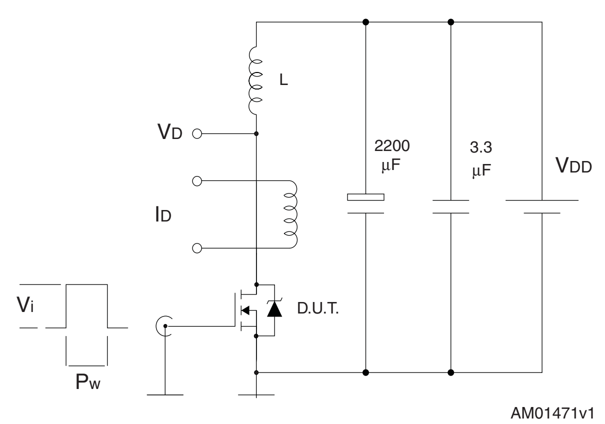


Figure 6. Unclamped inductive waveform

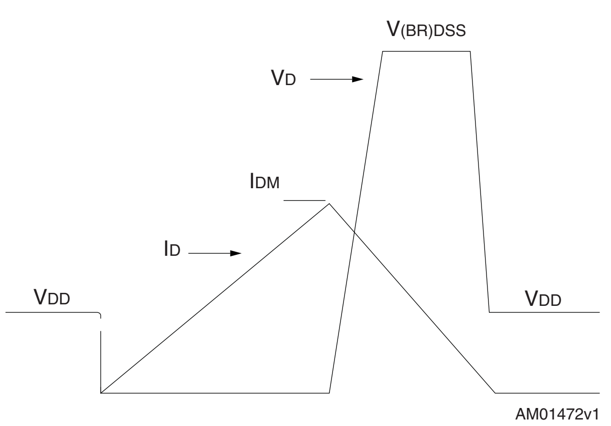
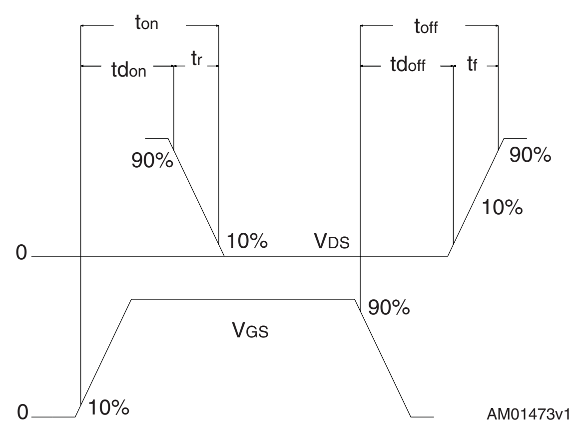


Figure 7. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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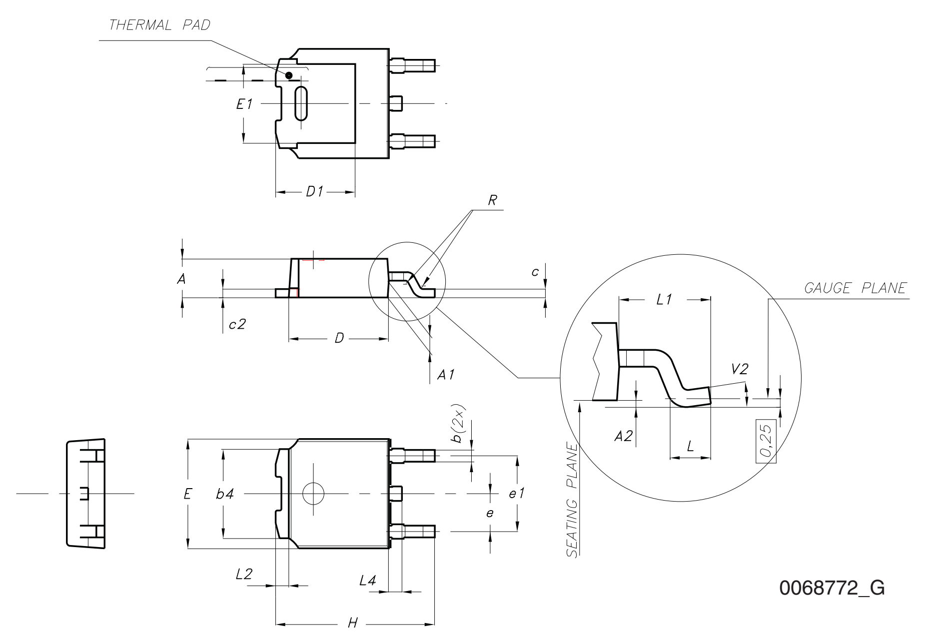
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



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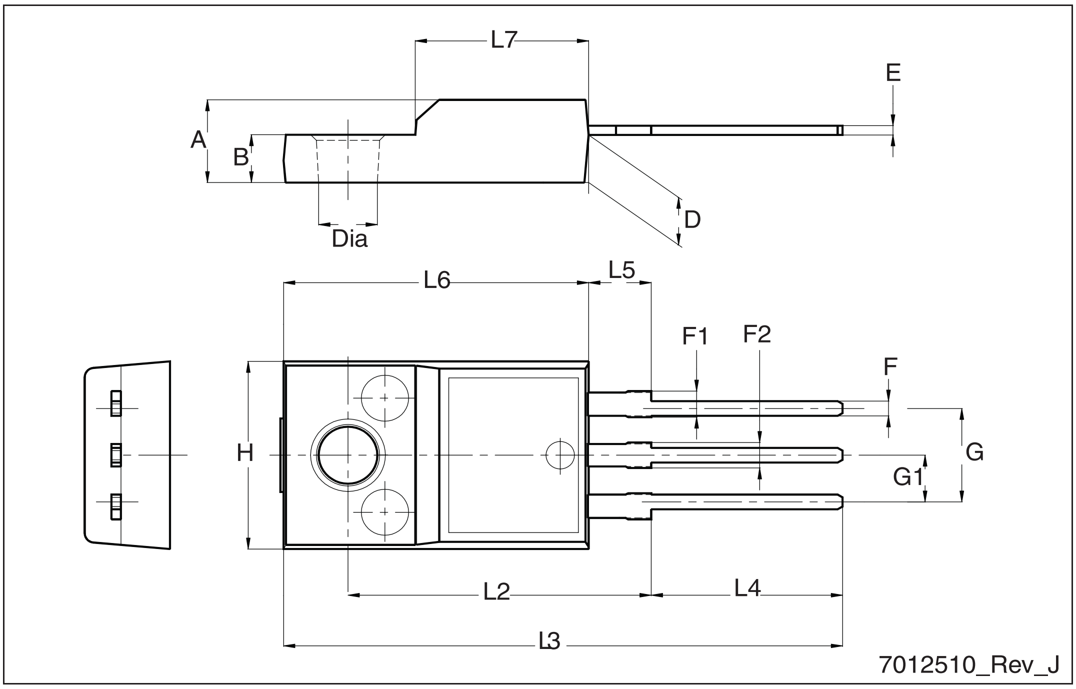
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



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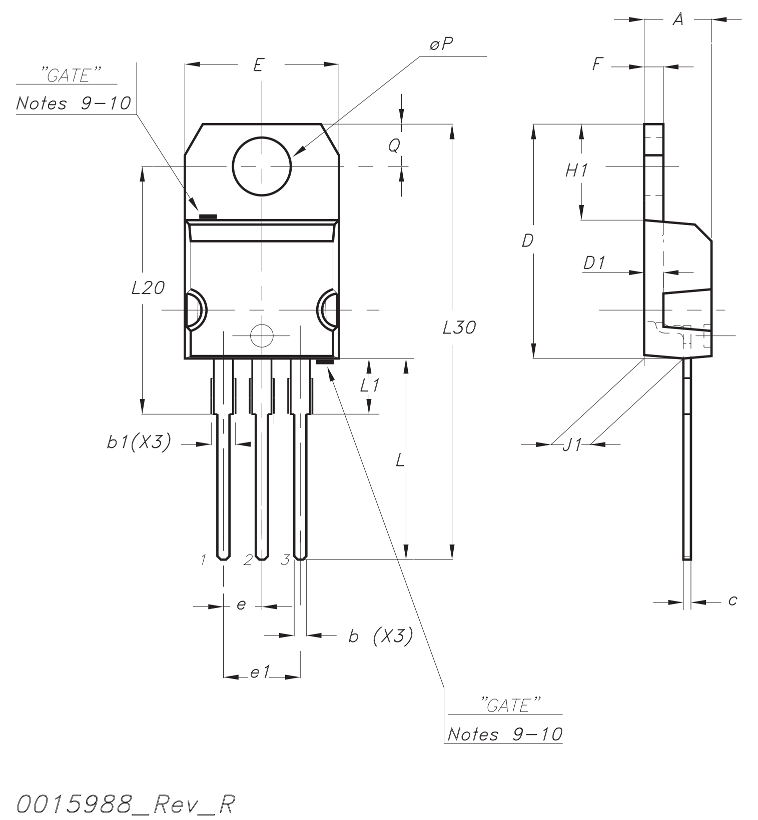
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



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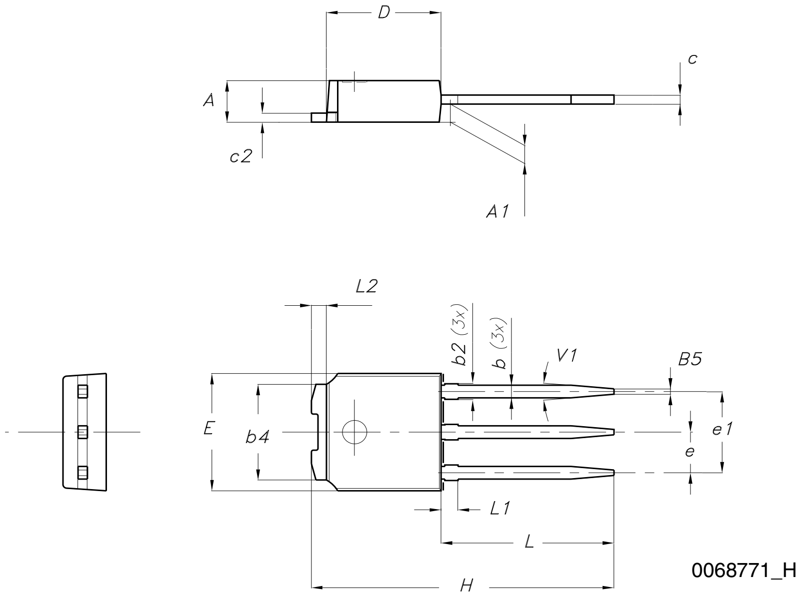
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	



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5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-May-2009	1	First release

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