T-46-07-09

GigaBit Logic

10G023
10G023K

Quad D Flip Flop with 2:1 Muxed Inputs 1.9 GHz Clock Rate
10G PicoLogic™ Family

FEATURES

- 850 ps typical clock to output delay
- Individual or common clock inputs
- Differential outputs with common output enable control
- Common asynchronous clear control
- Temperature and voltage compensated design
- ≤ 50 ps clock to output delay skew
- ECL and PicoLogic™ compatible I/O
- Ouput Wire-OR capability
- Available in 40 pin C-Leaded or Leadless chip carriers and dice form
- Extended Temp. Range: -40°C to +100°C (10G023K)

APPLICATIONS

- Registered data or address MUX
- Pipeline register
- High speed state machines
- High speed status register

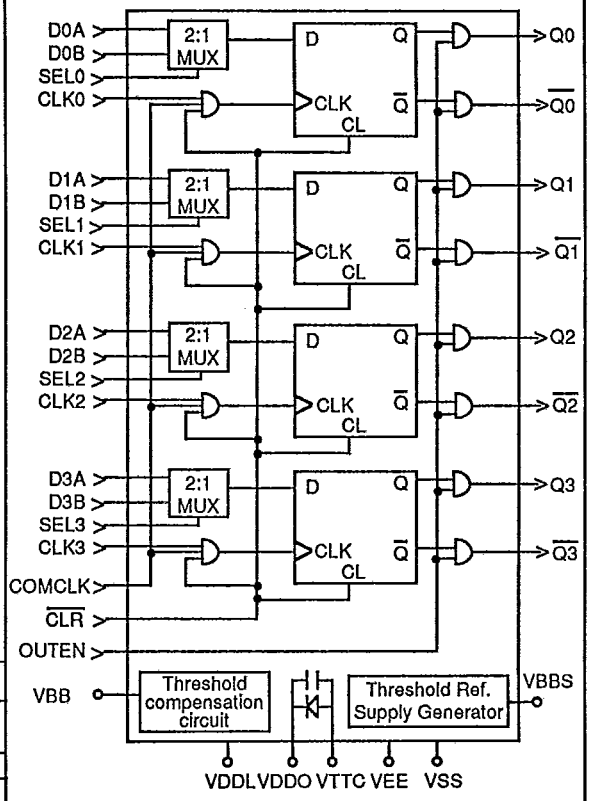
FUNCTIONAL DESCRIPTION

The 10G023 is an ultra-high speed quad D-type flip flop with individually 2:1 multiplexed data inputs (D0A-D3A, D0B-D3B). Data to each of the four stages is selected by an individual select control (SEL0-SEL3) and is latched into the flipflop by the rising edge of either the individual clock inputs (CLK0-CLK3) or the common clock input (COMCLK). An active low common clear (CLR) input is provided for resetting the Q output of each flip flop asynchronously to a low level. All device outputs can be disabled (brought low), without interfering with the current state of the flip flop, via the output enable (OUTEN) control. This permits wired-OR bus connection.

The 10G023 can be clocked at 2.1 GHz typically The operating frequency of the SEL input is much greater than half the clock frequency. Typical clock to output delay is 850 ps and the skew in output delay time is tightly matched to 30 ps typically which results in a highly symmetric output eye pattern.

The 10G023/023K is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G023 ORDERING INFORMATION

PKG. TYPE	Min. Speed 0°C to 85°C		Min. Speed -40°C to +100°C
	1.9 GHz	1.6 GHz	1.0 GHz
C L X	10G023-2C 10G023-2L	10G023-3C 10G023-3L 10G023-3X	10G023K-2C 10G023K-2L 10G023K-2X

GigaBit Logic

10G023
10G023K

10G023 OPERATION

Truth Table

Function	SELn	$\overline{CLR}$	OE	CLKn	COMCLK	DnA	DnB	Output Qn (t+1)
Clear*	X	L	H	X	X	X	X	L
Output Disabled	X	H	L	L or H	L or H	X	X	L
Output Enabled	X	H	H	L or H	L or H	X	X	Qn(t)
Select A	H	H	H	⎍	H	DnA(t)	X	DnA(t)
Select B	L	H	H	⎍	H	X	DnB(t)	DnB(t)
Select A	H	H	H	H	⎍	DnA(t)	X	DnA(t)
Select B	L	H	H	H	⎍	X	DnB(t)	DnB(t)
Clock Disabled	X	H	H	L	⎍	X	X	Qn(t)
Clock Disabled	X	H	H	⎍	L	X	X	Qn(t)

* The $\overline{CLR}$ control gates the clock inputs. Therefore, when both CLKn and COMCLK are high, resetting $\overline{CLR}$ by returning it to its high state will cause data at the input pins to be clocked into the flip flops at the rising edge of $\overline{CLR}$.

The operation of the 10G023 is described in the truth table above. All flip flop stages are reset to low by bringing $\overline{CLR}$ low at any time. All outputs can be forced low for bus connection, without altering the current state of the flip flops, by bringing OUTEN low. The clock should not transition high when OUTEN is brought low so that the output state of each flip flop is maintained. When SEL is high, A Data are selected assuming both SEL and Data setup and hold time requirements are met. Setting SEL low selects the B Data inputs. At any time, the clock input can be disabled by setting the unused clock input(s) low. The current output state of each flip flop is maintained in this case.

10G024 Compatibility

To make the 10G023 compatible with the 10G024, tie the "B" input and the SELx low.

PIN DESCRIPTIONS

D0A - D3A	A data inputs
D0B - D3B	B data inputs
SEL0 -SEL3	2:1 MUX select inputs
CLK0 - CLK3	Individual flip flop clock inputs
$\overline{COM}$CLK	Common clock input to all four flip flops
$\overline{CLR}$	Active low asynchronous clear control
OUTEN	Active high output enable control
Q0 - Q3	True data outputs
$\overline{Q0}$ - $\overline{Q3}$	Complement data outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VTTC	AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.
VDCH	Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G023's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G023 from ECL. Connect to the VBBS pin when the 10G023 is driven from PicoLogic™. This pin may not be left unconnected.
VBBS	PicoLogic™ threshold reference output voltage. Connect to VBB when driving from PicoLogic™.

GigaBit Logic

10G023
10G023K

DC CHARACTERISTICS

Tc = -40°C to 100°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I in 1	Input Current; Data, Sel, CLKn		200	500	µA	VIN = -1.0 V to -1.6 V
I in 2	Input Current; COMCLK, CLR, OUTEN		500	1000	µA	
ISS	Power Supply Current (10G023)		260	340	mA	
ISS	Power Supply Current (10G023K)		260	375	mA	
IEE	Power Supply Current (10G023)		35	65	mA	
IEE	Power Supply Current (10G023K)		35	70	mA	
VIH	Input High Voltage (10G023K)	-0.8			V	
VIL	Input Low Voltage (10G023K)			-1.8	V	
PD	Power Dissipation (10G023)		1.0	1.5	W	
PD	Power Dissipation (10G023K)		1.0	1.7	W	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Notes 1, 2)

VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

		10G023-2							10G023-3							
		Tc= 0° C		Tc= 25° C			Tc= 85° C		Tc= 0° C		Tc= 25° C			Tc= 85° C		
SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNITS
1/Tc1	Individual clock freq.	1.9		1.9	2.1		1.9		1.6		1.6	1.8		1.6		GHz
1/Tc2	Common clock freq.	1.6		1.6	1.8		1.6		1.3		1.3	1.5		1.3		GHz
Tsd	Data setup time	-50		-50			-50		-40		-40			-40		ps
Tss	SEL setup time	-50		-50			-50		-40		-40			-40		ps
Thd	Data hold time	250		250			250		275		275			275		ps
Ths	SEL hold time	150		150			150		165		165			165		ps
Tdod	Output disable delay	375	650	350	500	550	350	650	400	700	350	550	600	400	700	ps
Tdoe	Output enable delay	350	600	350	450	500	350	600	350	650	350	500	550	350	650	ps
Twc	Clear pulse width	500					500		550					550		ps
Tdc	Output clear delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdhl	Clock to output H-L delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdlh	Clock to output L-H delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
	Clock to output skew		50		30	50		50		50		30	50		50	ps
Tr	Output rise time		175		175			200		200		175			225	ps
Tf	Output fall time		150		125			150		175		125			175	ps

NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

GigaBit Logic

10G023
10G023K

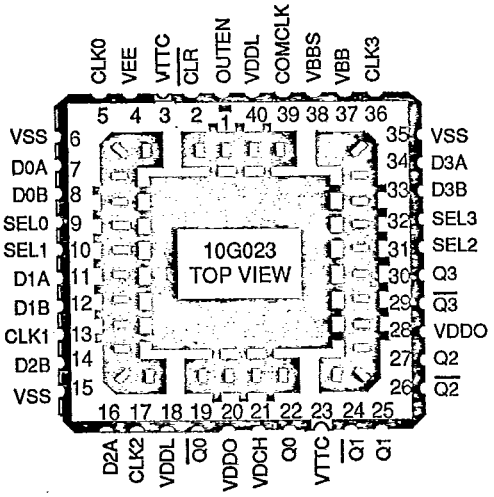
AC CHARACTERISTICS (Notes 1, 2)

VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

SYMBOL	PARAMETER	10G023K-2							UNITS
		Tc= -40° C		Tc= 25° C			Tc= 100° C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/Tc1	Individual clock freq.	1.0		1.9	2.1		1.0		GHz
1/Tc2	Common clock freq.	0.8		1.6	1.8		0.8		GHz
Tsd	Data setup time	-40		-50			-40		ps
Tss	SEL setup time	-40		-50			-40		ps
Thd	Data hold time	275		250			275		ps
Ths	SEL hold time	165		150			165		ps
Tdod	Output disable delay	400	700	350	500	550	400	700	ps
Tdoe	Output enable delay	350	650	350	450	500	350	650	ps
Twc	Clear pulse width	550					550		ps
Tdc	Output clear delay	600	1050	600	850	900	600	1050	ps
Tdhl	Clock to output H-L delay	600	1050	600	850	900	600	1050	ps
Tdlh	Clock to output L-H delay	600	1050	600	850	900	600	1050	ps
	Clock to output skew		50		30	50		50	ps
Tr	Output rise time		200		175			225	ps
Tf	Output fall time		175		125			175	ps

NOTES:
1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



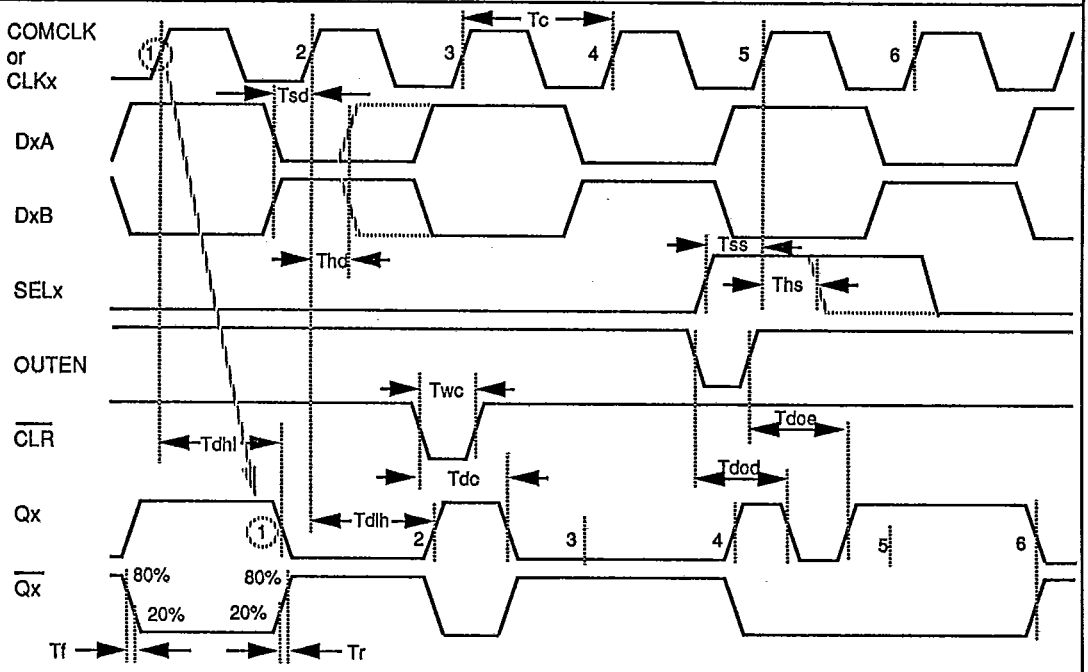
NOTE: Pin 1 is marked for orientation.

T-46-07-09

GigaBit Logic

10G023
10G023K

SWITCHING WAVEFORMS



NOTES

T-90-20

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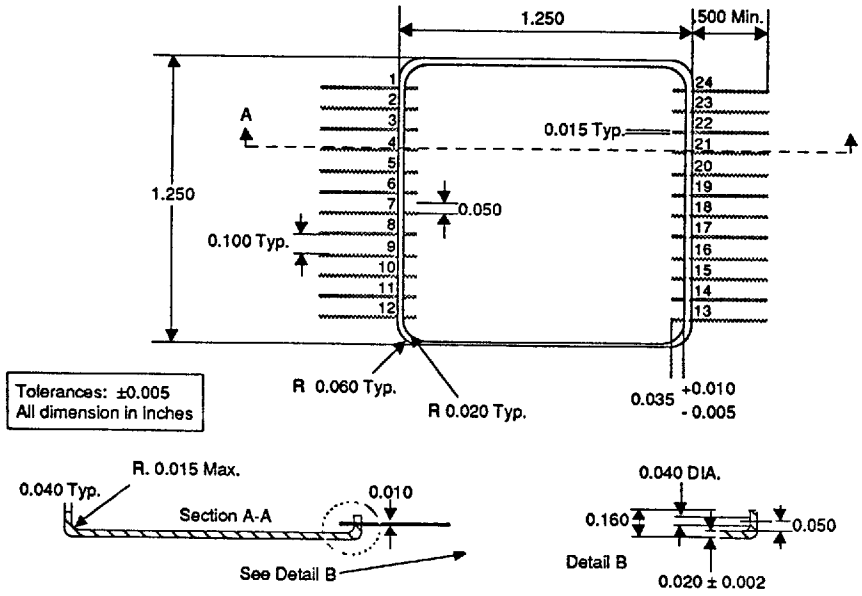
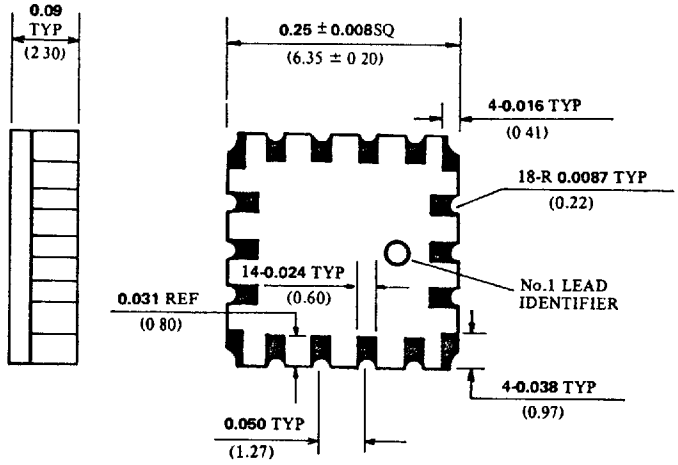
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

11

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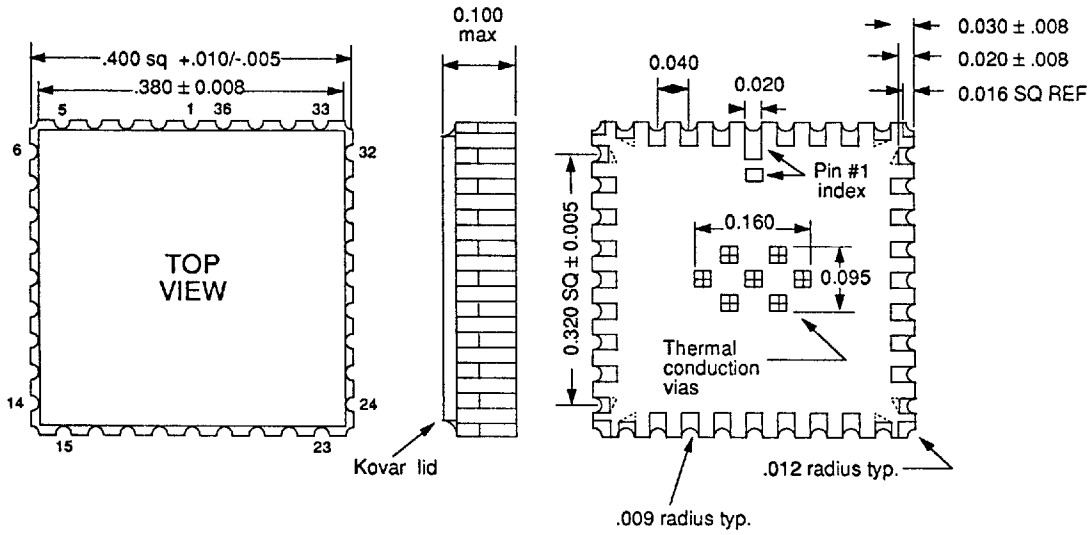
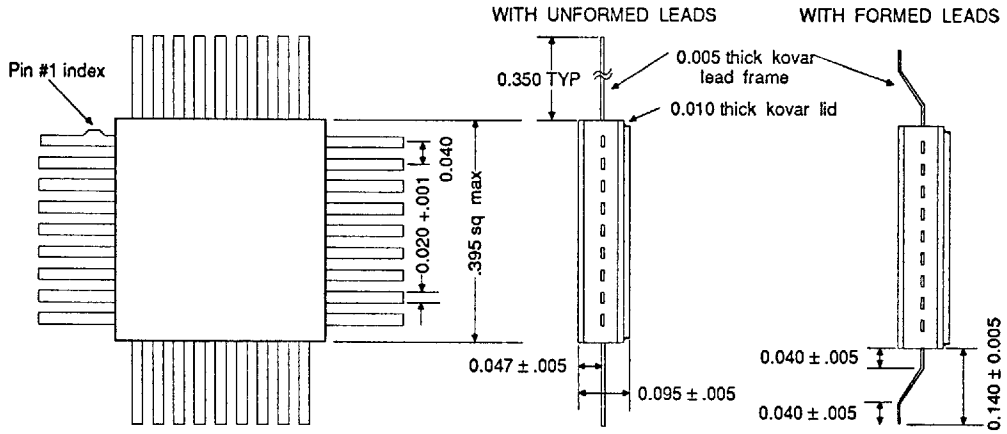
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



T-90-20

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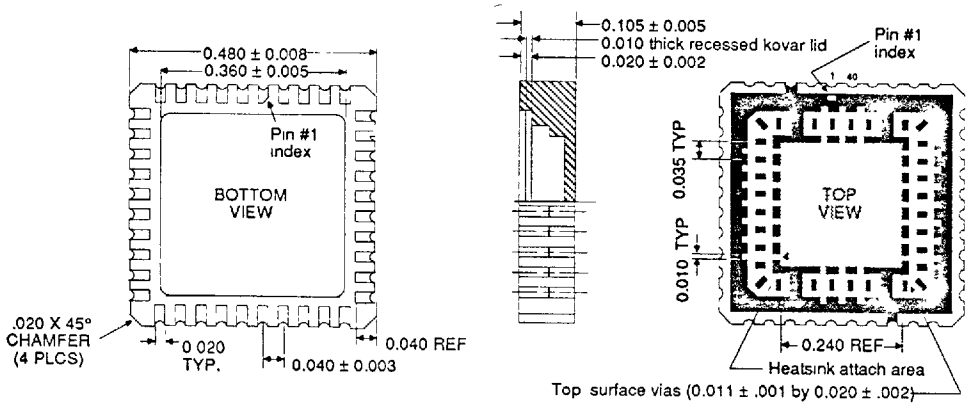
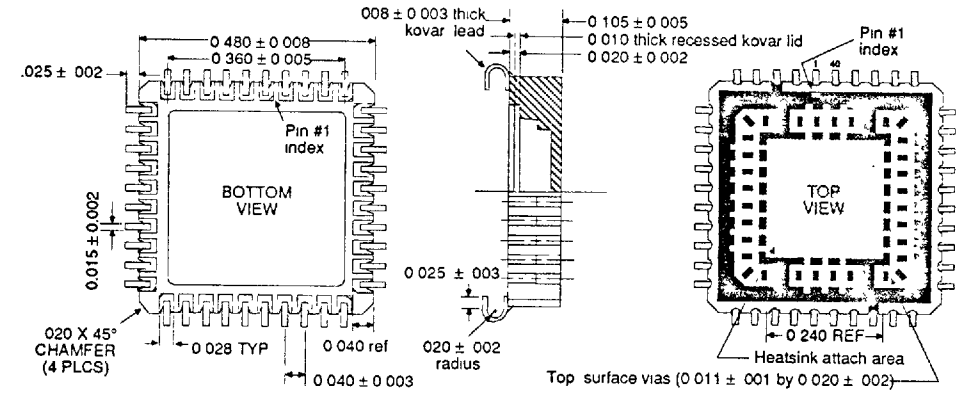
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

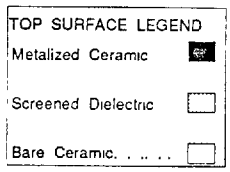


40 PIN LEADED CHIP CARRIER
TYPE C

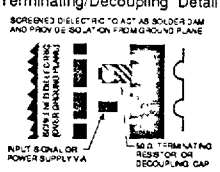


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



T-90-20

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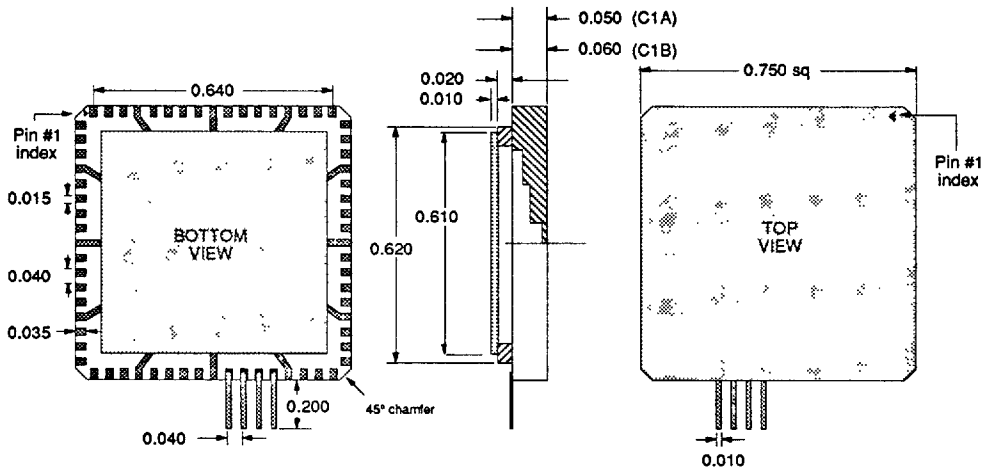
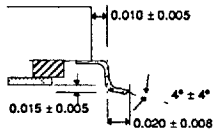
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3