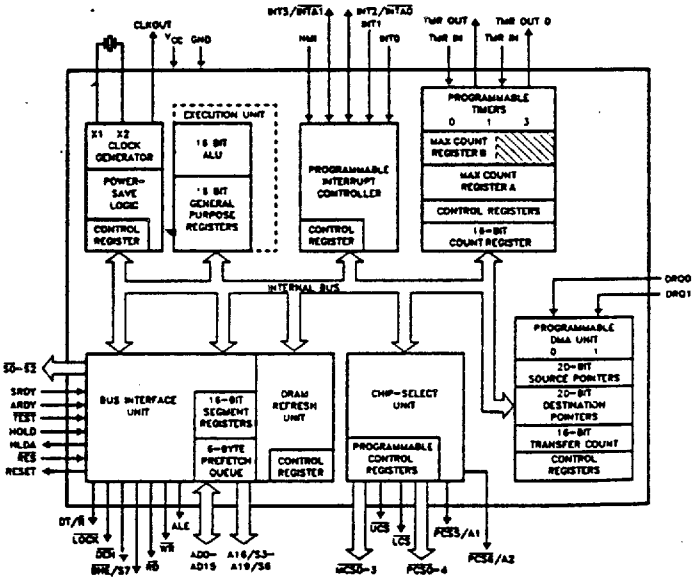
Radiation Hardened 80C186RP CHMOS Field 16 - bit Microprocessor

For Space Applications



SEI's 80C186RP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 80C186RP is fully equivalent to the commercial Intel's M80C186 16-bit CMOS microprocessor. It features a DRAM refresh control unit, power-save mode, and a direct numerics interface. This device is a very high integration 16-bit microprocessor which combines 15-20 of the most common microprocessor system components onto one chip. The 80C186RP contains a DMA controller which provides two independent high speed DMA channels. Data transfers can occur between memory and I/O spaces or within the same space. Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20 bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles, which is a minimum of 8 clocks, one cycle to fetch data and the other to store data. Capable of surviving space environments, the 80C186RP is ideal for satellite, spacecraft, and space probe mission. The RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 80C186RP is available in Class S packaging and screening.

SPACE ELECTRONICS INCORPORATED
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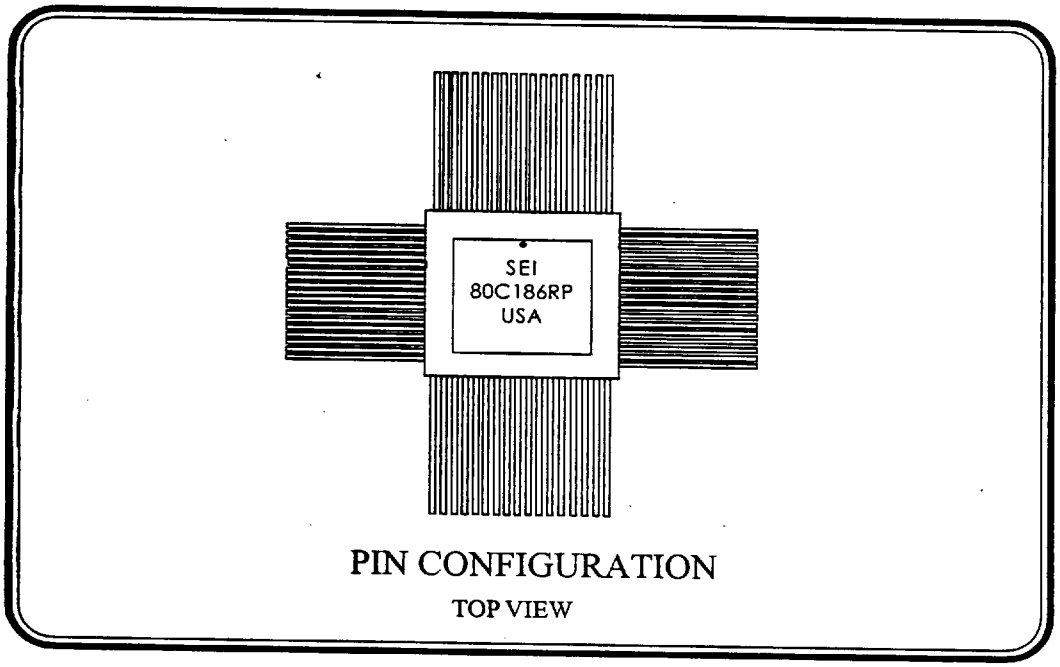
Radiation Hardened
80C186RP

High Speed CMOS
16 - bit Microprocessor



PIN CONFIGURATION
TOP VIEW

Features

- 16-bit CMOS Microprocessor
- Pin Compatible with Intel M80C186
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
  - 68 Pin RAD-PAK® quad flat pack (0.9 in. x 0.9 in.)
  - Weight – 12 grams
- Available in standard 12.5 MHz or 16MHz
- JEDEC Approved Byte Wide Pinout
- Available Temperature Range: -55°C to +125°C
- Enhanced Mode CHMOS Technology
  - Dynamic RAM Refresh Control Unit
  - Power-Save Mode
  - Asynchronous Numeric Coprocessor Interface
  - Clock Generator
  - Programmable Wait State Generator
  - Programmable Interrupt Controller
  - Local Bus Controller
  - 2 Independent DMA Channels
  - 3 Programmable 16-bit Timers

TQM
Total Quality Management

March 1995

For Further Information Contact:
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80C186RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	-0.5	6.5	V
Voltage, Any Pin		-1.0	+7.0	V
Power Dissipation			1.0	W
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	-55	+125	°C

80C186RP DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Low Voltage (Except X1)	V_{IL}	-0.5	0.2 V_{CC}-0.3	V	
Input High Voltage (All except X1,RES\, ARDY, and SRDY)	V_{IH}	0.2V_{CC}+0.9	V_{CC}+0.5	V	
Input High Voltage (RES\)	V_{IH1}	3.0	V_{CC}+0.5	V	
Input High Voltage (SRDY, ARDY)	V_{IH2}	0.2V_{CC}+1.1	V_{CC}+0.5	V	
Clock Input Low Voltage (X1)	V_{IL1}	-0.5	0.6	V	
Clock Input High Voltage (X1)	V_{IH3}	3.9	V_{CC}+0.5	V	
Output Low Voltage I_{OL}=2.5 mA (S0,1,2). I_{OL}=2.0 mA (others)	V_{OL}		0.45	V	
Output High Voltage I_{OH}=-2.4 mA @ 2.4 V I_{OH}=-200 uA @ V_{CC}-0.5	V_{OH}	2.4 V_{CC}-0.5	V_{CC} V_{CC}	V V	

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80C186RP DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Current @ 16 MHz, 0°C V_{CC}= 5.25 V @ 12.5 MHz, 0°C V_{CC}= 5.5 V @ 10 MHz, 0°C V_{CC}= 5.5 V	I_{CC}		 150 120 100	 mA mA mA	 (-16) (-12) (-10)
Input Leakage Current @ 0.5 MHz, 0.45 V $\leq V_{IN} \leq V_{CC}$	I_{LI}		±10	uA	
Output Leakage Current @ 0.5 MHz, 0.45 V $\leq V_{OUT} \leq V_{CC}$	I_{LO}		±10	uA	
Clock Output Low I_{CLO}= 4.0 mA	V_{CLO}		0.45	V	
Clock Output High I_{CHO}= -500 uA	V_{CHO}	V_{CC} - 0.5		V	
Input Capacitance	C_{IN}		10	pF	f=1MHz
Output Capacitance	C_{IO}		20	pF	f=1MHz

Notes:
1. V_{CC} = 5V ±10% except V_{CC} = 5V ±5% at f> 12.5 MHz; T_A = -55 to +125 °C
2. Guaranteed by design.

80C186RP AC ELECTRICAL CHARACTERISTICS [1,2,4,5]

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Data in Setup (A/D)[3]	T_{DVCL}	15		ns	
Data in Hold (A/D)[3]	T_{CLDX}	3		ns	
Status Active Delay	T_{CHSV}	5	35	ns	
Status Inactive Delay	T_{CLSH}	5	35	ns	
Address Valid Delay	T_{CLAV}	5	36	ns	
Address Hold[3]	T_{CLAX}	0		ns	
Data Valid Delay	T_{CLDV}	5	36	ns	
Status Hold Time	T_{CHDX}	10		ns	
ALE Active Delay	T_{CHLH}		25	ns	

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80C186RP AC ELECTRICAL CHARACTERISTICS [1,2,4,5]

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
ALE Width[3]	T_{LHLL}	$T_{CLCL-15}$		ns	
ALE Inactive Delay	T_{CHLL}		25	ns	
Address Valid to ALE Low	T_{AVLL}	$T_{CHCL-15}$		ns	Equal Loading
Address Hold from ALE Inactive	T_{LLAX}	$T_{CHCL-15}$		ns	Equal Loading
Address Valid to Clock High[3]	T_{AVCH}	0		ns	
Address Float Delay	T_{CLAZ}	T_{CLAX}	25	ns	
Chip-Select Active Delay	T_{CLCSV}	3	33	ns	
Chip-Select Hold from Command Inactive	T_{CXCSX}	$T_{CLCX-10}$		ns	Equal Loading
Chip-Select Inactive Delay	T_{CHCSX}	5	30	ns	
DEN Inactive to DT/R\ Low[3]	T_{DXDL}	0		ns	
Control Active Delay 1	T_{CVCTV}	3	37	ns	
DEN\ Inctive Delay	T_{CVDEX}	5	37	ns	
Control Active Delay 2	T_{CHCTV}	5	37	ns	
LOCK\ Valid/Invalid Delay	T_{CLLV}	3	37	ns	
Address Float to RD Active[6]	T_{AZRL}	0		ns	
RD Active Delay	T_{CLRL}	5	37	ns	
RD Pulse Width[3]	T_{RLRH}	$2T_{CLCL-25}$		ns	
RD Inactive Delay	T_{CLRH}	5	37	ns	
RD Inactive to ALE High	T_{RHLH}	$T_{CLCH-14}$		ns	Equal Loading
RD Inactive to Address Active	T_{RHAV}	$T_{CLCH-15}$		ns	Equal Loading

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Notes:

1. V_{CC}= 5V ± 10% except V_{CC}= 5V ± 5% at f>12.5 MHz
   T_A= -55 to +125 °C
2. All timings are measured at 1.5V and 100pF loading on CLKOUT unless otherwise noted.
3. Tested by application of signal.
4. For A.C. tests, input V_{IL}=0.45V and V_{IH}=2.4V except at X1 where $V_{IH}=V_{CC}-0.5V$.
5. All output test conditions are with C_L=50-200 pF (10 MHz) and C_L=50-100 pF (12.5-16 MHz).
6. Guaranteed by design.

80C186RP MICROPROCESSOR PINOUT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AD15	18	DRQ0	35	MCS3\ /INPS\	52	SO\
2	AD7	19	DRQ1	36	MCS2\	53	S1\
3	AD14	20	TMR IN 0	37	MCS1\ /ERROR\	54	S2\
4	AD6	21	TMR IN 1	38	MCSO\ /PEREQ	55	ARDY
5	AD13	22	TMR OUT 0	39	DEN\	56	CLKOUT
6	AD5	23	TMR OUT 1	40	DT/R\	57	RESET
7	AD12	24	RES\	41	INT3/INTA1\	58	X2
8	AD4	25	PCSO\	42	INT2/INTA0\	59	X1
9	Vcc	26	Vss	43	Vcc	60	Vss
10	AD11	27	PCS1\	44	INT1	61	ALE/QS0
11	AD3	28	PCS2\	45	INT0	62	RD\ /QSMD\
12	AD10	29	PCS3\	46	NMI	63	WR\ /QS1
13	AD2	30	PCS4\	47	TEST\ /BUSY	64	BHE\
14	AD9	31	PCS5\ /A1	48	LOCK\	65	A18.S6
15	AD1	32	PCS6\ /A2	49	SRDY	66	A18/S5
16	AD8	33	LCS\	50	HOLD	67	A17/S4
17	AD0	34	UCS\	51	HLDA	68	A16/S3

80C186RP Package Ordering Guide

Package Style	Case Outline 1/	Description
Q	Q-68	68 Pin Quad Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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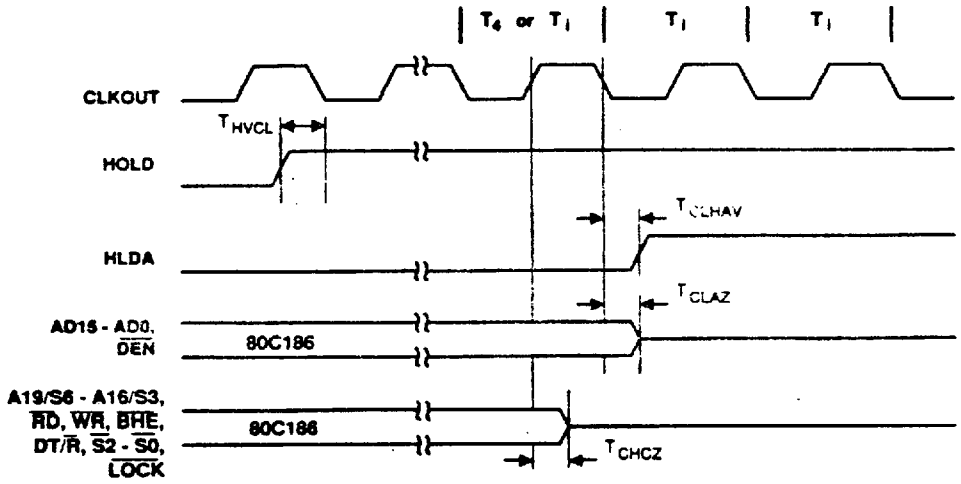
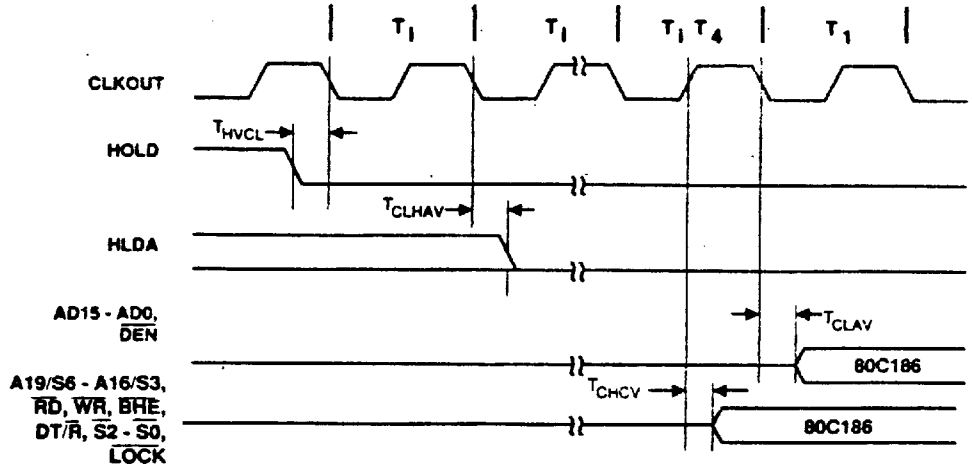
HOLD/HLDA WAVEFORMS (Entering Hold)



HOLD/HLDA WAVEFORMS (Leaving Hold)



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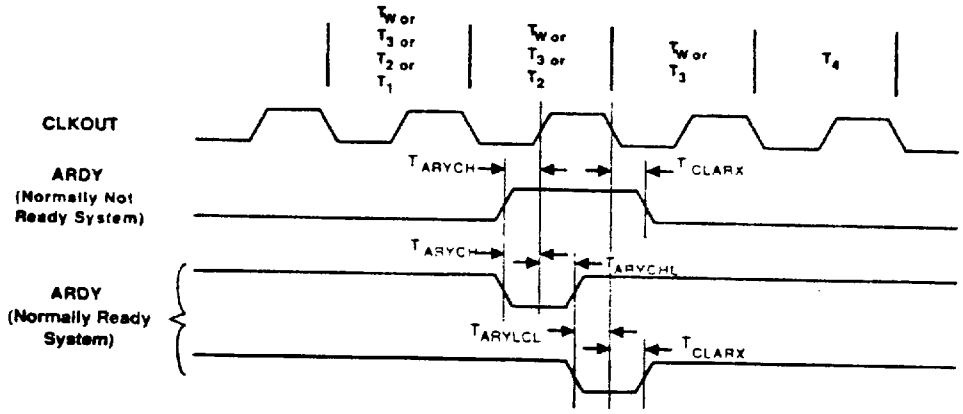
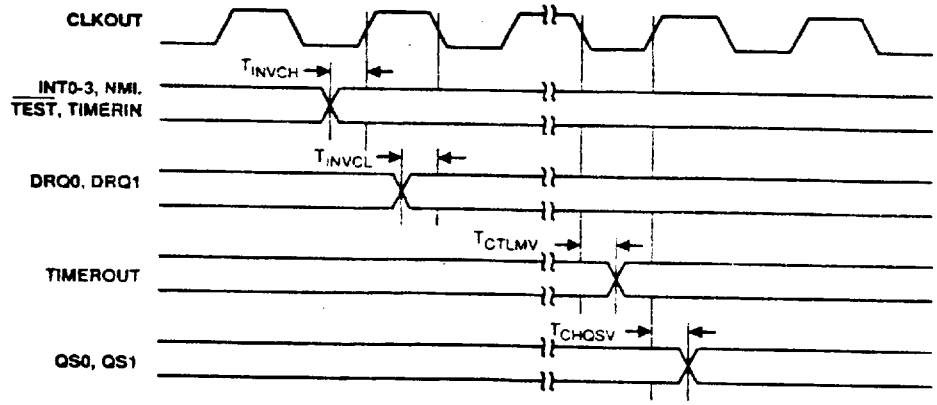
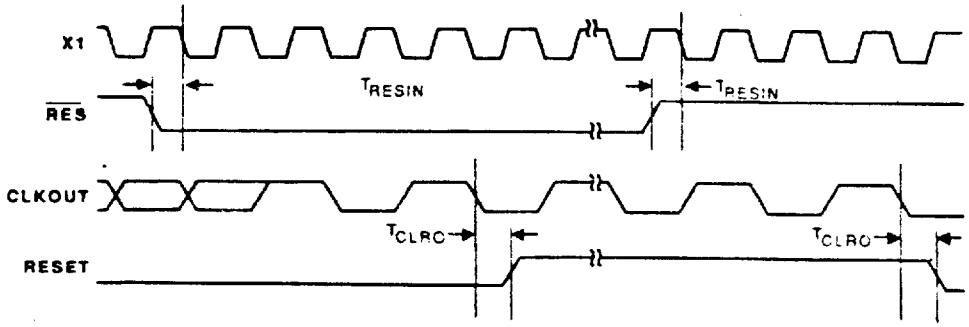
ASYNCHRONOUS READY (ARDY) WAVEFORMS



PERIPHERAL AND QUEUE STATUS WAVEFORMS



RESET WAVEFORMS



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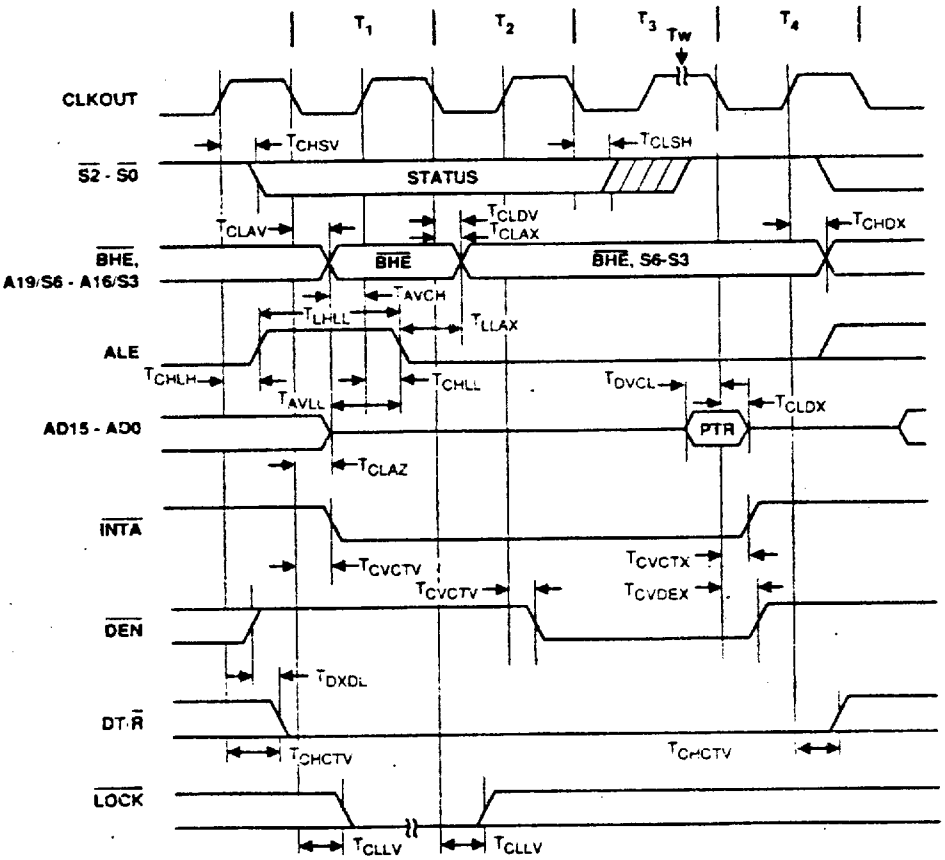
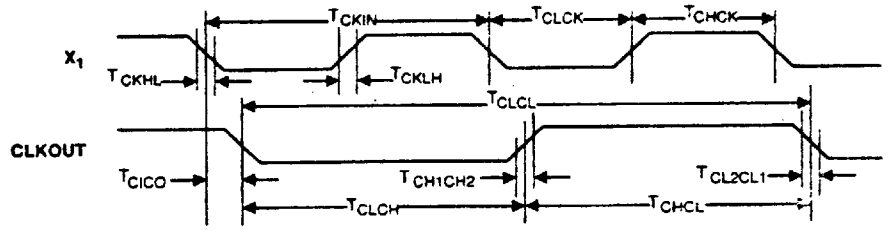
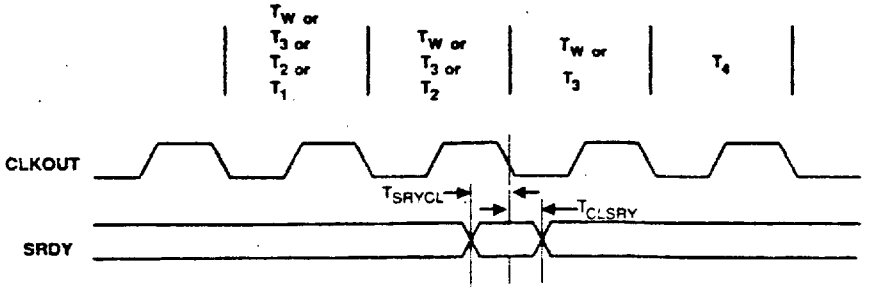
INTERRUPT ACKNOWLEDGE CYCLE WAVEFORMS



CLOCK WAVEFORMS



SYNCHRONOUS READY (SRDY) WAVEFORMS



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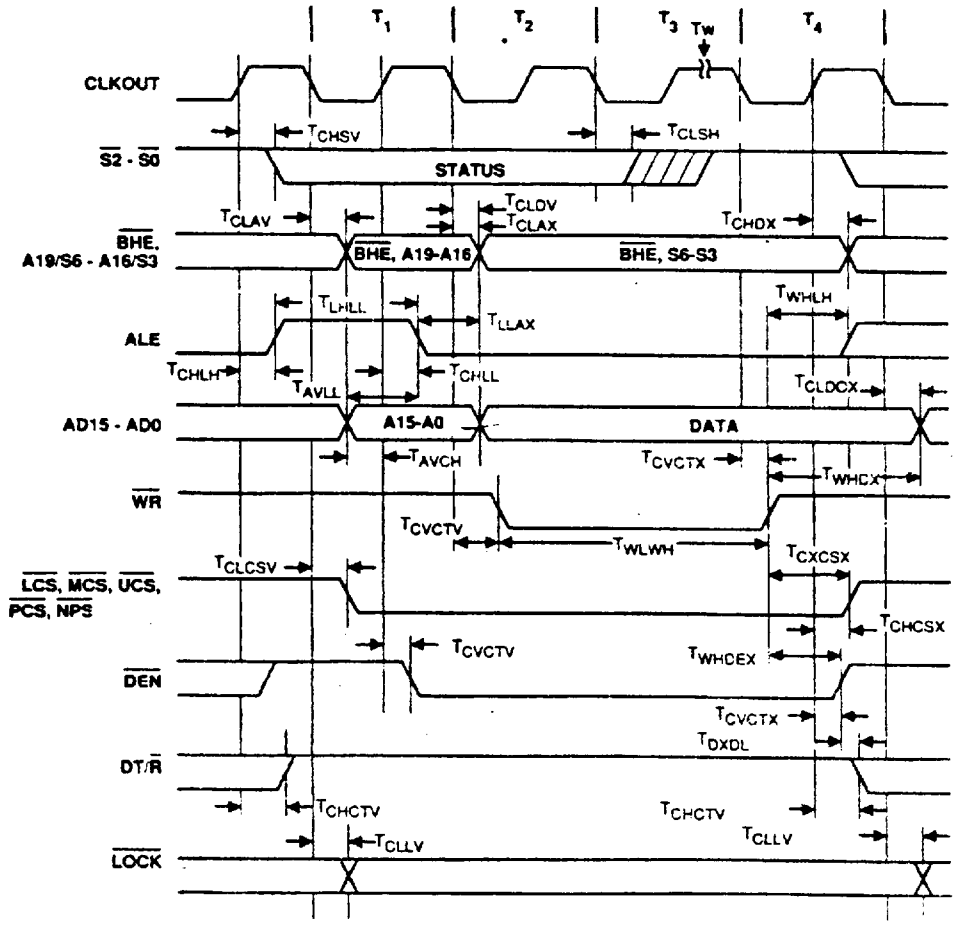
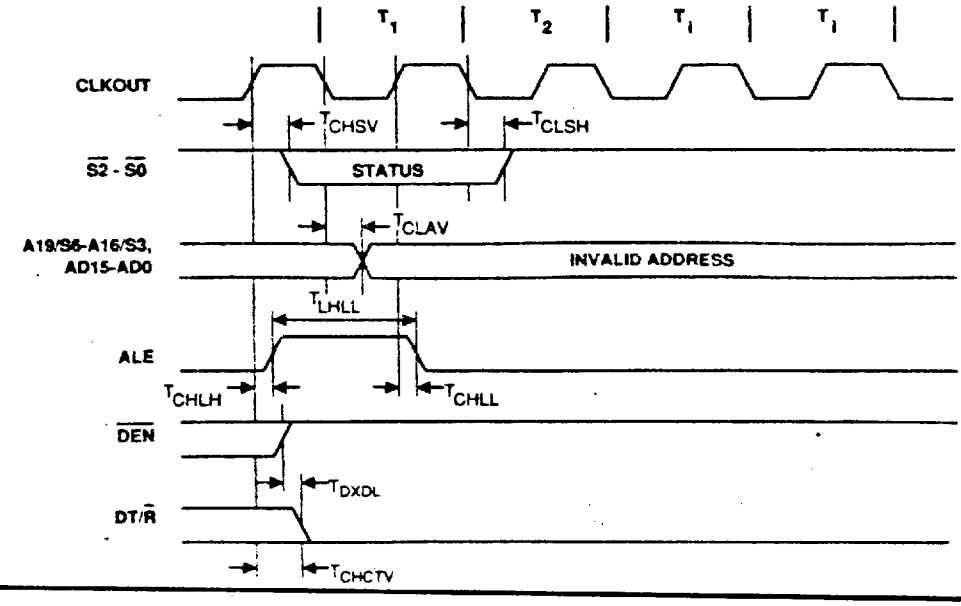
WRITE CYCLE WAVEFORMS



SOFTWARE HALT CYCLE WAVEFORMS



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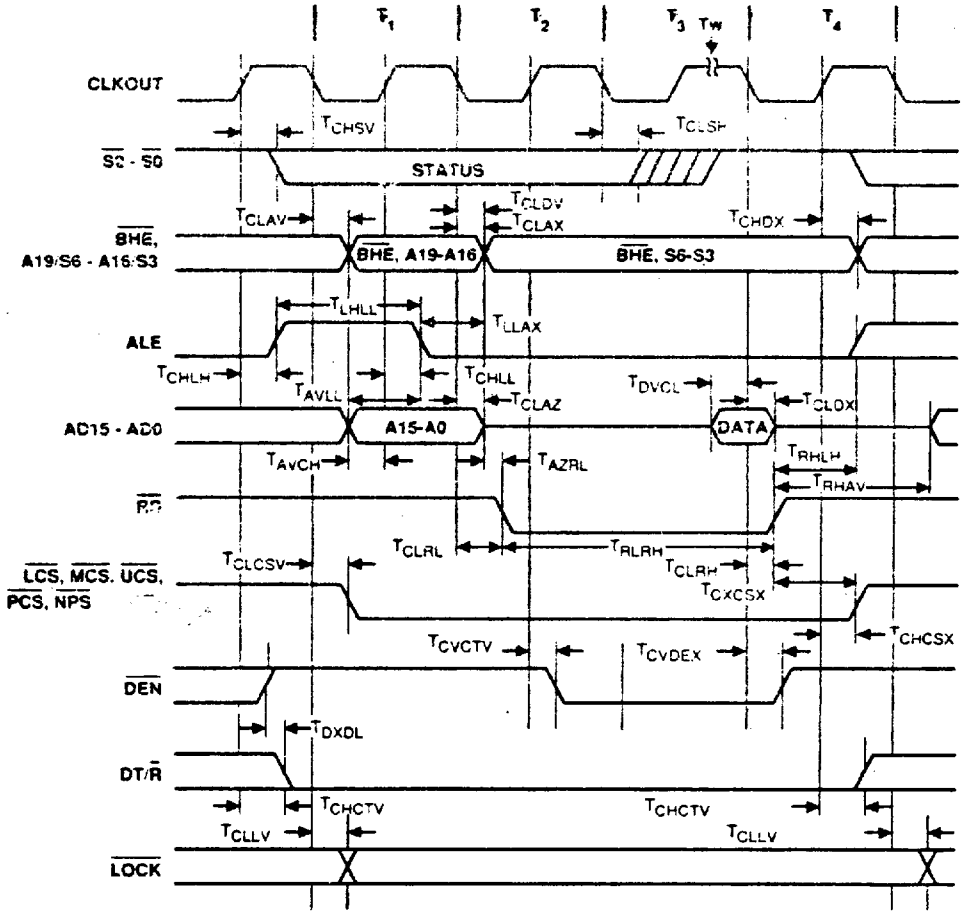
READ CYCLE WAVEFORMS



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