SONY

CXD1197AQ

CD-ROM decoder with ADPCM decoder

Description

The CXD1197AQ is a CD-ROM decoder LSI which features a built-in ADPCM decoder.

Features

- Supports CD-ROM, CD-I, and CD-ROM XA formats.
- Real-time error correction.
- Double-speed playback.
- All audio output sampling frequencies operate at 132.3 KHz.
  (Built-in oversampling filter.)
- Built-in de-emphasis digital filter.
- 68000 system host interface.

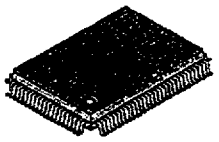
Application

CD-ROM drive

Structure

Silicon gate CMOS IC

100 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25°C)

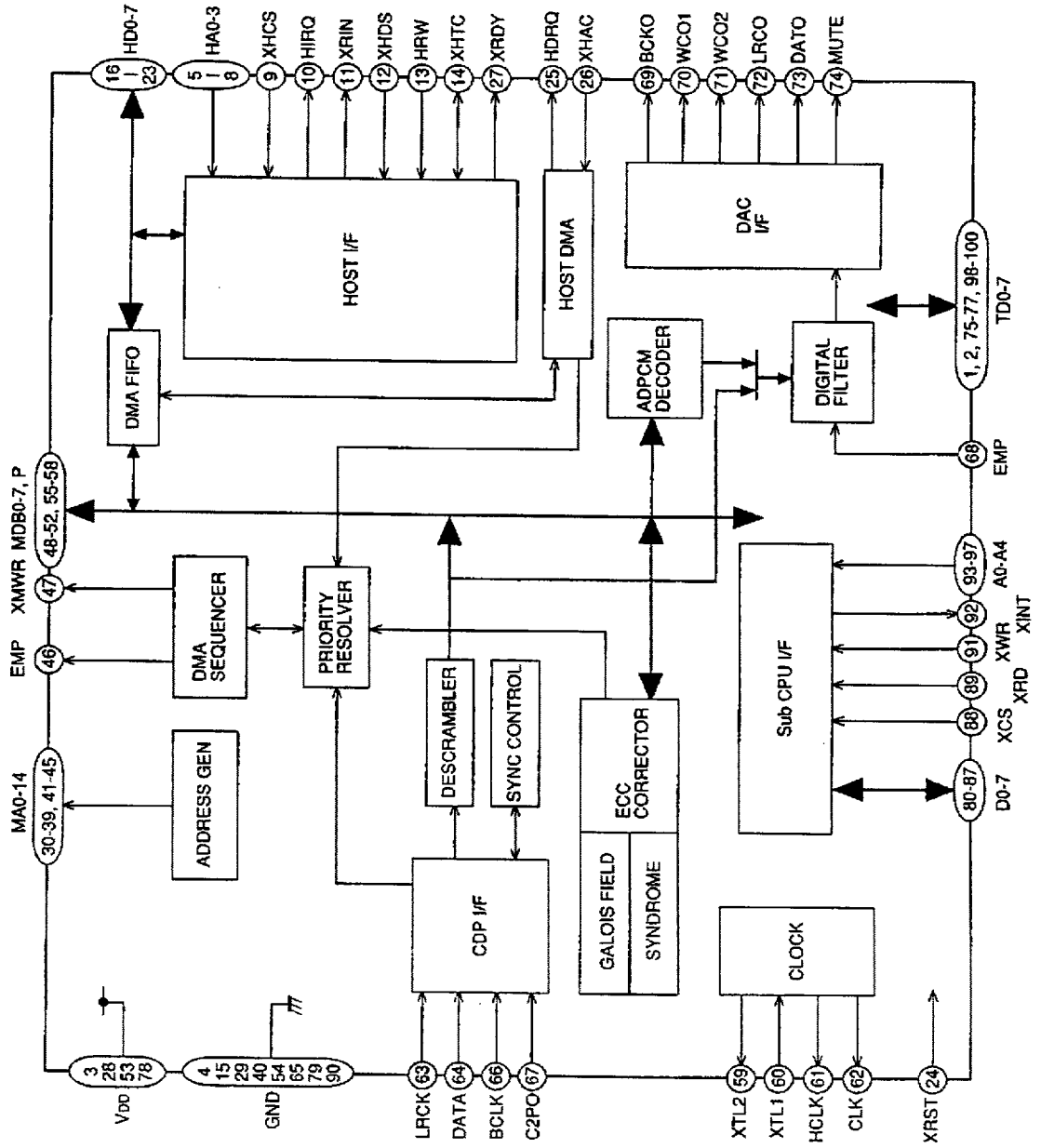
• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_I	−0.5 to V_{DD}+0.5	V
• Output voltage	V_I	−0.5 to V_{DD}+0.5	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	+4.5 to +5.5 (+5.0 Typ.)	V
• Operating temperature	T_{opr}	−20 to +75	°C

E92504A2X-TE

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	TD1	I/O	Test input/output
2	TD0	I/O	Test input/output
3	VDD	—	Power supply (+5V)
4	GND	—	GND
5	HA0	I	Host address
6	HA1	I	Host address
7	HA2	I	Host address
8	HA3	I	Host address
9	XHCS	I	CXD1197AQ select from host (negative logic)
10	HIRQ	O	Interrupt request to host (negative logic). Open drain output.
11	XRIN	O	Remote control interrupt request to host (negative logic). Open drain output.
12	XHDS	I	Data strobe from host (negative logic).
13	HRW	I	Read/write from host.
14	XHTC	I/O	Data acknowledge with host (negative logic). Open drain output.
15	GND	—	GND
16	HD0	I/O	Host data bus
17	HD1	I/O	Host data bus
18	HD2	I/O	Host data bus
19	HD3	I/O	Host data bus
20	HD4	I/O	Host data bus
21	HD5	I/O	Host data bus
22	HD6	I/O	Host data bus
23	HD7	I/O	Host data bus
24	XRST	I	Reset (negative logic).
25	HDRQ	O	DMA request to host (negative logic). Open drain output.
26	XHAC	I	DMA acknowledge from host (negative logic).
27	XRDY	O	Data ready to host (negative logic). Open drain output.
28	VDD	—	Power supply (+5V)
29	GND	—	GND
30	MA0	O	Buffer address (LSB)
31	MA1	O	Buffer address
32	MA2	O	Buffer address
33	MA3	O	Buffer address
34	MA4	O	Buffer address
35	MA5	O	Buffer address

Pin No.	Symbol	I/O	Description
36	MA6	O	Buffer address
37	MA7	O	Buffer address
38	MA8	O	Buffer address
39	MA9	O	Buffer address
40	GND	—	GND
41	MA10	O	Buffer address
42	MA11	O	Buffer address
43	MA12	O	Buffer address
44	MA13	O	Buffer address
45	MA14	O	Buffer address
46	XMOE	O	Buffer output enable (negative logic).
47	XMWR	O	Buffer write enable (negative logic).
48	MDB0	I/O	Buffer data bus
49	MDB1	I/O	Buffer data bus
50	MDB2	I/O	Buffer data bus
51	MDB3	I/O	Buffer data bus
52	MDB4	I/O	Buffer data bus
53	VDD	—	Power supply (+5V)
54	GND	—	GND
55	MDB5	I/O	Buffer data bus
56	MDB6	I/O	Buffer data bus
57	MDB7	I/O	Buffer data bus
58	MDBP	I/O	Buffer data bus (for error flag).
59	XTL2	O	Crystal oscillator output
60	XTL1	I	Crystal oscillator input (16.9344 MHz)
61	HCLK	O	8.4672 MHz clock output
62	CLK	O	16.9344 MHz clock output
63	LRCK	I	Left/right clock from CD DSP (Selects L/R channel).
64	DATA	I	Data input from CD DSP
65	GND	—	GND
66	BCLK	I	Data strobe clock (bit clock).
67	C2PO	I	Error flag from CD DSP - C2 pointer (positive logic).
68	EMP	I	Emphasis ON from CD DSP (positive logic).
69	BCKO	O	Bit clock to D/A converter (DAC).
70	WCO1	O	Word clock line 1 to DAC.

Pin No.	Symbol	I/O	Description
71	WCO2	O	Word clock line 2 to DAC.
72	LRCO	O	Left/right clock to DAC
73	DATO	O	Data output to DAC
74	MUTE	O	Mute (positive logic)
75	TD7	O	Test input/output
76	TD6	O	Test input/output
77	TD5	O	Test input/output
78	VDD	—	Power supply (+5V)
79	GND	—	GND
80	D0	O	Sub CPU data bus
81	D1	O	Sub CPU data bus
82	D2	O	Sub CPU data bus
83	D3	O	Sub CPU data bus
84	D4	O	Sub CPU data bus
85	D5	O	Sub CPU data bus
86	D6	O	Sub CPU data bus
87	D7	O	Sub CPU data bus
88	XCS	I	CXD1197AQ select from sub CPU (negative logic).
89	XRD	I	CXD1197AQ internal register read strobe from sub CPU (negative logic).
90	GND	—	GND
91	XWR	I	CXD1197AQ internal register write strobe from sub CPU (negative logic).
92	XINT	O	Interrupt request to sub CPU (negative logic).
93	A0	I	Sub CPU address
94	A1	I	Sub CPU address
95	A2	I	Sub CPU address
96	A3	I	Sub CPU address
97	A4	I	Sub CPU address
98	TD4	O	Test input/output
99	TD3	O	Test input/output
100	TD2	O	Test input/output

Electrical Characteristics

DC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Topr=−20 to 75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
TTL input pin levels (*1) "High"-level input voltage	V_{IH1}		2.2			V
TTL input pin levels (*1) "Low"-level input voltage	V_{IL1}				0.8	V
CMOS input pin levels (*2) "High"-level input voltage	V_{IH2}		0.7V_{DD}			V
CMOS input pin levels (*2) "Low"-level input voltage	V_{IL2}				0.3V_{DD}	V
CMOS Schmitt input pin levels (*3) "High"-level input voltage	V_{IH4}		0.8V_{DD}			V
CMOS Schmitt input pin levels (*3) "Low"-level input voltage	V_{IL4}				0.2V_{DD}	V
CMOS Schmitt input pin levels (*3) Hysteresis of input voltage	$V_{IH4}-V_{IL4}$			0.6		V
Bi-directional pins with pull-up resistor (*4) Input current	I_{IL3}	V_{IN}=0V	−90	−200	−440	μA
Output voltage "High"-level (*5)	V_{OH1}	I_{OH}=−2mA	V_{DD}−0.8			V
Output voltage "Low"-level (*6)	V_{OL1}	I_{OL}=4mA			0.4	V
Input leakage current (*7)	I_{I1}	V_{IN}=V_{SS} or V_{DD}	−10		10	μA
Input leakage current (*8)	I_{I2}	V_{IN}=V_{SS} or V_{DD}	−40		40	μA
Output leakage current (*9)	I_{OZ}	HiZ	−40		40	μA
Oscillator cell (*10) "High"-level input voltage	V_{IH4}		0.7V_{DD}			V
Oscillator cell "Low"-level input voltage	V_{IL4}				0.3V_{DD}	V
Oscillator cell logic threshold value	LV_{TH}			0.5V_{DD}		V
Oscillator cell feedback resistor value	R_{FB}	V_{IN}=V_{SS} or V_{DD}	250k	1M	2.5M	Ω
Oscillator cell "High"-level output voltage	V_{OH2}	I_{OH}=−3mA	0.5V_{DD}			V
Oscillator cell "Low"-level output voltage	V_{OL2}	I_{OL}=3mA			0.5V_{DD}	V

*1. D0 to D7, A0 to A4, XWR, XRD, XCS, MDB0 to MDB7, MDBP, TD0 to TD7
*2. DATA, LRCK, C2PO, EMP, HRW, HD0 to HD7, XHDS, HA00 to HA03, XHTC
*3. BCLK, XRST
*4. D0 to D7, MDB0 to MDB7, TD0 to TD7
*5. XMWR, XMOE, MA0 to MA14, D0 to D7, HD0 to HD7, MDB0 to MDB7, MDBP, TD0 to TD7, BCKO, WCO1, WCO2, LRCO, DATO, MUTE, CLK, HCLK
*6. All outputs except XTL2
*7. All inputs except XTL1 and those listed in *4 & *9
*8. HD0 to HD7, XHTC
*9. HDRQ, HIRQ, XRDY, XRIN
*10. Input: XTL1, Output: XTL2

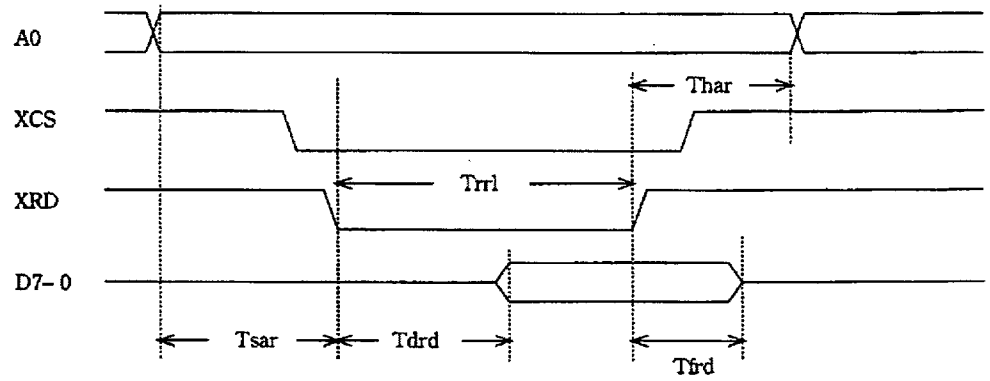
I/O Capacitances (V_{DD}=V_I=0V, f=1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pins	C_{IN}			9	pF
Output pins	C_{OUT}			11	pF
I/O pins	C_{OUT}			11	pF

AC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Topr=−20 to 75, Output Load=50pF)

1. sub CPU Interface

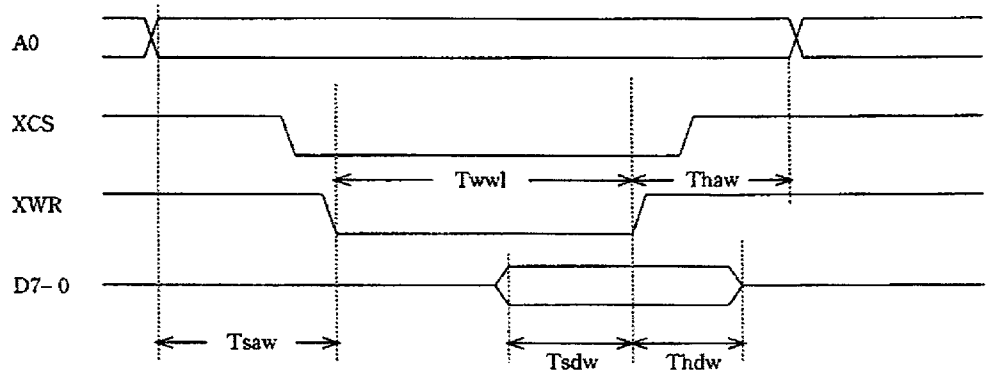
(1) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Address set-up time (In reference to XCS&XRD ↓)	Tsar	30			ns
Address hold time (In reference to XCS&XRD ↑)	Thar	20			ns
Data propagation delay (In reference to XCS&XRD ↓)	Tdrd			100	ns
Data float time (In reference to XCS&XRD ↑)	Tfrd	0		20	ns
Pulse width of XRD "Low"-level	Trrl	120			ns

* '&' in the table stands for logical AND.

(2) Write

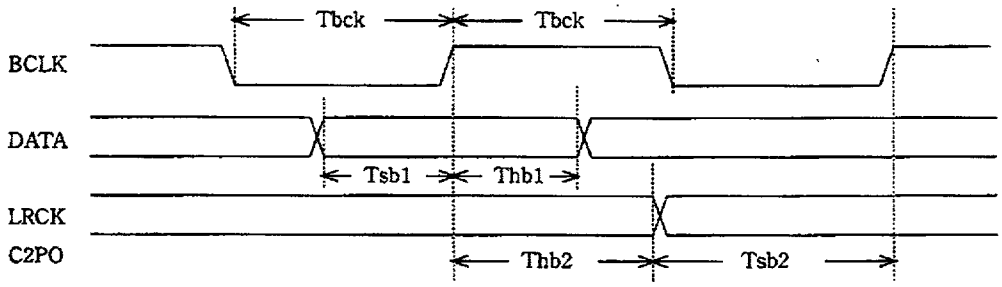


Item	Symbol	Min.	Typ.	Max.	Unit
Address set-up time (In reference to XCS&XWR ↓)	Tsaw	30			ns
Address hold time (In reference to XCS&XWR ↑)	Thaw	20			ns
Data set-up (In reference to XCS&XWR ↓))	Tsdw	50			ns
Data hold time (In reference to XCS&XWR ↑)	Thwd	20			ns
Pulse width of XWR "Low"-level	Twwl	70			ns

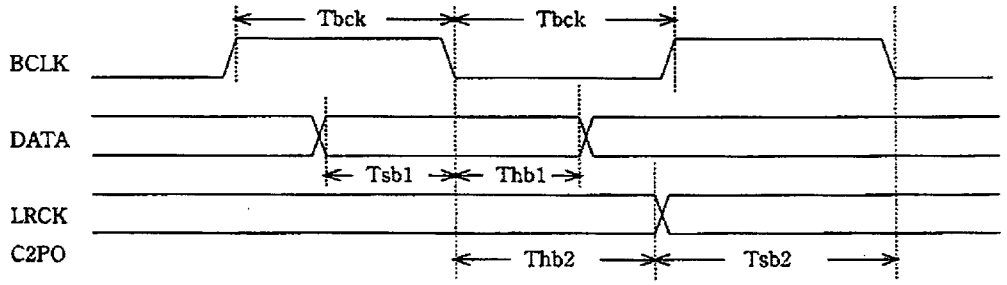
* '&' in the table stands for logical AND.

2. CD DSP Interface

BCKRED = "High"



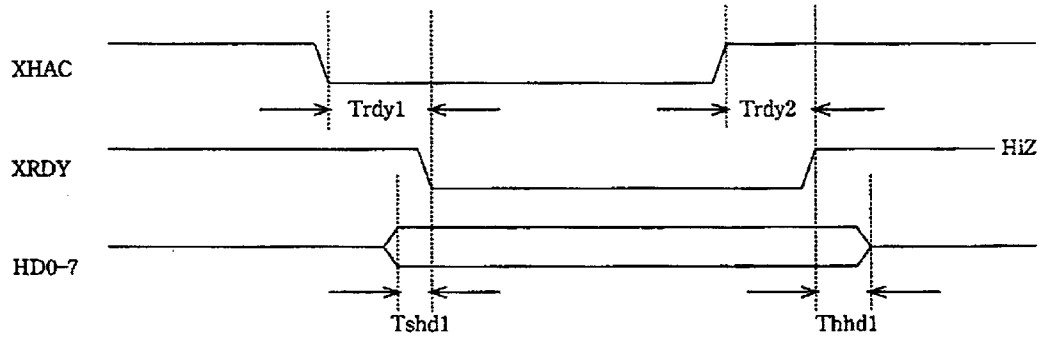
BCKRED = "Low"



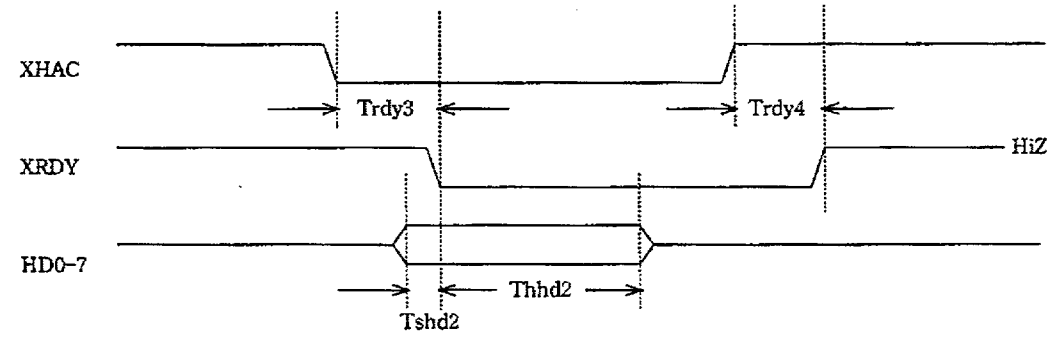
Item	Symbol	Min.	Typ.	Max.	Unit
BCLK frequency	Fbck			5.7	MHz
BCLK pulse width	Tbck	85			ns
DATA set-up time (In reference to BCLK)	Tsb1	50			ns
DATA hold time (In reference to BCLK)	Thb1	50			ns
LRCK, C2PO set-up time (In reference to BCLK)	Tsb2	50			ns
LRCK, C2PO hold time (In reference to BCLK)	Thb2	50			ns

3. Host Interface (Output Load=75pF)

(1) Host memory write (DMAC, CXD1197AQ → host memory)



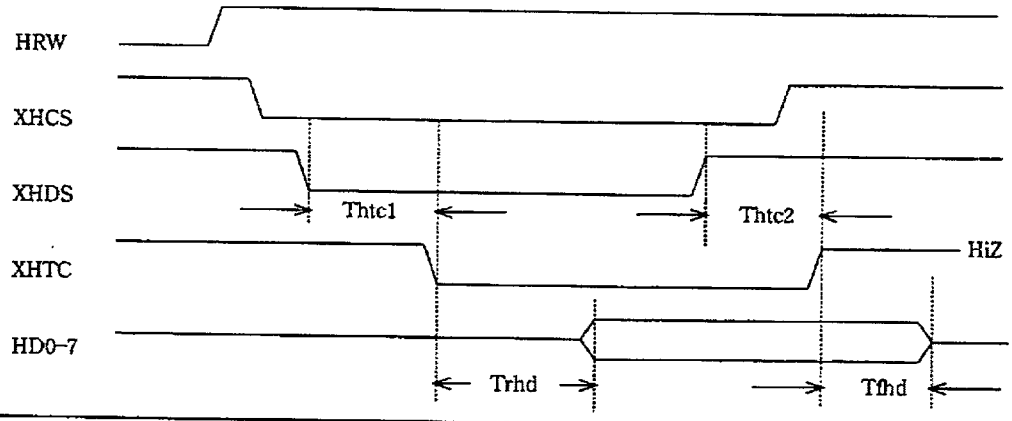
Item	Symbol	Min.	Typ.	Max.	Unit
XRDY fall time (In reference to XHAC↓)	Trdy1	70		145	ns
XRDY float time (In reference to XHAC↑)	Trdy2			75	ns
Data set-up time (In reference to XRDY↓)	Tshd1	0			ns
Data hold time (In reference to XRDY↑)	Thhd1	0			ns



Item	Symbol	Min.	Typ.	Max.	Unit
XRDY fall time (In reference to XHAC↓)	Trdy3			85	ns
XRDY float time (In reference to XHAC↑)	Trdy4			70	ns
Data set-up time (In reference to XRDY↓)	Tshd2	0			ns
Data hold time (In reference to XRDY↑)	Thhd2	55			ns

(2) Host memory read (DMAC, host memory → CXD1197AQ)

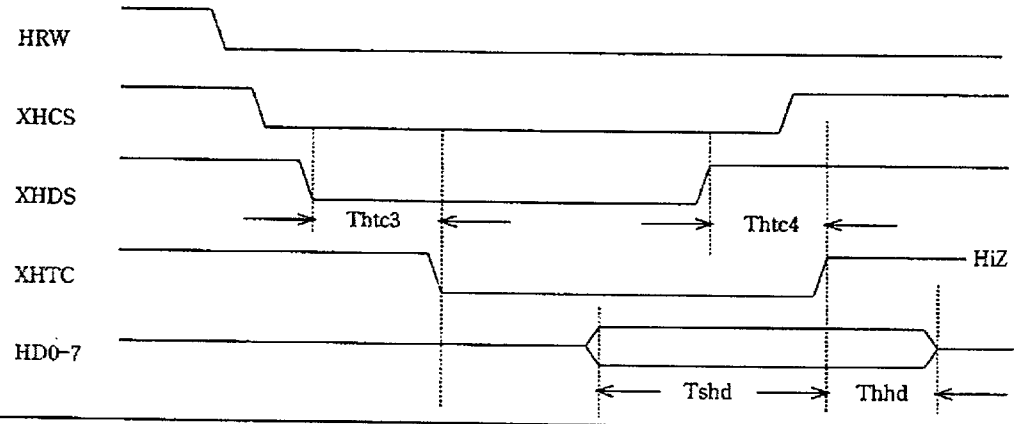
(3) Read



Item	Symbol	Min.	Typ.	Max.	Unit
Data delay time (In reference to XHCS&XHDS↓)	Trhd			60	ns
Data float time (In reference to XHCS&XHDS↑)	Tfhd	0			ns
XHTC fall time	Thtc1	160		250	ns
XHTC float time	Thtc2			25	ns

* '&' in the table stands for logical AND.

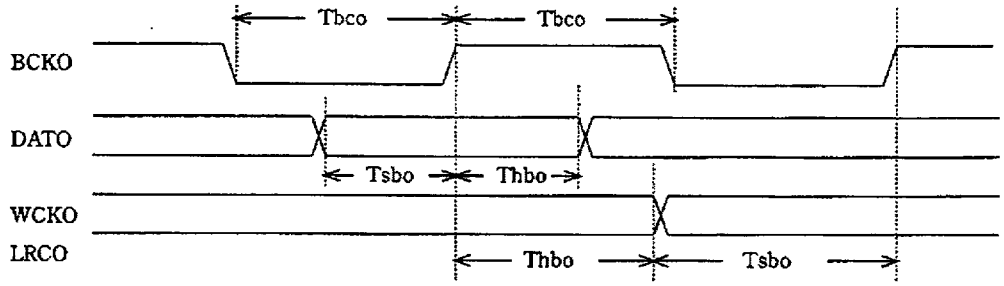
(4)Write



Item	Symbol	Min.	Typ.	Max.	Unit
Data set-up time (In reference to XHCS&XHDS↓)	Tshd	50			ns
Data hold time (In reference to XHCS&XHDS↑)	Thhd	15			ns
XHTC fall time	Thtc3			40	ns
XHTC float time	Thtc4			20	ns

* '&' in the table stands for logical AND.

4. DAC Interface



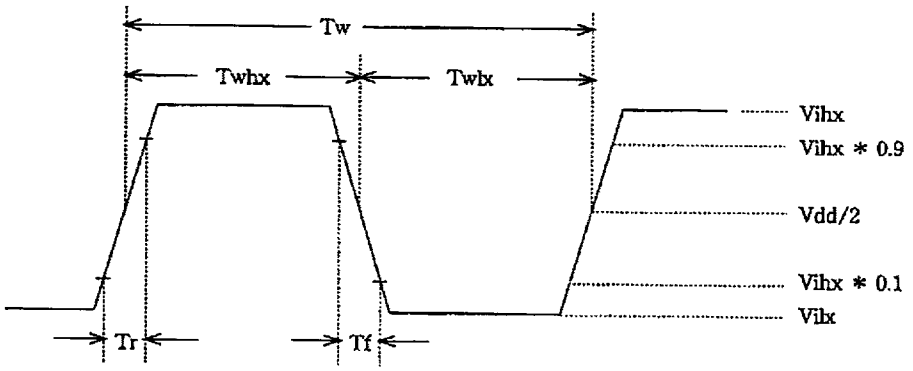
Item	Symbol	Min.	Typ.	Max.	Unit
BCKO frequency	Fbco		8.4672		MHz
BCKO pulse width	Tbco	50			ns
DATO, WCO1, WCO2, LRCO set-up time (In reference to BCKO ↑)	Tsbo	30			ns
DATO, WCO1, WCO2, LRCO hold time (In reference to BCKO ↑)	Thbo	30			ns

5. Pins XTL1 and XTL2

(1) For self-generated oscillation

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	Fmax		16.9344		MHz

(2) For pulse input to Pin XTL1



Item	Symbol	Min.	Typ.	Max.	Unit
"High"-level pulse width	Twhx	20			ns
"Low"-level pulse width	Twlx	20			ns
Pulse period	Tw		59		ns
"High"-level input	Vihx	VDD−1.0			ns
"Low"-level input	Vilx			0.8	ns
Rise time	Tr			15	ns
Fall time	Tf			15	ns

Note: The XTL1 clock should be synchronized with that of the CD DSP. (Use the same oscillator for both clocks.)

Description of Functions

1. Pin Desciption

The pins are described below according to function.

1.1. CD Player Interface (5 lines)

For Sony CD digital signal processing LSIs, direct connection is possible. In the following description, CD digital signal processing LSI will be referred to as CD DSP. Refer to section 2.1.1 for the data format description.

(1) DATA (Data: input)
Serial data stream input from CD DSP.

(2) BCLK (Bit clock: input)
Bit clock signal. Used to strobe data line.

(3) LRCK (Left/right clock: input)
Left/right clock signal. Indicates whether data represents Lch or Rch.

(4) C2PO (C2 pointer: input)
C2 pointer signal. Indicates error status of data input.

(5) EMP (Emphasis: input)
Emphasis signal (positive logic). Indicates whether emphasis is on or not for data from CD DSP.

1.2. Buffer Memory Interface (26 lines)

32 K bytes (256 K bits) of standard SRAM should be used.

(1) XMWR (BUFFER MEMORY WRITE: output)
Write strobe output to memory (negative logic).

(2) XMOE (BUFFER MEMORY OUTPUT ENABLE: output)
Read strobe output to memory (negative logic).

(3) MA0 to MA14 (BUFFER MEMORY ADDRESS: output)
Buffer memory address.

(4) MDB0 to MDB7, MDBP (BUFFER MEMORY DATA BUS: bus)
Buffer memory data bus. Standard 25 KΩ pull-up resistor should be used.
When an 8-bit/word SRAM is connected, the MDBP pin should be left open.

1.3 Sub CPU Interface (17 lines)

(1) XWR (Sub CPU WRITE: input)
Strobe for writing to this IC's internal registers (negative logic).

(2) XRD (Sub CPU READ: input)
Strobe for reading from this IC's internal registers (negative logic).

(3) D0 to D7 (Sub CPU DATA BUS: input/output)
8-bit data bus.

(4) A0 to A4 (Sub CPU ADDRESS: input)
Address lines from sub CPU for selecting this IC's internal register.

(5) XINT (Sub CPU Interrupt: output)
Interrupt request to sub CPU (negative logic).

(6) XCS (CHIP SELECT: input)
Sub CPU CXD1197AQ chip select (negative logic).

1.4. Host (68000) Interface (21 lines)

(1) HRW (READ/WRITE: input)
Determines whether the data bus is in read or write transfer cycle.
When the host performs a status read of the CXD1197AQ, HRW input is "High."
When the host performs input to the CXD1197AQ registers, HRW input is "Low."

(2) HD0 to HD7 (host DATA BUS: input/output)
Host data bus.

(3) XHDS (host DATA STROBE: input)
Data strobe (negative logic).

(4) HA0 to HA3 (host ADDRESS: input)
Address from host for selecting internal register of the CXD1197AQ.

(5) HIRQ (Host interrupt: output)
Interrupt request to host (negative logic). Open drain.

(6) XHCS (CHIP SELECT: input)
Host chip select (negative logic).

(7) HDRQ (DMA REQUEST: output)
DMA request (negative logic). Open drain.

(8) XHAC (DMA ACKNOWLEDGE: input)
DMA acknowledge (negative logic).

(9) XHTC (DATA TRANSFER ACKNOWLEDGE: input/output)
Acknowledges completion of data transfer (negative logic). Open drain output.

(10) XRDY (READY: output)
Data ready (negative logic). Open drain.

(11) XRIN (REMOTE CONTROLLER INTERRUPT: output)
Remote contoller interrupt request (negative logic). Open drain.

1.5. DAC Interface (5 lines)

Please refer to section 2.1.2 for output format description.

(1) BCKO (BIT CLOCK OUTPUT: output)
Bit clock output to D/A converter.

(2) WCO1 and WCO2 (WORD CLOCK OUTPUT: output)
Word clock output to D/A converter.

(3) LRCO (L/R CLOCK OUTPUT: output)
Left/right clock output to D/A converter.

(4) DATO (DATA OUTPUT: output)
Data output to D/A converter.

1.6. General (14 lines)

(1) MUTE (MUTE: output)
When the D/A converter data (DATO) is muted, the output is "High."

(2) XRST (RESET: input)
Chip reset input (negative logic).

(3) XTL1 (X'TAL 1: input)

(4) XTL2 (X'TAL 2: output)
A 16.9344 MHZ crystal oscillator should be connected between XTL1 and XTL2. (The capacitor value depends on the crystal oscillator.) Alternatively, a 16.9344 MHz clock can be input to XTL1.

(5) CLK (Clock: output)
Outputs 16.9344 MHz clock. If this output is not to be used, CLK output can be fixed at "Low."

(6) HCLK (Half clock: output)
Outputs 8.4672 MHz clock. If this output is not to be used, HCLK output can be fixed at "Low."

(7) TD0 to TD7 (TEST DATA 0 to 7: input/output)
Data pins for testing this IC. Pull-up with a 25 kΩ (typ.) resistor.
Under normal conditions, these pins should be left open.

1.7. Power Supply Pins (12 lines)
V_{DD}: 4 lines; GND: 8 lines.

2. Sub CPU Register

2.1. Write Register

2.1.1. DRVIF (Drive Interface) Register

This register controls the interface mode with the CD DSP. After the CXD1197AQ is reset, the sub CPU sets this register to match the CP DSP interface.

bit 7 C2PL1ST (C2PO Lower-byte 1st)

'H': The 2 byte input of the C2PO data is input in order of lower-byte to upper-byte.

'L': The 2 byte input of the C2PO data is input in order of upper-byte to lower-byte. The upper-byte is the high 8-bit data from the CD DSP including the MSB; the lower-byte is the low 8-bit data from the CD DSP including the LSB. For example, the header minute is input to the lower-byte and the header second input to the upper-byte.

bit 6 LCHLOW (LCH LOW)

'H': When LRCK is 'L', data is regarded as Lch data.

'L': When LRCK is 'H', data is regarded as Lch data.

bit 5 BCKRED (BCLK rising edge)

'H': Data is strobed at the rising edge of BCLK.

'L': Data is strobed at the falling edge of BCLK.

bits 4 & 3 BCKMD1,0 (BCLK mode 1, 0)

These bits are set to determine how many BCLKs are output within one WCLK1 period by the CD DSP.

BCKDM1	BCKDM0	
'L'	'L'	16BCLKs/WCLK
'L'	'H'	24BCLKs/WCLK
'H'	'X'	32BCLKs/WCLK

bit 2 LSBIST (LSB first)

'H': Interface set for CD DSP data output LSB first.

'L': Interface set for CD DSP data output MSB first.

bit 1 RESERVED

bit 0 RESERVED

The bits of the DRVIF register should not be changed if one of the following conditions exists:

(1) The decoder is not disabled.

(2) During ADPCM playback. (Equivalent to real-time and sound map modes.)

(3) During CD-DA playback.

Immediately following sub CPU resets, setting the DRVIF register is recommended.

Also, in case of CD LRCK signal from the DSP is stopped for some reason, the DRVIF register should be reset before the sub CPU restarts LRCK.

Table 2.1.1 shows the settings for bits 2 to 7 when used with a Sony CD DSP. The input timing chart is shown in Figures 2.1.1 (1) - (3).

Sony CD DSP	DRVIF register						Timing chart
	bit7	bit6	bit5	bit4	bit3	bit2	
	c2po	lrck	bedg	bck1	bck0	lsb	
CDL30 Series CDL35 Series	L	L	L	L	H	L	Fig. 2.1.1(1)
CDL40 Series (48-bit slot mode)	L	L	H	L	H	L	Fig. 2.1.1(2)
CDL40 Series (64-bit slot mode)	L	H	L	H	X	H	Fig.2.1.1(3)

Table 2.1.1 DRVIF Register Settings

Note 1:

CDL30Series	CXD1125Q/QZ, CXD1130Q/QZ, CXD1135Q/QZ CXD1241Q/QZ, CXD1245Q, CXD1246Q/QZ CXD1247Q/QZ/R etc
CDL35Series	CXD1165Q, CXD1167Q/QZ/R etc
CDL40Series	CXD2500Q/QZ etc

2.1.2 COFIG (Configuration) Register

This register is set to accomodate the configuration of the hardware peripheral to the CXD1197AQ. This resister is set by the sub CPU when the CXD1197AQ is reset.

bit 7 XHSTWAIT (/Host wait)
'H': No delay occurs between CXD1197AQ <=> Host data transfers.
'L': A delay occurs between CXD1197AQ <=> Host data transfers. (Details are given in later section.)

bit 6 RESERVED
For normal operation should be set to 'L'.

bit 5 SPECTL (Sound parameter error control)

bit 4 SPMCTL (Sound parameter majority control)
These two bits control sound processing for ADPCM decoder playback. (Please see section7 for details.)

bit 3 DACMODE (D/A converter mode)
'H': Output to D/A converter performed according to Fig. 2.1.2 (1).
'L': Output to D/A converter performed according to Fig. 2.1.2 (2).

bit 2 9 BITRAM
'H': A 9 -bit/word SRAM to be used.
'L': An 8- bit/word SRAM to be used.

bit 1 CLKDIS (CLK disable)
'H': CLK pin is fixed 'L'.
'L': A 16.9344 MHz clock is output from the CLK pin.

bit 0 HCLKDIS (Half CLK disable)
'H': HCLK pin is fixed 'L'.
'L': An 8.4672 MHz clock is output from the HCLK pin.

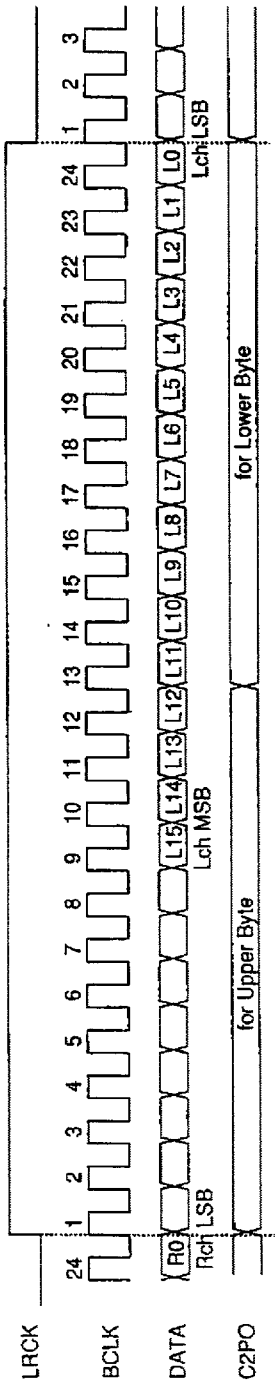


Fig. 2.1.1. (1) CDL30, 35 Series Timing Chart

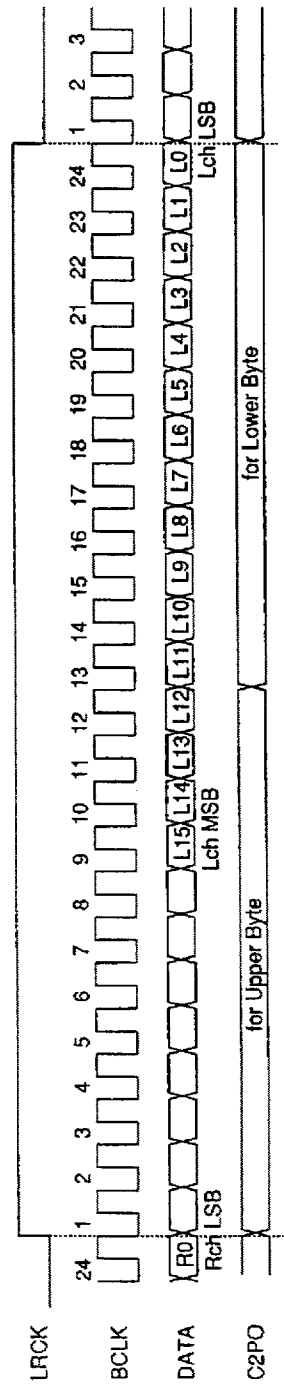


Fig. 2.1.1. (2) CDL40 Series, 48-bit Slot Mode Timing Chart

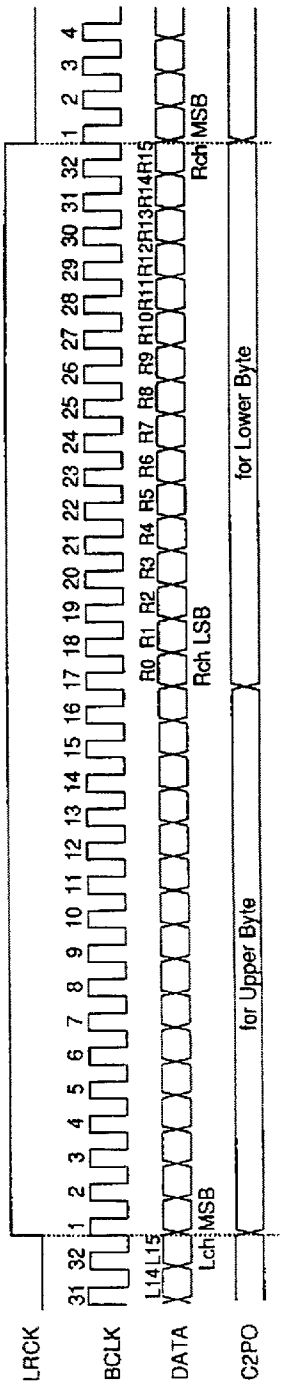


Fig. 2.1.1. (3) CDL40 Series, 64-bit Slot Mode Timing Chart

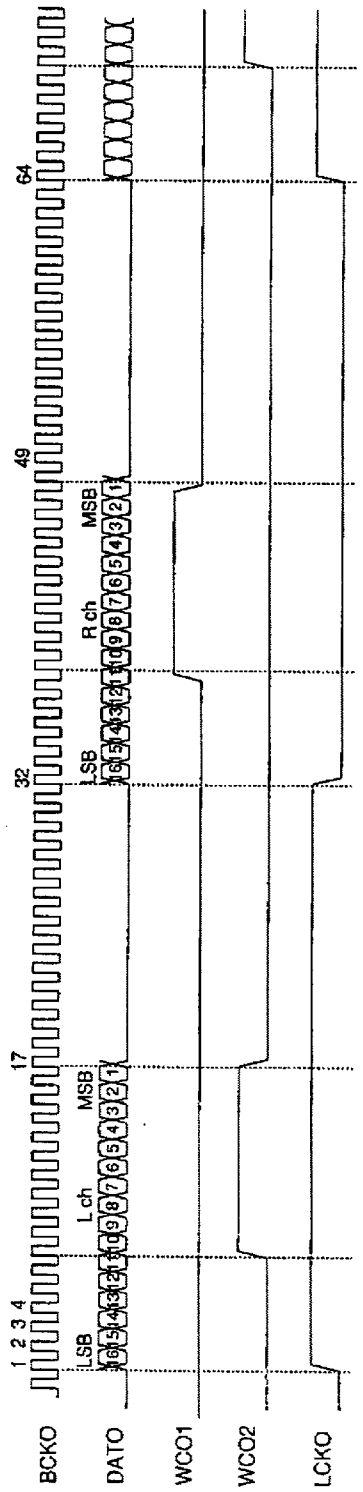


Fig. 2.1.2. (1) DACMODE = 'High' Output Format

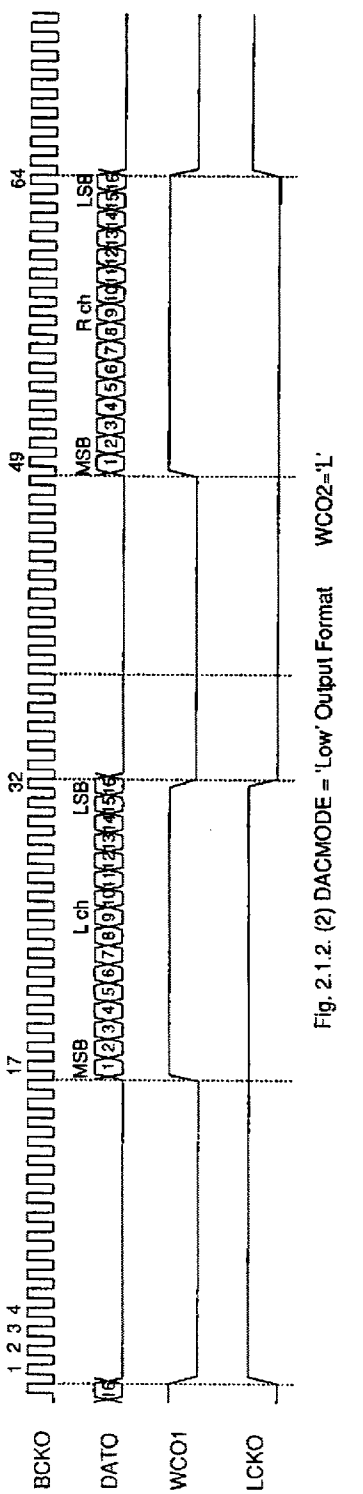


Fig. 2.1.2. (2) DACMODE = 'Low' Output Format WCO2='L'

2.1.3. DECODER CONTROL (DECCTL) Register

bit 7 ENDLADR (Enable drive last address)

'H': Setting this bit to 'H' enables the DLADR (Drive last address).
When the decoder is in write-only, real-time correction mode and the CD is in DA mode, if the DADRC and DLADR become equal, writing of the driver data to the buffer is terminated.

'L': Setting this bit to 'L' disables the DLADR (Drive last address).
Writing of driver data to the buffer is not terminated if the DADRC and DLADR become equal when the decoder is in write-only, real-time correction mode and the CD is in DA mode.

bit 6 ECCSTR (ECC strategy)

'H': All error flags are taken into account for error correction.

'L': All error flags are not taken into account for error correction.
Erasure correction is not performed. This bit should be set 'L' when an 8 bit/word SRAM is used or double-speed playback is performed.

bit 5 MODESEL (Mode select)

bit 4 FORMSEL (Form select)

When AUTODIST='L', sectors are corrected according to MODE and FORM as shown below

MODESEL	FORMSEL	
'L'	'L'	MODE1
'H'	'L'	MODE2, FORM1
'H'	'H'	MODE2, FORM2

bit3 AUTODIST (Auto-distinction)

'H': Error correction is performed according to the MODE byte and FORM bit read from the drive.

'L': Error correction is performed according to bits 4 & 5 of the MODESEL and FORMSEL bits.

bits 0 to 2 DECMD 0 to 2 (Decoder mode 0 to 2)

DECMD2	DECMD1	DECMD0	
'L'	'L'	'X'	Decoder disable
'L'	'H'	'X'	Monitor-only mode
'H'	'L'	'L'	Write-only mode
'H'	'L'	'H'	Real-time correction mode
H'	'H'	'L'	Repeat correction mode
'H'	'H'	'H'	CD-DA mode

When the CHPCTL register CD-DA bit (bit 4) is set 'H', the decoder should be disabled and the CD-DA mode activated.

2.1.4. DLADR-L

2.1.5. DLADR-H

When the decoder is in write-only, real-time correction mode and the CD-DA mode is active, the DLADR lines determine the last address for data loaded from the driver to the buffer. When the decoder is in the mode described above and the ENDLADR bit (bit 7) of theDECCTL register is set 'H', data is loaded from the driver to the buffer at the address specified by DLADR and further buffer writes are prohibited.

2.1.6. Chip Control (CHPCTL) Register

bit 7 SM MUTE (Sound map mute)
When this bit is set 'H', the audio output is muted during sound map ADPCM playback.

bit 6 RT MUTE (Real time mute)
When this bit is set 'H', the audio output is muted during real time ADPCM playback.

bit 5 CD-DA MUTE
When this bit is set 'H', the audio output is muted during CD-DA (digital audio) disc playback with bit 4 'H'. For a disc (or a track) playback other than CD-DA, this bit has no effect on the audio output.

bit 4 CD-DA
'H': For CD-DA (digital audio) disc audio playback, this bit is set 'H'.
'L': If CD-DA disc audio playback is not desired, this bit should be set 'L'.

bit 3 SWOPN (Sync window open)
'H': When this bit is set 'H', the window for SYNC mark detection is opened. At this time the SYNC protection circuit is disabled.
'L': When this bit is set 'L', the SYNC protection circuit controls the window for SYNC mark detection.

bit 2 RPSTART (Repeat correction start)
When the decoder is set to recursive correction mode and this bit is set 'H', sector error correction is started. After correction is started this bit is automatically reset to 'L', so CPU resetting of the bit is unnecessary.

bit 1 CHPRST (Chip reset)
When this bit is set 'H', the IC is initialized. After initialization is complete, the bit automatically becomes 'L', so CPU resetting of the bit is unnecessary.

bit 0 RTADPEN (Real-time ADPCM enable)
During real-time ADPCM playback, the CPU sets this bit 'H'.

2.1.7. INTMSK1 (Interrupt Mask 1) Register

When each bit of this register is brought 'H', an interrupt request to the CPU is enabled corresponding to the interrupt status. (The interrupt pin is activated when the interrupt status condition is met.) The interrupt status remains unaffected.

bits 2 to 7 RESERVED
Should be fixed to 'L'.

bit 1 RCDTEMPT (Remote controller data empty)
When the host retrieves the last word of data from the RMCNDT register, the RCDTEMPT status becomes "1."

bit 0 RLSTEMPT (Result empty)
When the host retrieves the last word of data from the RESULT register, the RSLTEMP status becomes "1." (Used when 17 bytes or more of "Result" data are sent to host.)

2.1.8. INTMSK2 (Interrupt Mask 2) Register

When all bits of this register are set 'H', an interrupt request to the CPU is enabled corresponding to the interrupt status. (The Interrupt pin is activated when the interrupt status condition is met.) The interrupt status remains unaffected.

bit 7 DRVOVRN (Drive over run)
When the ENDLADR bit (bit 7) of the DECCTL register is set 'H' while the decoder is in write-only, real-time correction mode, if DADRC and DLADR become equal, the DRVOVRN status becomes "1." If the decoder is in CD-DA mode, the DRVOVRN status becomes "1" if DADRC and DLADR become equal regardless of the ENDLADR bit value.

bit 6 DECTOUT (Decoder time out)
After the decoder has been set to the monitor-only, write-only, or real-time correction mode, if a SYNC mark is not detected within 3 sector periods (40.6ms for normal playback speed), the DECTOUT status becomes "1."

bit 5 RESERVED
Normally, should be fixed at 'L'.

bit 4 RTADPEND (Real time ADPCM end)
When 1 sector of real time ADPCM decoding is complete, the ADPEND status becomes "1."

bit 3 HDMACMP (host DMA complete)
When data transfer between the Host and the buffer memory has been executed by HXFRC, the HDMACMP status becomes "1."

bit 2 DECINT (Decoder interrupt)
When the decoder is in the write-only, monitor-only, or real-time correction mode, and a SYNC Mark is detected or inserted, the DECINT status becomes "1." However, when the SYNC Mark detection window is open and the SYNC Mark interval is less than 2352 bytes, the DECINT is not tripped. Also, when the decoder is operating in the recursive correction mode, DECINT is tripped every time a correction is completed.

bit 1 HSTCMND (host command)
When the host writes to the COMMAND register, the HSTCMND status becomes "1."

bit 0 HCRISD (Host chip reset issued)
When the host clears the CXD1197AQ, the HCRISD status becomes "1."

2.1.9. CLRINT1 (Clear interrupt status1) Register

When a bit in this register becomes 'H', the corresponding interrupt status is cleared. After the interrupt status is clear, the bit is automatically reset to 'L', so resetting the bit with the CPU is unnecessary.

bits 2 to 7 RESERVED

Setting these bits to 'H' is prohibited.

bit 1 RCDTEMP (Remote controller data empty)

bit 0 RSLTEMP (Result empty)

2.1.10. CLRINT2 (Clear interrupt status2) Register

When a bit in this register becomes 'H', the corresponding interrupt status is cleared. After the interrupt status is clear, the bit is automatically reset to 'L', so resetting the bit with the CPU is unnecessary.

bit 7 DRVOVRN (Drive overrun)

bit 6 DECTOUT (Decoder time-out)

bit 4 ADPEND (ADPCM end)

bit 3 HDMACMP (host DMA complete)

bit 2 DECINT (Decoder interrupt)

bit 1 HSTCMND (host command)

bit 0 HCRISD (Host chip reset issued)

2.1.11. HXFR-L (Host transfer-low)

2.1.12. HXFR-H (Host transfer-high)

bit 7 DISHXFRC (Disable host transfer counter)

'H': HXFRC disables "transfer complete" for data transfers between the host and the buffer. When transfer is complete, the host must set the BFRD (bit 6) and BFWR (bit 5) bits of the HCHPCTL register to 'L'.

'L': HXFCR enables "transfer complete" for data transfers between the host and buffer. Transfer complete is indicated when HXFRC becomes 000hex.

bits 4 to 6 RESERVED

bit 3 HXFR11

Bit 11 (MSB) of HXFR (host transfer counter).

bit 2 HXFR10

Bit 10 of HXFR.

bit 1 HXFR9

Bit 9 of HXFR.

bit 0 HXFR8

Bit 8 of HXFR.

The HXFR (host transfer) register controls the number of data transfers between the host and the buffer. When the DISHXFRC bit is set 'L' and data transfer between the host and the buffer is initiated, the sub CPU loads the data transfer count to the HXFR register. Actual loading occurs for the following conditions:

(1) When the host enables buffer ==> host data transfer. (The BFRD bit (bit 7) of the HCHPCTL register is set 'H'.)

(2) When the host enables host ==> buffer transfer (The FWR bit (bit 6) of the CHPCTL register is set 'H'.) provided the SMEN bit (bit 7) of the ADPCTL register is 'L'.

2.1.13. HADR-L

2.1.14. HADR-H

The HADR (Host address) register stores the first address for data transfers between the host and buffer. The HADR register data is loaded from the HADRC for the following conditions

(1) When the host enables buffer ==> host data transfer.(The BFRD bit (bit 7) of the HCHPCTL register is set 'H'.)

(2) When the host enables host ==> buffer transfer (The BFWR bit (bit 6) of the HCHPCTL register is set 'H'.) provided the SMEN bit (bit 7) of the ADPCTL register is 'L'.

2.1.15. DADRC-L

2.1.16. DADRC-H

The DADRC is a counter for storing the address for writing data from the driver to buffer. When data is to be written from the driver to buffer, the DADRC value is output to Pins MA0 to MA14. After each byte is written to buffer, DADRC is incremented.

Before the decoder enters write-only, real-time correction, or CD-DA modes, the CPU loads the first address of the buffer to the DADRC counter.

The sub CPU can load the DADRC counter at any time; however, when the decoder is in one of the above modes the DADRC contents should not be written over.

2.1.17. RMCNDT (Remote controller data)

The RMCNDT register stores remote control data and is formed by 3 bytes of FIFO data. The number of bytes to be sent to the host is determined by RCDTBYTE bits 0 & 1 (bits 3 & 4) of the HIFCTL register. After the sub CPU loads the byte number specified by these two bits, the XRIN pin can be activated.

2.1.18. HIFCTL (host interface control)

bit 7 CLRBUSY (Clear busy)

Setting this bit 'H' clears the HIFSTS register BUSYSTS bit.

bit 6 CLRRSLT (Clear result)

Setting this bit 'H' clears the RESULT register.

bit 5 CLRRCDT (Clear RMCNDT)

Setting this bit 'H' clears the RMCNDT register. These 3 bits are automatically reset to 'L' after either the register or status clears are performed, eliminating the need for sub CPU resetting.

bits 3 & 4 RCDTBYTE 0 & 1 (RMCNDT BYTE 0 & 1)

These two bits determine the number of bytes to be sent to the host from the remote control register as shown in the table below.

RCDTBYTE1	RCDTBYTE0	Byte count
'L'	'L'	Prohibited
'L'	'H'	1
'H'	'L'	2
'H'	'H'	3

bit 2 HINT#2

Assumes the same value as HINTSTS#2 of the host STATUS register.

bit 1 HINT#1

Assumes the same value as HINTSTS#1 of the host STATUS register.

bit 0 HINT#0

Assumes the same value as HINTSTS#0 of the host STATUS register.

2.1.19. RESULT

This register is used to send results to the host and is formed by 16 bytes of FIFO data.

2.1.20. TEST1 to 3

These registers are used for storing CXD1197AQ test results.
Normally, all bits should be set to 'L'.

2.1.21. ADPMNT-H

The ADPMNT-H register provides the upper 6 bits of the first playback sector during real-time ADPCM playback Values which can be written to this register are 00, 0C, 18, 24, 30, 3C, 48, and 54 hex.

2.1.22. CI

The CI register provides the coding information byte used in real-time ADPCM playback.

bit 6 EMPHASIS
Set 'H' when an emphasised ADPCM sector is played back.

bit 4 BITLNGTH (Bit length)
Indicates the bit length of ADPCM playback coding information.
'H': 8 bits
'L': 4 bits

bit 2 FS (Sampling frequency)
Indicates the ADPCM playback sampling frequency.
'H': 18.9 KHz
'L': 37.8 KHz

bit 0 M/S (MONO/STEREO)
Indicates whether the ADPCM coding information is mono or stereo.
'H': Stereo
'L': Mono

bits 1, 3, 5, & 7 RESERVED
Normally, should be set 'L'.

2.1.23. AUDIOCTL (Audio control)

bit 7 RTADPCLR (Real-time ADPCM clear)

(1) During real-time ADPCM playback (DECSTS register RTADPBSY bit is 'H'.), when the RTADPCLR bit is set 'H' the following actions result:
•ADPCM decoder is shutdown. (Noise may occur.)
•ADPEND interrupt status is activated.
Note: Before this bit is set 'H', the ADPEN bit (CHPCTL register bit 0) must be set 'L'.

(2) If RTADPCLR is set 'H' at any time other than real-time ADPCM playback, no action results.

bit 6 RESERVED
Normally, should be set 'L'.

bit 5 SMBF2 (Sound map buffer2)
Indicates the number of buffer areas for the sound map ADPCM.
'H': 2 buffer areas for the sound map.
'L': 3 buffer areas for the sound map.

bit 4 XATNIF (/ATTENUATOR infinite)

Selects attenuation factor.

'L': When ATVO 0 to 3 register is between 1E and 7Fhex, the attenuation factor is infinite.

'H': When ATVO 0 to 3 register is between 1E and 7Fhex, the attenuation factor is approx. 30dB.

bit 3 DAMIXEN (Digital audio mixer enable)

'H': Attenuator and mixer operate over the CD-DA mode.

'L': Attenuator and mixer do not operate.

bits 0 to 2 RESERVED

Normally, should be set 'L'.

All write registers are set to 00hex when the IC is reset by hardware or software. The only exception is the HCRISD bit of the INTMSK2 register which is not affected by host software reset. The HCRISD bit is set to 'L' by host hardware reset or sub CPU software reset. Hardware reset is performed by a 'L' pulse to the XRST pin. The sub CPU or host controls software reset of the CXD1197AQ.

2.2. Read Registers

Throughout the description for the ECCSTS, DECSTS, HDRFLG, HDR, SHDR, and CM ADR H registers, a "current sector" is denotes a sector which is effective in regard to the decoder interrupt (DECINT). In the monitor-only and write-only modes, the sector transferred from the CD DSP immediately before decoder interrupt is known as the "current sector." For the real-time correction and recursive correction modes, the sector which completes error detection correction is known as the "current sector."

2.2.1. ECCSTS (ECC status)

bit 7 EDCALL0 (EDC ALL 0)

When 4 successive EDC parity bytes generate no error flags and the value is 00h for the current sector, the EDCALL0 flag becomes 'H'.

bit 6 ERINBLK (Erasure in block)

(1) When the decoder is in real-time mode for monitor-only, write-only, and ierasure correction prohibited operation, if 1 or more byte error flags (C2PO) occur over the current sector of data from the CD DSP (excluding the SYNC Mark), ERINBLK is tripped.

(2) When the decoder is in real-time mode for erasure operation, if 1 or more byte error flags (MDBP) occur over the current sector of data from the CD DSP (excluding the SYNC Mark), ERINBLK is tripped.

bit 5 CORINH (Correction inhibit)

When the DECCTL register AUTODIST bit is 'H' and MODE and FORM of the current sector can not be determined, CORINH becomes 'H'. ECC and EDC is not executed for this sector. If AUTODIST is 'L', CORINH is disregarded. CORINH also becomes 'H' under following conditions (AUTODIST must be 'H'):

(1) C2 pointer of MODE byte was 'H'.

(2) MODE byte value other than 01hex or 02hex present.

(3) MODE byte value was 02hex and C2 pointer of SUBMODE byte was 'H'.

bit 4 CORDONE (Correction done)

Indicates error correction was performed over a byte in the current sector.

bit 3 EDCOK

Indicates no-error result for EDC check over current sector.

bit 2 ECCOK

Indicates that current sector has become error free from the Header to P parity byte. (This bit will be ignored in sectors MODE2 and FORM2.)

EDCOK	ECCOK	Description
'L'	'L'	Current sector error
'L'	'H'	(1),(2), or (3) error (1) EDC miss (2) Miss-correction (3) FORM2 header byte error
'H'	'L'	(1) EDC miss or (2) P parity byte error
'H'	'H'	No current sector error

bit 1 CMODE (Correction mode)

bit 0 CFORM (Correction form)

These bits indicate that a MODE and/or FORM error correction was performed when the decoder was either in the real-time correction or recursive correction mode.

CFORM	CMODE	
'X'	'L'	MODE1
'L'	'H'	MODE2, FORM1
'H'	'H'	MODE2, FORM2

2.2.2. DECSTS (Decoder status) Register

bit 5 RTADPBSY (Real time ADPCM busy)

Becomes 'H' during real-time ADPCM playback.

bit 1 SHRTSCT (Short sector)

Indicates SYNC Mark interval was less than 2351 bytes. Short sector are not successfully stored in buffer.

bit 0 NOSYNC

Indicates that a SYNC Mark has been inserted where expected SYNC Mark detection failed.

2.2.3. Header Flag (HDRFLG) Register

Indicates error flag status for each byte of Header and Sub Header registers.

2.2.4. Header (HDR) Register

4-byte register which indicates the current sector Header byte. By setting the sub CPU address to 03hex and performing consecutive reads, the current sector Header byte value is written to the MINUTE byte, which can be readout.

2.2.5. Sub Header (SHDR) Register

4-byte register which indicates the current sector Sub Header byte. By setting the sub CPU address to 04hex and performing consecutive reads, the current sector Sub Header byte value is written to the FILE byte, which can be readout.

In reference to the contents of the HDRFLG, HDR, and SHDR registers:

(1) Value is result of correction for real-time and repeat correction modes.

(2) Value is raw data value from driver for monitor-only and write-only modes.

Bits CMODE and CFORM of ECCSTS register show which FORM/MODE the decoder determines in this sector by using raw data from the disc. Due to correction errors, etc., the value of these bits, the MODE byte of the HDR resister, and Sub mode byte (bit 5) of the SHDR resister may differ.

2.2.6. Current Minute Address High (CMADR-H) Register

Indicates the upper 7 bits of buffer address to which the current sector minute byte is writing (corrected data). (Lower 8 bits are 00hex.)

2.2.7. Interrupt Status1 (INTSTS1) Register

Each bit indicates the current value of its corresponding interrupt status. This register has does not affect the values of the INTMSK register.

bit 1 RCDTEMPT (Remote controller data empty)

bit 0 RSLTEMPT (Results empty)

2.2.8. Interrupt Status2 (INTSTS2) Register

Each bit indicates the current value of its corresponding interrupt status. This register does not affect the values of the INTMSK register.

bit 7 DRVOVRN (Drive over run)

bit 6 DECTOUT (Decoder time out)

bit 4 ADPEND (ADPCM end)

bit 3 HDMACMP (host DMA complete)

bit 2 DECINT (Decoder interrupt)

bit 1 STCMND (host command)

bit 0 HCRISD (Host chip reset issued)

2.2.9. ADPCI (ADPCM coding information) Register

bit 7 MUTE

When DA data is muted, becomes 'H'.

bit 6 EMPHASIS

When ADPCM data is emphasized, becomes 'H'.

bit 5 ADPBUSY

When ADPCM is decoding, becomes 'H'.

bit 4 BITLNGTH (Bit length)

Indicates bit length of ADPCM playback coding information.

'H': 8 bits

'L': 4 bits

bit 2 FS (Sampling frequency)

Indicates sampling frequency of ADPCM playback.

'H': 18.9 KHz

'L': 37.8 KHz

bit 0 M/S (MONO/STEREO)

Indicates whether the ADPCM coding information is mono or stereo.

'H': Stereo

'L': Mono

2.2.10. HXFRC-L (Host transfer counter-low)

2.2.11. HXFRC-H (Host transfer counter-high)

HXFRC is a counter which indicates the number of remaining bytes to be transferred between the buffer and the host. Before data transfer data is loaded to HXFRC as shown in the table below. Loading occurs immediately after the host sets the BFRD and BFWR bits (bits 6 & 7) of the HCHPCTL register 'H'.

SMEN BFRD BFWR	HXFRC load value		
'L'	'L'	'H'	HXFR (from sub CPU register)
'X'	'H'	'L'	HXFR (from sub CPU register)
'H' (For sound map data transfer)	'L'	'H'	2304 (900hex)

HXFRC is decremented after data is read from buffer (BFRD='H') or data is transferred from the host to the CXD1197AQ.

2.2.12. HADRC-L (Host address counter-low)

2.2.13. HADRC-H (Host address counter-high)

The HADRC counter maintains the current address for data transfers between buffer and the host. Before data transfer data is loaded to HADRC according to the value of SMEN (ADPCTL register bit 7). Data transfer occurs when the host sets the BFRD and BFWR bits (bits 6 & 7) of register HCHPCTL 'H'.

SMEN	BFRD	BFWR	HADRC load value
'L'	'L'	'H'	HADR (from sub CPU register)
'X'	'H'	'L'	HADR (from sub CPU register)
'H' (For sound map data transfer)	'L'	'H'	600Chex, 6A0Chex, or 740Chex

The HADRC counter value is output to Pins MA0 to MA14 during data transfers between the host and buffer. HADRC is incremented after 1 byte of data is read from the buffer to the driver (BFRD='H') or written to the buffer from the driver (BFWR='H').

2.2.14. DADRC-L

2.2.15. DADRC-H

2.2.16. HIFSTS1 (Host interface status1) Register

bit 2 HINSTS#2 (Host interrupt status#2)

Becomes 'H' when data is written from the sub CPU to HINT#2 (HIFCTL register bit 2).

Becomes 'L' when data is written from the host to CLRINT#2 (Control register bit 2). This bit is used for monitoring the host interrupt status.

bit 1 HINSTS#1 (Host interrupt status#1)

Becomes 'H' when data is written from the sub CPU to HINT#1 (HIFCTL register bit 2).

Becomes 'L'when data is written from the host to CLRINT#2 (Control register bit 1). This bit is used for monitoring the host interrupt status.

bit 0 HINSTS#0 (Host interrupt status#0)
Becomes 'H' when data is written from the sub CPU to HINT#0 (HIFCTL register bit 0). Becomes 'L' when data is written from the host to CLRINT#0 (Control register bit 0). This bit is used for monitoring the host interrupt status.

2.2.17. HIFSTS2 (Host interface status2)

bit 7 BUSYSTS (BUSY status)
The value of this bit is the same as that of the host Status Register BUSYSTS (bit 7). These bits becomse 'H' when the host writes a command to the command register. When the sub CPU sets the CLRBUSY bit of the HIFCTL register these bits become 'L'.

bit 6 RCDTWRDY (RMCNDT write ready)
'H' when the RMCNDT register is not full.

bit 5 RCDTEMPT (RMCNDT empty)
'H' when the RMCNDT register is empty.

bit 4 RSLWRDY (Result write ready)
'H' when the Result register is not full. At this time, results from sub CPU command executions can be written to the result register.

bit 3 RSLEMPT (Result empty)
'H' when the Result register is empty. Indicates that the host has read the status (Result register) from the sub CPU.

bit 2 PRMRRDY (Parameter read ready)
'High' when the Parameter register is not empty. At this time, the sub CPU can read the command parameters from the Parameter register.

bit 1 DMABUSY (DMA busy)
'H' when data transfer is in process between the host and buffer memory. Data transfer is intitiated when the host sets either the BFRD bit (bit 7) or BFWR bit (bit 6) of the HCHPCTL register 'H'. DMABUSY is reset to 'L' when one of following conditions is met.
•After HXFRC becomes 00hex, the data transfer FIFO register (WRDATA or RDDATA) becomes empty
•If data transfer is terminated due to a DMA hang-up (DMAHUP status).

bit 0 RINTSTS (Remote controller interrupt status)
'H' when data has been written to the sub CPU RMCONDT register. After host reads RMCONDT register, this bit becomes 'L'. This bit is used to monitor the remote controller interrupt status.

2.2.18. HSTPRM (Host parameter)

The host command parameter can be read from this register which is formed by a 10 bytes of FIFO data.

2.2.19. HSTCMD (Host command)

The host command can be read from this register.

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DRVIF	00	C2PO L1st	LCH LOW	BCK RED	BCKL MD1	BCKL MD0	LSB 1st	'L'	'L'
CONFIG	01	XHST WAIT	'L'	SPE CTL	SPMJ CTL	DAC MODE	9bit RAM	CLK DIS	HCLK DIS
DECCTL	02	EN DLADR	ECC STR	MODE SEL	FORM SEL	AUTO DIST	DEC MD2	DEC MD1	DEC MD0
DLADR -L	03	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DLADR -H	04	'L'	bit14	bit13	bit12	bit11	bit10	bit9	bit8
CHPCTL	05	SM MUTE	RT MUTE	CDDA MUTE	CD-DA	SW OPEN	RPS TART	CHP ST	RTADP EN
INTMSK 1	06	'L'	'L'	'L'	'L'	'L'	'L'	RCDT EMPT	RSLT EMPT
INTMSK 2	07	DRV OVRN	DEC TOUT	DMA HUP	RTADP END	HDMA CMP	DEC INT	HST CMND	HCR ISD
INTCLR 1	08	'L'	'L'	'L'	'L'	'L'	'L'	RCDT EMPT	RSLT EMPT
INTCLR 2	09	DRV OVRN	DEC TOUT	'L'	RTADP END	HDMA CMP	DEC INT	HST CMND	HCR ISD
HXFRC -L	0A	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HXFRC -H	0B	DIS HXFRC	'L'	'L'	'L'	bit11	bit10	bit9	bit8
HADRC -L	0C	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HADRC -H	0D	'L'	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DADRC -L	0E	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DADRC -H	0F	'L'	bit14	bit13	bit12	bit11	bit10	bit9	bit8
RMCNDT	10	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HIFCTL	11	CLR BUSY	CLR RSLT	CLR RCDT	RCDT BYTE1	RCDT BYTE0	HINT #2	HINT #1	HINT #0
RESULT	12	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TEST1	13	'L'	'L'	'L'	'L'	'L'	'L'	'L'	'L'
TEST2	14	'L'	'L'	'L'	'L'	'L'	'L'	'L'	'L'
TEST3	15	'L'	'L'	'L'	'L'	'L'	'L'	'L'	'L'
ADPMNT -H	18	'L'	bit14	bit13	bit12	bit11	bit10	bit9	bit8
CI	19	'L'	EMPH ASIS	'L'	BIT L4H8	'L'	FS L3H1	'L'	MONO STE
AUDIO CTL	1A	RTADP CLR	'L'	SM BF2	XATN IF	DAMIX EN	'L'	'L'	'L'

sub CPU Write Registers

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ECCSTS	00	EDC ALL0	ERIN BLK	COR INH	COR DONE	EDC OK	ECC OK	C MODE	C FORM
DECSTS	01	—	—	RTADP BSY	—	—	—	SHRT SCT	NO SYNC
HDRFLG	02	MIN	SEC	BLO CK	MODE	FILE	CHAN NEL	SUB MODE	CI
HDR	03	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SHDR	04	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CMADR -H	05	—	bit14	bit13	bit12	bit11	bit10	bit9	bit8
INTSTS 1	06	—	—	—	—	—	—	RCDT EMPT	RSLT EMPT
INTSTS 2	07	DRV OVRN	DEC TOUT	—	RTADP END	HDMA CMP	DEC INT	HST CMND	HCR ISD
ADPCI	08	—	EMPH ASIS	—	BIT L4H8	—	FS L3H1	—	MONO STE
	09	—	—	—	—	—	—	—	—
HXFRC -L	0A	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HXFRC -H	0B	—	bit14	bit13	bit12	bit11	bit10	bit9	bit8
HADRC -L	0C	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HADRC -H	0D	—	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DADRC -L	0E	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DADRC -H	0F	'H'	bit14	bit13	bit12	bit11	bit10	bit9	bit8
HIFSTS 1	10	—	—	—	—	—	HINT STS2	HINT STS1	HINT STS0
HIFSTS 2	11	BUSY STS	RCDT WRDY	RCDT EMPT	RSLT WRDY	RSLT EMPT	PRM RRDY	DMA BUSY	RINT STS
HSTPRM	12	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HSTCMD	13	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

sub CPU Read Registers

3. Host Registers

3.1. Write Registers

3.1.1. COMMAND Register

Host writes commands to this register. After the host writes a command to this register, interrupt requests to the sub CPU are possible. The control program can use this register as necessary for processing.

3.1.2. PARAMETER Register

Host writes parameters necessary for command execution to this register which is formed by 10 byte of FIFO data.

3.1.3. Write Data (WRDATA) Register

This register used to write data from the host to buffer. Data can be written using the I/O mode or DMAC. This register is formed by 2 bytes of FIFO data.

3.1.4. Host Interrupt Mask (HINTMSK) Register

Setting bits 'H' enable interrupt request from CXD1197AQ to the host according to the bit's corresponding interrupt status. The bits do not effect their corresponding interrupt status.

bit 7 RESERVED
bit 6 ENRINT (Enable remote control interrupt)
bit 5 ENDHUP (Enable DMA hang up interrupt)
bit 4 ENBFWRDY (Enable buffer write ready interrupt)
bit 3 ENBFEMPT (Enable buffer write empty interrupt)
bits 0 to 2 ENINT#0-2 (Enable interrupt#0-2)

3.1.5. Host Clear Interrupt (HCLRINT) Register

Setting bits 'H' clear their corresponding interrupt status and any generated interrupt request to the host. Incidently, when the host reads the RMCNDT register, RINTSTS is cleared.

bits 6 & 7 RESERVED
bit 5 CLRDHUP (Clear DMA hang up interrupt)
bit 4 CLRBFWRDY (Clear buffer write ready interrupt)
bit 3 CLRBFEMPT (Clear buffer write empty interrupt)
bits 0 to 2 CLRINT#0-2 (Clear interrupt#0-2)

3.1.6. Host Chip Control (HCHPCTL) Register

bit 7 BFRD (Buffer read)
Setting to 'H' initiates data transfer from buffer to the host (driver). When data transfer is complete, this bit is automatically reset to 'L'.

bit 6 BFWR (Buffer write)
Setting to 'H' initiates data transfer from host to buffer memory. When data transfer is complete, this bit is automatically reset to 'L'.

bit 5 CHPRST (Chip reset)
Setting to 'H' initializes CXD1197AQ. After initialization is complete, this bit is automatically reset to 'L', eliminating the need to reset by the host.

bit 4 CLRPRM (Clear Parameter)
Setting to 'H' clears the PARAMETER register. After register is cleared, this bit is automatically reset to 'L', eliminating the need to reset by the host.

bit 3 HDRQEN (HDRQ enable)
Setting to 'H' enables the HDRQ pin. After this, setting either the BFRD bit of BFWR bit 'H' activates HDRQ (becomes 'L'). When HDRQ is 'L', the HDRQ pin is normally inactive (high impedance).

3.1.7. ADPCTL (ADPCM control) Register

bit 7 SMEN (Sound map en)
During sound map ADPCM playback, this bit is 'H'.

bit 6 ADPMUTE (ADPCM mute)
During ADPCM decoding when ADPCM audio is muted, this bit is 'H'.

bit 5 SMADPCLR (Sound map ADPCM clear)
When control is passed from the sound map ADPCM decoder, this bit becomes 'H'.

(1) During sound map ADPCM playback (SMEN is 'H' and ADPBSY (HSTS register bit 0) is 'H'), if SMADPCLR is set 'H', the following results:
- The ADPCM decoder is terminated during playback. (Noise may occur.)
- CXD1197AQ's sound map buffer management circuit is cleared. Also, the buffer is emptied. However, the BFEMPT interrupt status is not changed.

Note: At the same time this bit is set 'H', the SMEN bit should be set 'L'.

(2) If SMADPCLR is set 'H' when the sound map ADPCM is not in playback, no action is taken.

bits 0 to 4 RESERVED

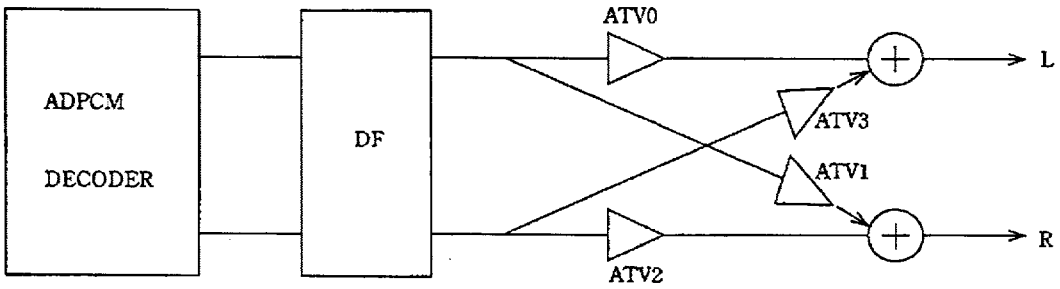
3.1.8. ATV (Attenuation value) Register 0

3.1.9. ATV (Attenuation value) Register 1

3.1.10. ATV (Attenuation value) Register 2

3.1.11. ATV (Attenuation value) Register 3

The attenuation value should be stored in these registers.



3.1.12. CI (Coding information) Register

During sound map playback, this register determines coding information. After bit allocation, this register is the same as the sub Header Coding Information byte.

bits 1, 3, 5, 7 RESERVED

bit 6 EMPHASIS
'H': Emphasis on
'L': Emphasis off

bit 4 BITLENGTH (Bit length)
'H': 8 bits
'L': 4 bits

bit 2 FS (Sampling frequency)
'H': 18.9 KHz
'L': 37.8 KHz

bit 0 M/S (MONO/STEREO)
'H': Stereo
'L': Mono

All write registers are initialized to 00hex upon reset (hardware and software resets).

3.2. Read Registers

3.2.1. RESULT Register

Host outputs results of command executions through this register which is formed by 16 bytes of FIFO data.

3.2.2. Read Data (RDDATA) Register

This register used to read data from the buffer to the host. Data can be read using the I/O mode or DMAC. This register is formed by 2 bytes of FIFO data.

3.2.3. Interrupt Mask Status (INTMSKSTS) Register

Value written to HISTMSK register can be read out of this register.

3.2.4. Host Interrupt Status (HINTSTS) Register

bit 6 RINTSTS (Remote controller interrupt status)
After the sub CPU has written data to the RMCNDT register, this bit becomes 'H'.
After the host has read RMCNDT register, this bit becomes 'L'.

bit 5 DMAHUP (DMA hang up interrupt status)
When ENDHUP is 'H' (HINTMSK register bit 5) and the HDRQ pin is set 'L', if 136μs (68μs for double speed) pass and the XHAC pin is not activated (set 'L'), a DMAHUP state results. In this state data transfers between the host and buffer are terminated. The HDRQ pin becomes inactive (high impedance).

bit 4 BFWRDY (Buffer write ready)

During sound map playback, if one sector or more of writable area is encountered, a BFWRDY state results. Conditions which cause a BFWRDY state are:

(1) Host sets the SMEN bit of ADPCTL register 'H'.

(2) After the host writes 1 sector of sound map data to buffer memory, more than 1 sector of sound map data exists (and buffer is not full).

(3) If enough buffer for sound map data is freed after 1 sector of sound map data is ADPCM decoded.

bit 3 BFEMPT (Buffer Write empty)

If no more sector data is available after 1 sector of data has been ADPCM decoded during sound map playback, a BFEMPT state results.

bits 0 to 2 INSTS#0-2

These bit values are the same as their corresponding bit values in the sub CPU HIFCTL register.

3.2.5. RMCNDT Register

The value of the RMCNDT register, which is written by the sub CPU, can be readout through the RMCNDT register. When the host reads this register the RINTSTS status (INTSTS register bit3) and XRIN pin is cleared.

3.2.6. Host STATUS (HSTS) Register

bit 7 BUSYSTS (Busy status)

After the host writes a command to the command register, this bit becomes 'H'. BUSYSTS is reset 'L' when the sub CPU sets the CLRBUSY bit of the HIFCTL register.

bit 6 DRQSTS (Data request status)

Indicates that a buffer transfer request has been made to the host. During I/O mode data transfer the host should check this bit for 'H' to see if the WRDATA and RDDATA registers are accessed.

bit 5 RSLRRDY (Result read ready)

If 'H', the result register is not empty and can be read by the host.

bit 4 PRMWRDY (Parameter write ready)

If 'H', the parameter register is not full and can be written by the host.

bit 3 PRMEMPT (Parameter empty)

If 'H', the parameter register is empty.

bits 1, 2 RCDTBYTE0 & 1 (RMCNDT BYTE0 & 1)

Indicates the number of remote controller bytes (RMCNDT register) that have been sent from the sub CPU.

RCDTBYTE1	RCDTBYTE0	Byte Count
'L'	'L'	Prohibited
'L'	'H'	1
'H'	'L'	2
'H'	'H'	3

bit 0 ADPBUSY (ADPCM busy)

'H' when the ADPCM decoder is processing.

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
COMM AND	0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PARA METER	1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WR DAT A	2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HINT MSK	3	'L'	EN RINT	EN DHUP	ENBF WRDY	ENBF EMPT	EN INT2	EN INT1	EN INT0
HCLR INT	4	'L'	'L'	CLR DHUP	CLR WRDY	CLR EMPT	CLR INT2	CLR INT1	CLR INT0
HCHP CTL	5	BFRD	BFWR	CHP RST	CLR PRM	HDRQ EN	'L'	'L'	'L'
RESER VED	6	'L'	'L'	'L'	'L'	'L'	'L'	'L'	'L'
ADP CTL	7	SMEN	ADP MUTE	SMADP CLR	'L'	'L'	'L'	'L'	DIS ATT EN
ATV0	8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATV1	9	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATV2	A	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATV3	B	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CI	C	'L'	EMPH ASIS	'L'	BIT L4H8	'L'	FS L3H1	'L'	S/M
RESER VED	D~F	'L'	'L'	'L'	'L'	'L'	'L'	'L'	'L'

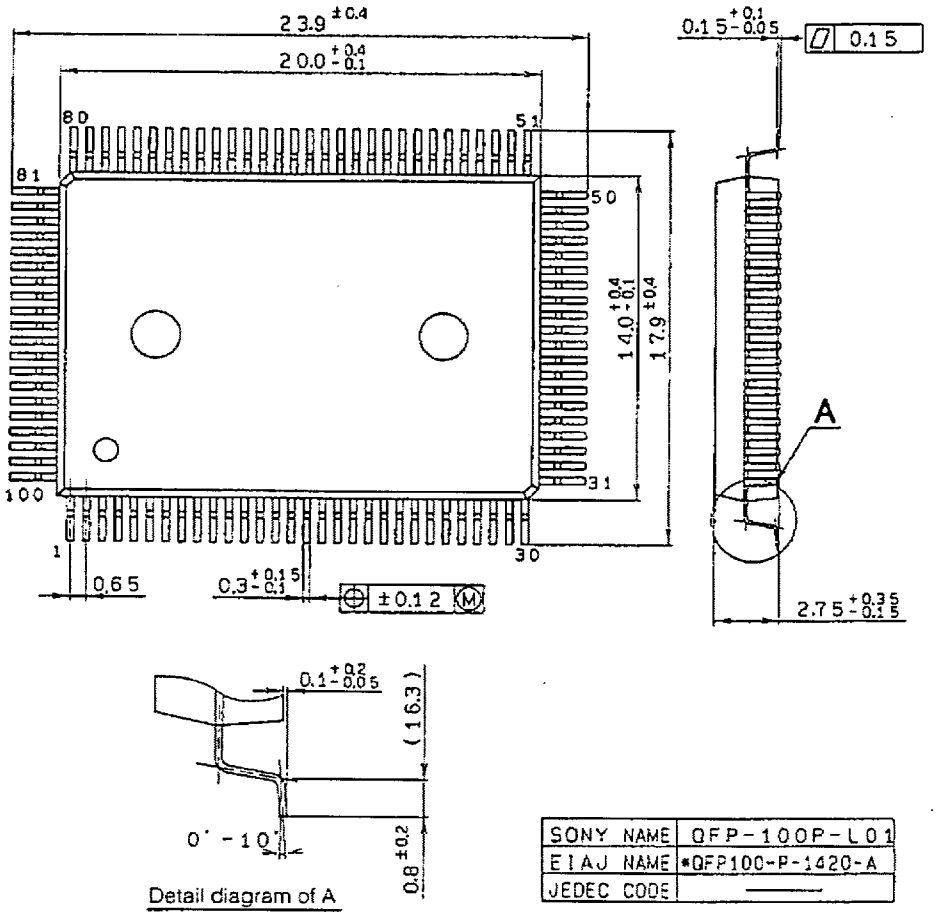
Host Write Registers

REG	ADR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	0	—	—	—	—	—	—	—	—
RE S U LT	1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RD DAT A	2	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
INTMSK S T S	3	'L'	EN RINT	EN DHUP	ENBF WRDY	ENBF EMPT	EN INT2	EN INT1	EN INT0
	4	—	—	—	—	—	—	—	—
HINT STS	5	—	RINT	DHUP	BF WRDY	BF EMPT	INT2	INT1	INT0
HSTS	6	BUSY STS	DRQ STS	RSL RRDY	PRM WRDY	PRM EMPT	RCDT BYTE1	RCDT BYTE0	ADP BUSY
	7	—	—	—	—	—	—	—	—
	8	—	—	—	—	—	—	—	—
	A	—	—	—	—	—	—	—	—
	B	—	—	—	—	—	—	—	—
	C	—	—	—	—	—	—	—	—
RMCN DT	D	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	E,F	—	—	—	—	—	—	—	—

Host Read Registers

Package Outlime Unit : mm

100pin QFP (Plastic)



SONY NAME	QFP-100P-L01
EIAJ NAME	*QFP100-P-1420-A
JEDEC CODE	———