Version :0.3

TECHNICAL SPECIFICATION

MODEL NO. : PD024OX4

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Confirmed By _____

Prepared By _____

FOR MORE INFORMATION:
AZ DISPLAYS, INC.
75 COLUMBIA, ALISO VIEJO, CA, 92656
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Date : Jun. 15, 2005

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TECHNICAL SPECIFICATION

CONTENTS

1. Application

This technical specification applies to a 2.36” color TFT-LCD panel.
This is designed for printer application and other electronic products which require high quality flat panel display.

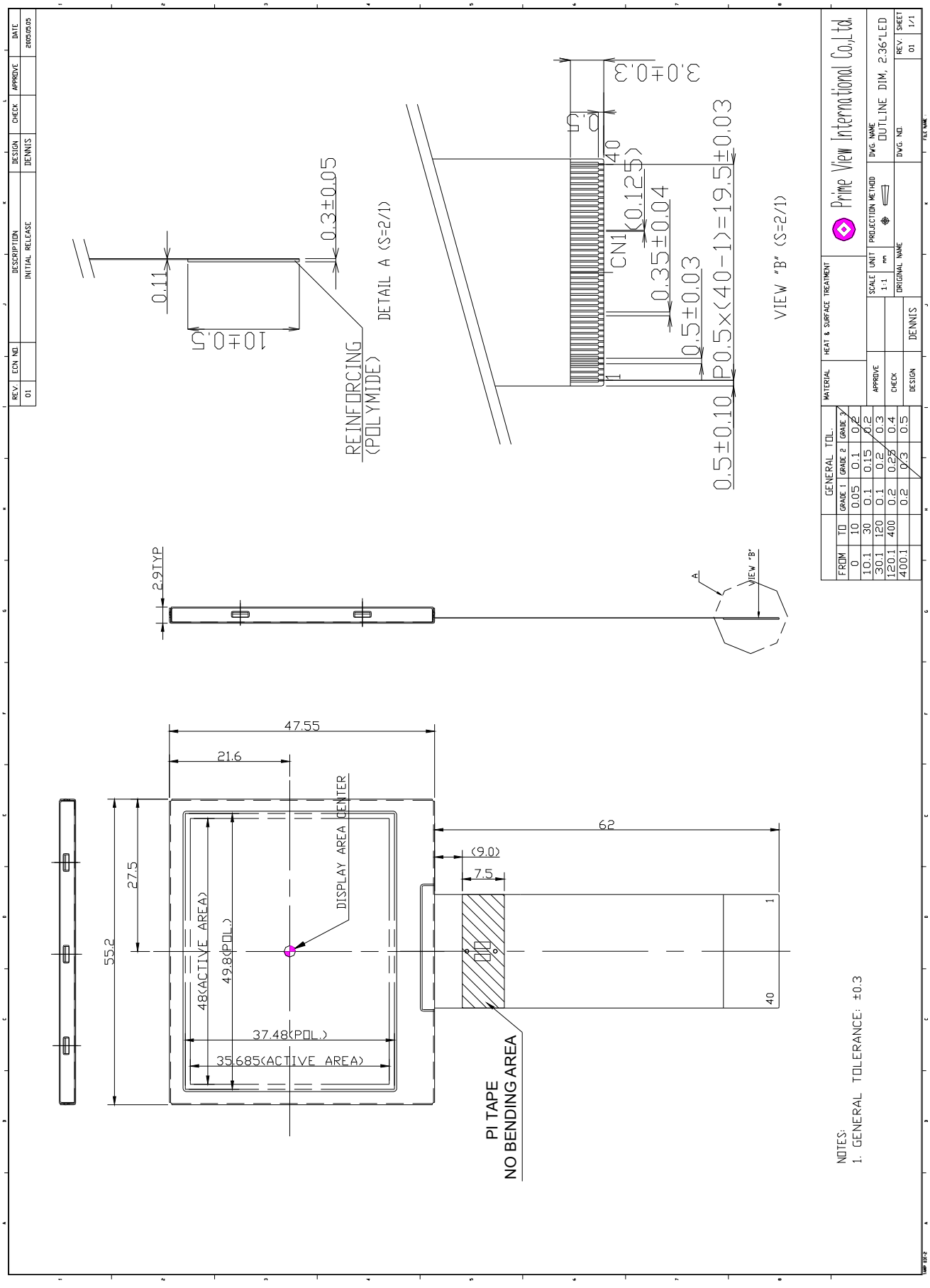
2. Features

. Pixel in delta configuration
. Enables an approximately 16,190,000 color display by pseudo 8-bit function.
. Provide a 3-wire clock synchronous serial interface for various operation mode settings.
. Built-in TCON corresponding to the image interface of the RGB form.
. Built-in gate driver interface circuit .
. Image reversion : Up/Down and Left/Right.
. Built-in control circuit for LED driving.
. Built-in power-save functions such as the stand-by mode.
. Built-in power-on reset signal generation circuit.
. Built-in Vcom amplitude voltage output circuit.

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	2.36	inch
Display Format	160 (RGB)×234	dot
Active Area	48.0(H)×35.685(V)	mm
Dot Pitch	0.1(H)×0.1525 (V)	mm
Pixel Configuration	Delta	
Outline Dimension	55.2(H)×47.55 (V) ×2.9(D)(typ.)	mm
Viewing direction	6 o’clock	
Surface Treatment	Anti – Glare	
Weight	15±1.5	g

4. Mechanical Drawing of TFT-LCD Module



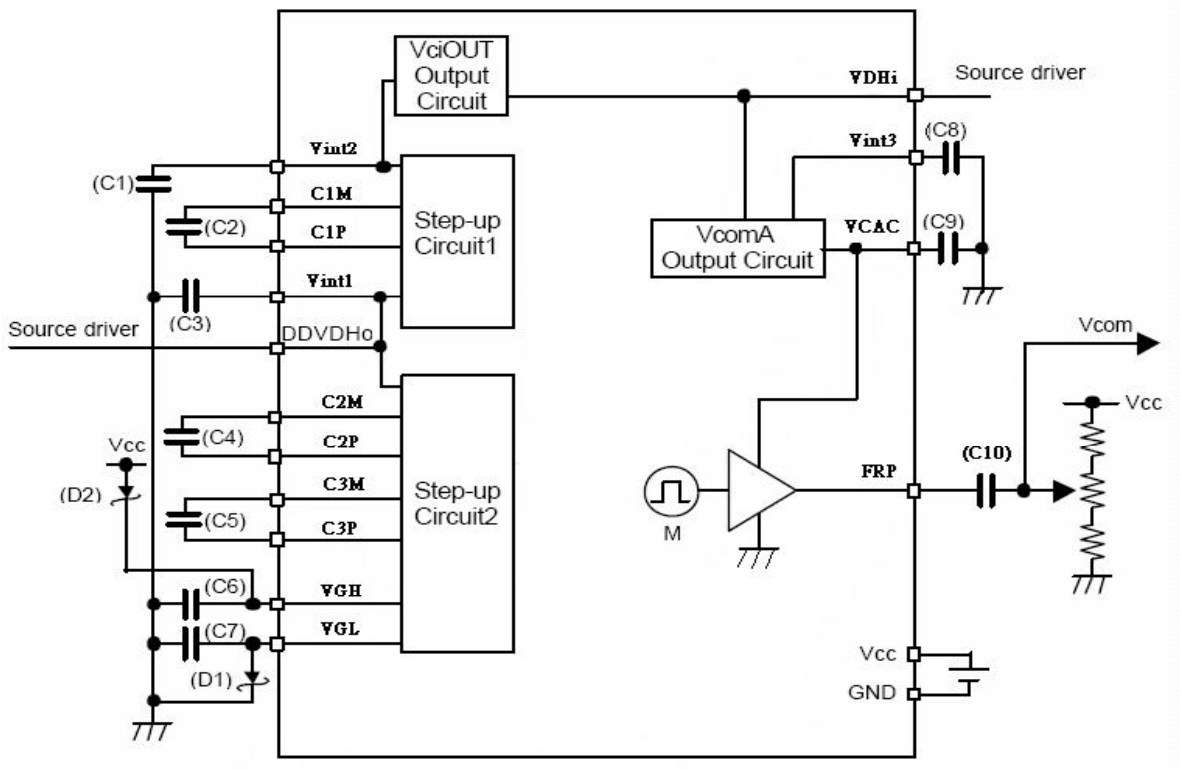
5. Input / Output Terminals

FPC Down Connect , 30Pins , Pitch : 0.5 mm PGND=GND=0V

Pin No	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode voltage	Note 5-1
2	N/C	-	-	
3	VGL		Negative power supply for gate driver	Note 5-2
4	C4P	C	Pins to connect capacitance for power circuitry	
5	C4M	C	Pins to connect capacitance for power circuitry	
6	VGH		Positive power supply for gate driver	
7	FRP	O	Frame polarity output for VCOM	
8	VCAC	C	Define the amplitude of the VCOM swing	
9	Vint3	I	Intermediate voltage for charge Pump	
10	C3P	C	Pins to connect capacitance for power circuitry	
11	C3M	C	Pins to connect capacitance for power circuitry	
12	Vint2	I	Intermediate voltage for charge Pump	
13	C2P	C	Pins to connect capacitance for power circuitry	
14	C2M	C	Pins to connect capacitance for power circuitry	
15	Vint1	I	Intermediate voltage for charge Pump	
16	C1P	C	Pins to connect capacitance for power circuitry	
17	C1M	C	Pins to connect capacitance for power circuitry	
18	PGND	I	Charge Pump Power GND	
19	PVDD	I	Charge Pump Power VDD	Note 5-3
20	DRV	O	Gate signal for the power transistor of the boost converter	Note 5-4
21	VLED	I	Supply voltage for LED backlight	
22	NC	-	Ground for LED backlight	
23	FB	I	Main boost regulator feedback input	Note 5-5
24	VCC	I	Digital power supply	Note 5-3
25	GND	I	Digital GND	
26	VCC	I	Digital power supply	Note 5-3
27	CS	I	Serial interface chip select signal	
28	SDA	I	Serial interface data input signal	
29	SCL	I	Serial interface transmission clock	
30	HSYNC	I	Horizontal sync input	Note 5-6
31	VSYNC	I	Vertical sync input	Note 5-7
32	DCLK	I	Clock input	Note 5-8
33	D7	I	Data input	Note 5-9
34	D6	I	Data input	
35	D5	I	Data input	
36	D4	I	Data input	
37	D3	I	Data input	
38	D2	I	Data input	
39	D1	I	Data input	
40	D0	I	Data input	

Note 5-1:V_{COM} = +5.0 Vp-p. (Typ.)
Note 5-2: This is generated by the Step-up Circuit 1 and 2 , The external capacitor is required On those pins as following.

Capacitor	Capacity and Applied voltage	Recommended Breakdown	Remark
(C1)Vint2	1uF/Vint2	6V	
(C2)C1P/M	1uF/Vint2	6V ~ 10V	
(C3)Vint1	1uF/Vint1	10V	
(C4)C2P/M	1uF/Vint1	10V ~ 16V	
(C5)C3P/M	1uF/Vint1	10V ~ 25V	
(C6)VGH	1uF/VGH	25V	
(C7)VGL	1uF/VGL	25V	
(C8)Vint3	1uF/Vint3	10V	
(C9)VCAC	1uF/VCAC	10V	
(C10) FRP	1uF/FRP	10V	

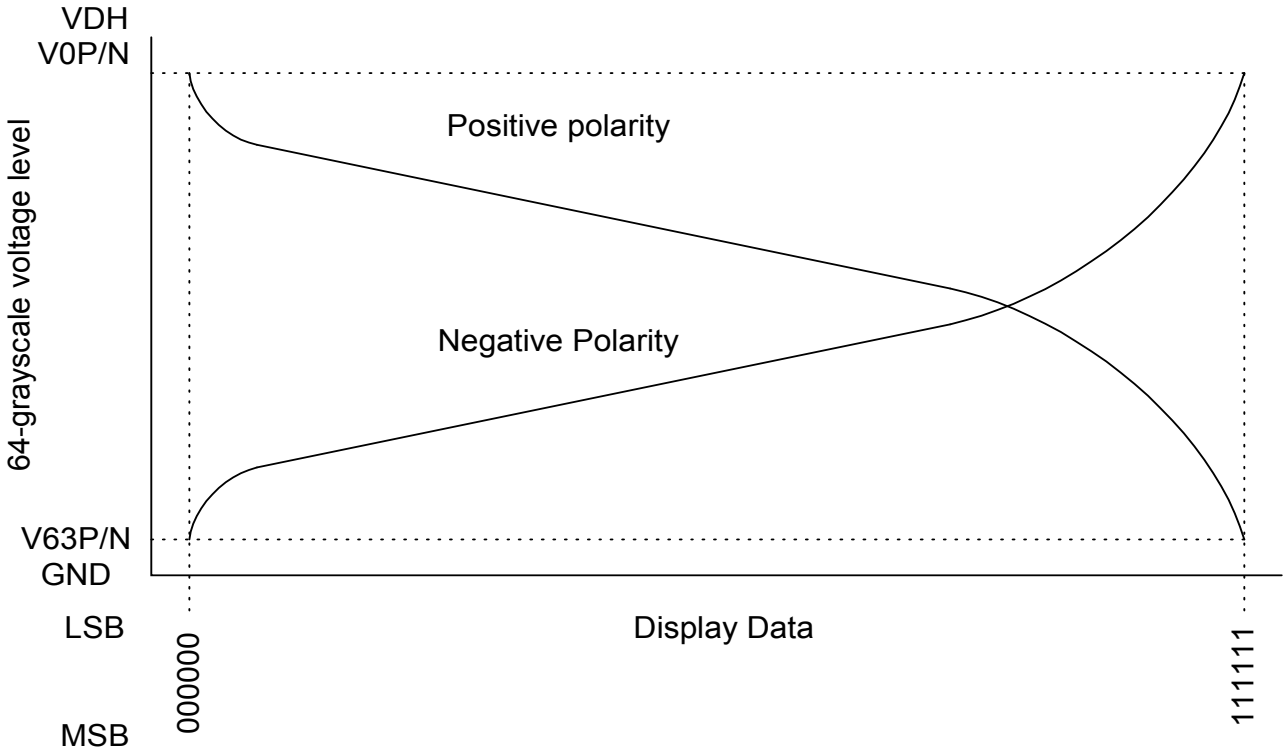


The values of wiring resistance at pins(The wiring resistance to parts to be connected).
(1) VCC, GND, C1P, C1M, Vint1, must be < 3ohm.
(2) C2P, C2M, C3P, C3M, Vint2, Vint3, VCAC, FRP, VGH, VGL, DDVDHo Must be < 5ohm.
(3) VDHi must be < 30ohm.

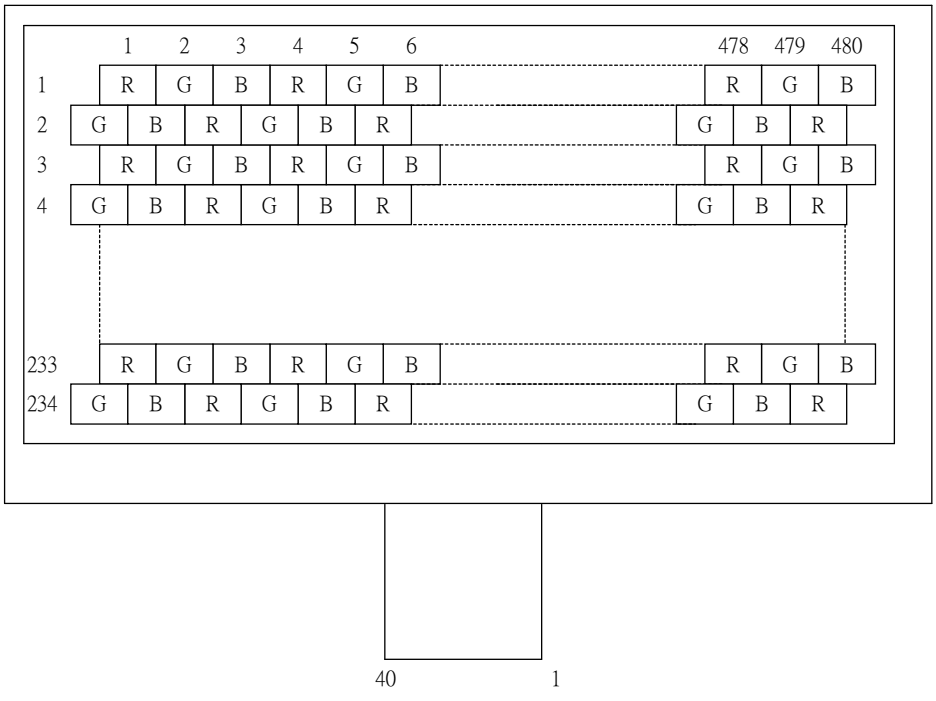
Note 5-3: PVDD, VCC = +3.3 V (Typ.)
Note 5-4: Outputs the control signal of switching regulator for LED. Duty cycle varies according to FB input voltage.

Note 5-5: Feedback signal of switching signal for LED. It controls DRV output duty cycle with 0.6V input level sense.

Note 5-7: Horizontal sync signal, it is a “Low” active signal
Note 5-8: Vertical sync signal, it is a “Low” active signal.
Note 5-9: Dot clock signal for RGB interface, timing for data loading defined at rising edge.
Note 5-10: 6-bit interface(When pseudo 8-bit function operation is off)☹D0~1 no use).
8-bit interface(When pseudo 8-bit function operation is on)D0~7.
＊R01h control pseudo 8-bit mode on/off.



6. Pixel arrangement and input pin connector No.



7. Internal Register Description and Timing Characteristics

7-1 List of register instructions

Register No.	Address			Data												
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	0	0	0	-	-	-	-	-	-	-	-	SORST	STB	LEDON	DCON
R01h	0	0	1	0	0	0	0	-	-	-	-	-	-	EDZ	-	-
R02h	0	1	0	0	-	-	-	-	-	-	-	-	MPOL	-	UD	RL
R03h	0	1	1	0	-	-	-	-	-	-	-	-	-	-	-	-
R04h	1	0	0	0	0	0	0	-	-	-	-	HBP4	HBP3	HBP2	HBP1	-
R05h	1	0	1	0	-	-	-	-	-	-	-	-	VBP3	-	VBP1	VBP0
R06h	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-
R07h	1	1	1	0	-	-	-	-	-	-	-	-	-	-	-	-

" – " means don't care

7-2 Register function description

∗ **R00h (system control)**

Register No.	Address			Data												
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	0	0	0	-	-	-	-	-	-	-	-	SORST	STB	LEDON	DCON
Default													1	1	0	1

SORST: Used for system reset. System reset starts when SORST ="0", and all instruction setting to default .

STB: The standby mode turned on when STB ="0", Display operation is off in standby mode.

LEDON: This controls the on/off of the DRV signal for LED BL, the DRV output level becomes GND when LEDON ="0".

DCON: This controls the generator start/stop of the step-up clock DCCLK. The DCCLK generator starts when DCON ="0".

∗ **R01h (Data control)**

Register No.	Address			Data												
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R01h	0	0	1	0	0	0	0	-	-	-	-	-	-	EDZ	-	-
Default														0		

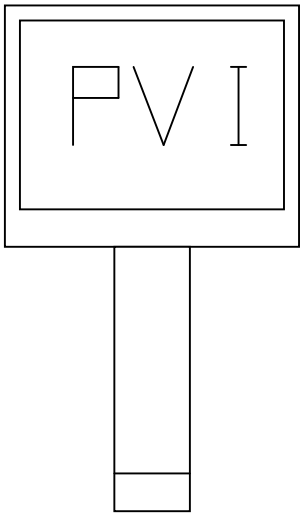
EDZ: When EDZ =”0”, pseudo 8-bit is implemented.
Data input pin D0 and D1 must fixed to GND or VCC level when EDZ =”1”.

∗ **R02h (Data control)**

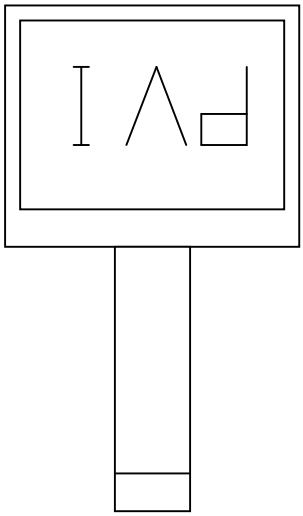
Register No.	Address			Data												
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R02h	0	1	0	0	-	-	-	-	-	-	-	-	MPOL	-	UD	RL
Default													0		1	1

MPOL: Reverse the polarity of FRP output when MPOL = “1”.

U/D = 1, R/L = 1



U/D = 0, R/L = 0



∗ **R04h (Timing control)**

Register No.	Address			Data											
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R04h	1	0	0	0	0	0	0	-	-	-	-	HBP4	HBP3	HBP2	HBP1	-
Default												0	0	0	0	

HBP4	HBP3	HBP2	HBP1	Horizontal back porch(Thb)
0	0	0	0	100DCLK
0	0	0	1	102DCLK
0	0	1	0	104DCLK
0	0	1	1	106DCLK
0	1	0	0	108DCLK
0	1	0	1	110DCLK
0	1	1	0	112DCLK
0	1	1	1	114DCLK
1	0	0	0	97DCLK
1	0	0	1	95DCLK
1	0	1	0	93DCLK
1	0	1	1	91DCLK
1	1	0	0	89DCLK
1	1	0	1	87DCLK
1	1	1	0	85DCLK
1	1	1	1	83DCLK

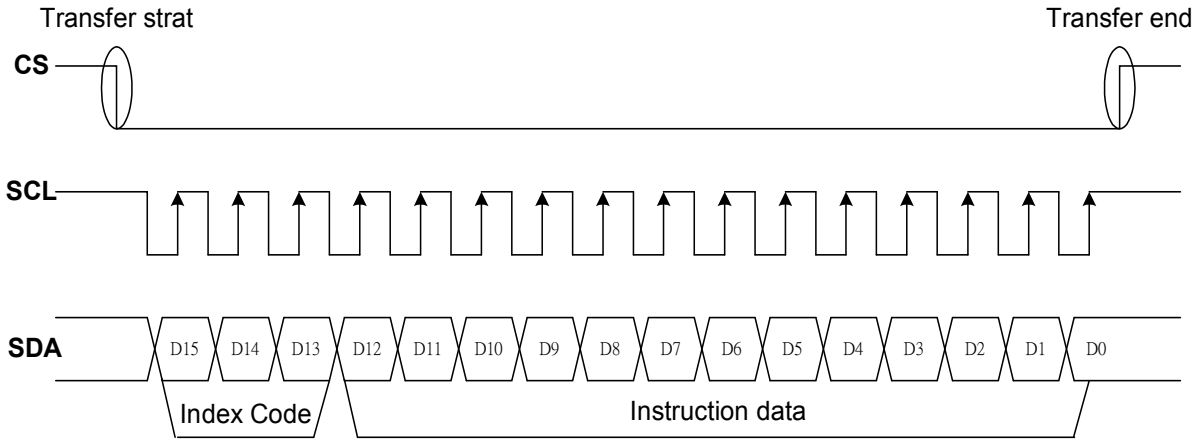
∗ **R05h (Data control)**

Register No.	Address			Data												
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R05h	1	0	1	0	-	-	-	-	-	-	-	-	VBP3	-	VBP1	VBP0
Default													0	-	0	0

VBP3	VBP1	VBP0	Vertical back porch(Tvb)
0	0	0	16 HSYNC
0	0	1	17 HSYNC
0	1	0	18 HSYNC
0	1	1	19 HSYNC
1	0	0	8 HSYNC
1	0	1	7 HSYNC
1	1	0	6 HSYNC
1	1	1	5 HSYNC

7-3 Timing characters of serial interface

Data loaded starting from the falling edge of CS input, ends at the rising edge. Data is on a 16bits basis. If an SCL of 16bits or more is not inputted during the CS "Low period", transmitted data becomes invalid, as the data is not loaded inside.
The register setting value after the data transmission is available in the next frame(after VSYNC input).



8. Absolute Maximum Ratings

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

PGND=GND=0V , Ta = 25℃

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Power Supply Voltage	Vcc	-0.3	4	V	
	PVDD	-0.3	4.6	V	
Input Signal Voltage	Vcom	-0.5	5.2	V	
Digital Input Voltage	V_{IN}	-0.3	Vcc+0.3	V	
Storage Temperature	T_{ST}	-20	70	°C	
Operation Temperature	T_{OP}	0	60	°C	
Maximum clock frequency	Fmax		12	MHz	

9. Electrical Characteristics

9-1 Operation condition

PGND=GND=0V , Ta = 25℃

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver		Vcc	3.0	3.3	3.6	V	
Supply Voltage for Gate Driver		PVDD	3.0	3.3	3.6		
	H level	V_{GH}	14.5	16.5	17.5	V	Note 9-1
	L level	V_{GL}	-12	-10	-9.4	V	Note 9-1
Digital input voltage	H level	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	L level	V_{IL}	0	-	0.3 V_{CC}	V	
Digital output voltage	H level	V_{OH}	0.7 V_{CC}	-	V_{CC}	V	
	L level	V_{OL}	0	-	0.3 V_{CC}	V	
V_{COM}		$V_{COM\ AC}$	-	+5.0	-	V_{P-P}	AC Component of V_{COM}
		$V_{COM\ DC}$	-	1.4	-	V	Note 9-2

Note 9-1: V_{GH} and V_{GL} supplied by internal setup-up circuit.

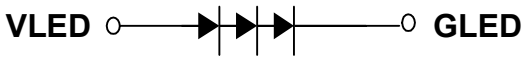
Note 9-2: PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 1.4V±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

9-2 Power consumption

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V_{LED}	9.0	10.0	11.5	V	I_L = 20 mA
Supply current of LED backlight	I_{LED}		20		mA	Note 9-3
Backlight Power Consumption	P_{LED}	180	200	230	mW	Note 9-4

Note 9-3: LED B/L applied information, please refer to the appendix at the end .

Note 9-4: $P_{LED} = V_{LED} * I_{LED}$.



Parameter	Symbol	Conditions	TYP.	MAX.	Unit	Remark
Supply current for source driver	ICC	VCC =+3.3V	6.0	8.0	mA	
Supply current for gate driver	PVDD	PVDD1=+3.3V	9.0	12.0	mA	
Total power consumption			49.5	66.0	W	

9-3 Timing characteristics of input signals

(1) Horizontal timing

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock cycle time	Trate	83.3	100	-	ns	
Clock low level pulse width	Tcwl	15	-	-	ns	
Clock high level pulse width	Tcwh	15	-	-	ns	
Data setup	Tds	12	-	-	ns	
Data hold	Tdh	12	-	-	ns	
HSYNC period	Th	-	63.5	-	us	
		-	635	-	CLK	
H front porch	Thf	5	5	-	CLK	
HSYNC low level pulse width	Thp	4	44	-	CLK	
H back porch	Thb	83	100	114	CLK	
DCLK setup	Tdcs	12	-	-	ns	
DCLK hold	Tdch	12	-	-	ns	
H valid display period	Thd	-	480	-	CLK	

(2) Vertical timing

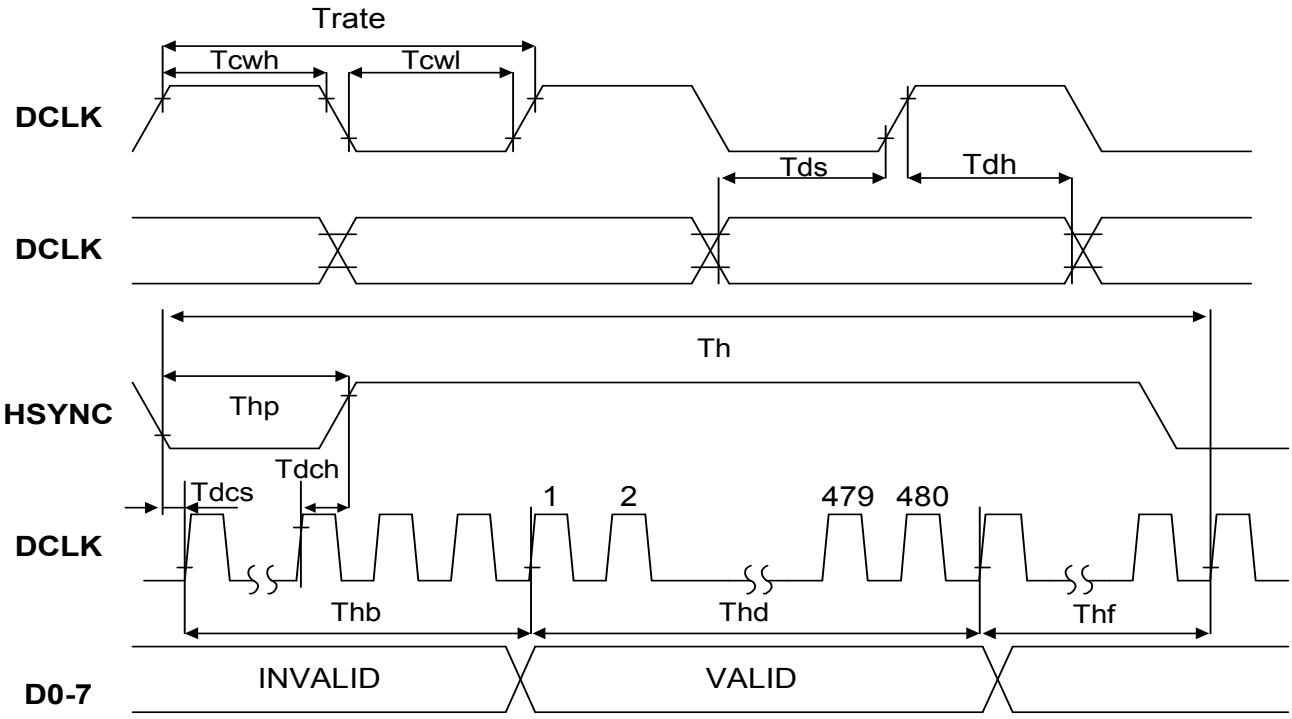
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
VSYNC period	Tv	-	16.67	-	ms	
		-	262	-	HSYNC	
V valid display period	Tvd	-	240	-	HSYNC	
V front porch	Tvf	6	-	-	HSYNC	
VSYNC low level pulse width	Tvp	-	9	-	HSYNC	
V back porch	Tvb	5	16	19	HSYNC	

(3) Serial interface timing

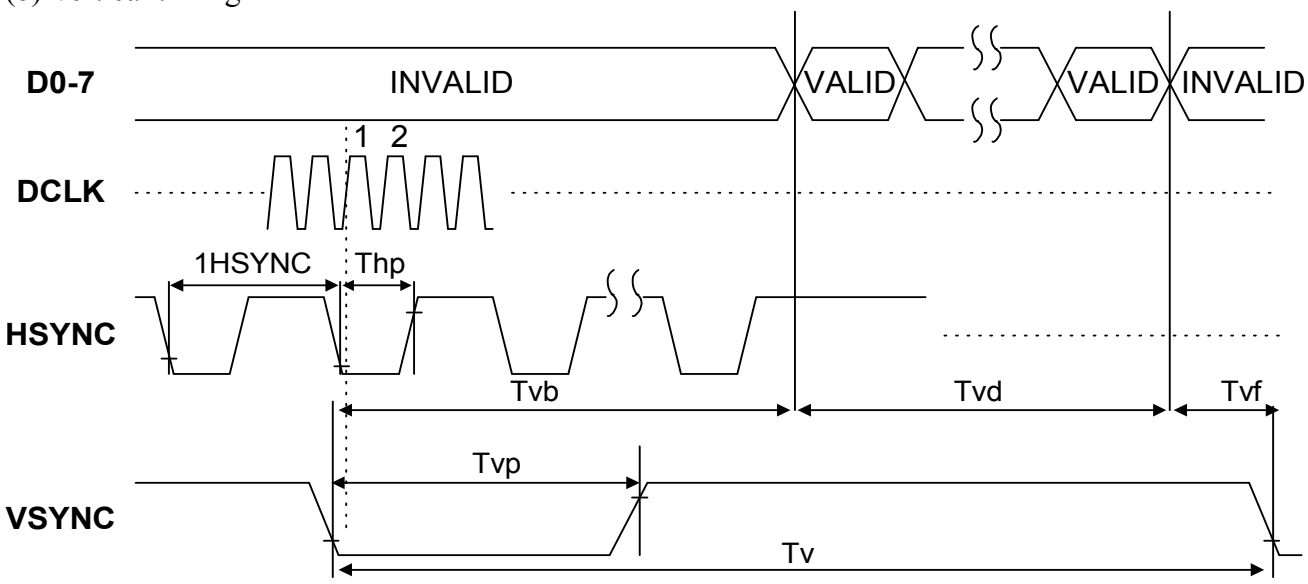
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock cycle time	Tcycs	320	-	-	ns	
Clock low level pulse width	Tscwl	120	-	-	ns	
Clock high level pulse width	Tscwh	120	-	-	ns	
Data setup	Tsds	120	-	-	ns	
Data hold	Tsdh	120	-	-	ns	
Chip select setup	Tcss	120	-	-	ns	
Chip select hold	Tcsh	120	-	-	ns	

9-4 Timing Chart

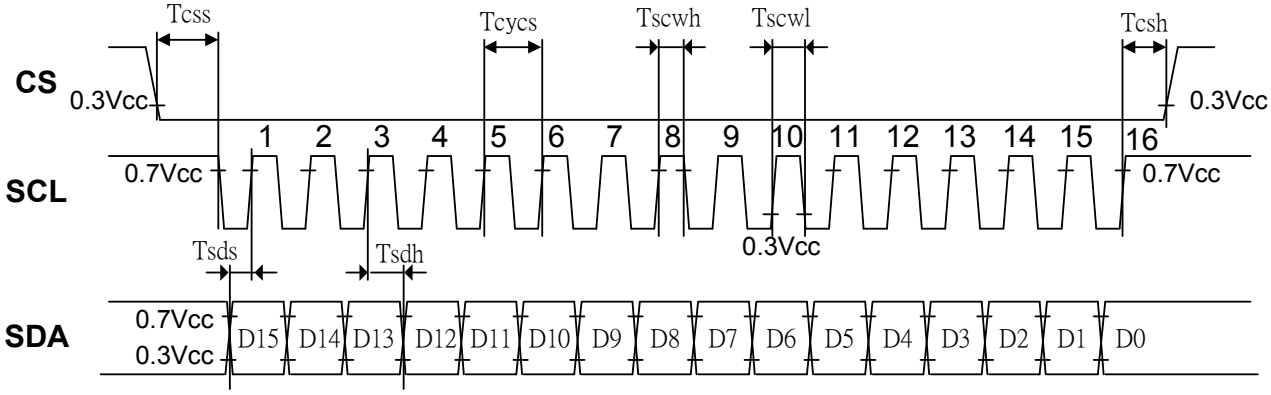
(a) Horizontal timing



(b) Vertical timing



(c) Serial interface



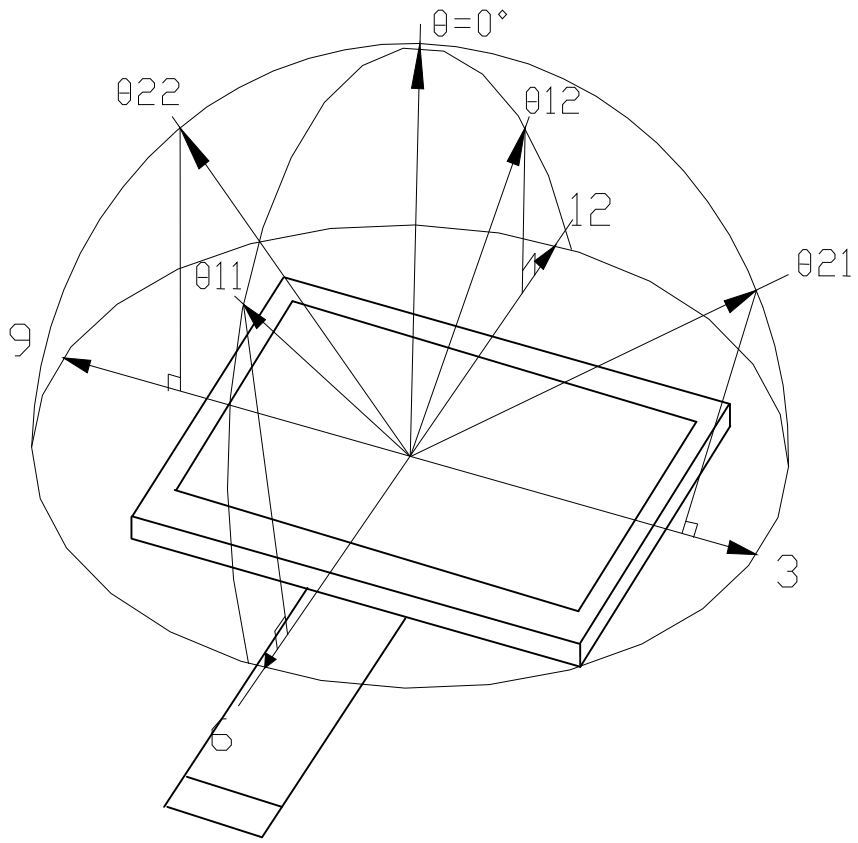
10. Optical Characteristics

10-1 Specification

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ21, θ22	CR≧10	45	50	---	deg	Note 10-1
	Vertical	θ11		30	35	---	deg	
		θ12		10	15	---	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	400	---		Note 10-2
Response time	Rise	Tr	θ=0°	---	6	12	ms	Note 10-3
	Fall	Tf		---	15	30	ms	
Uniformity		U		70	75		%	Note 10-4
Brightness		L		200	250		cd/㎡	Note 10-5
White Chromaticity		X	θ=0°		0.31			Note 10-5
		y	θ=0°		0.33			
LED Life Time					10000		hrs	Note10-6

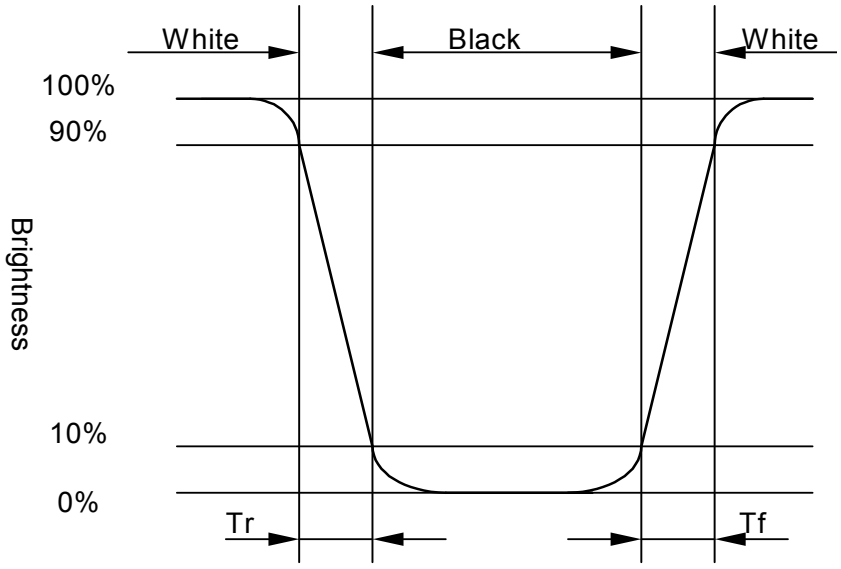
Note 10-1 : The definitions of viewing angles



Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

Contrast ratio is measured in optimum common electrode voltage.

Note 10-3 : The definition of response time :

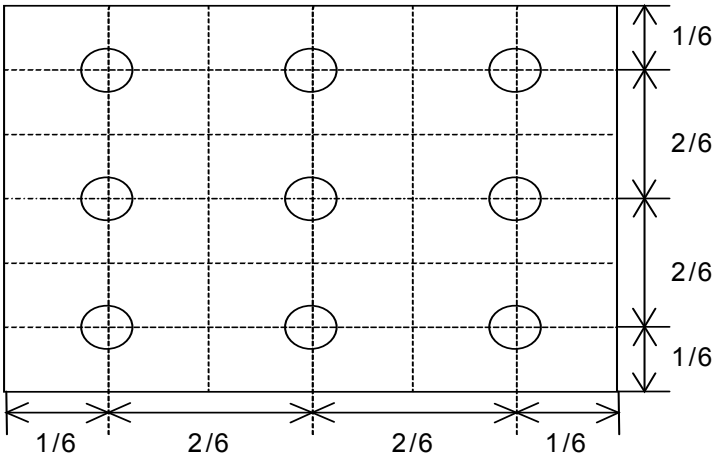


Note 10-4 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

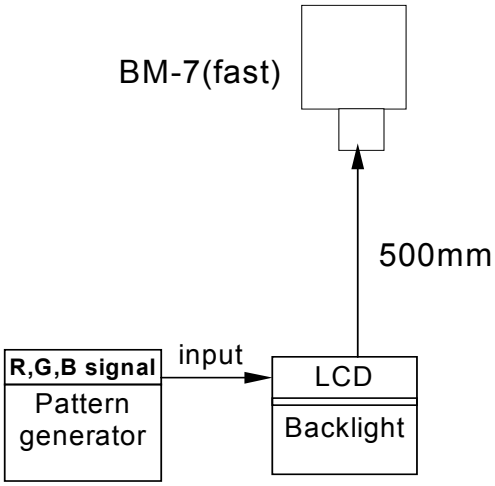
The test pattern is white



Note 10-5 : Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (use PVI backlight after 5 minutes operating , ILED = 20mA.

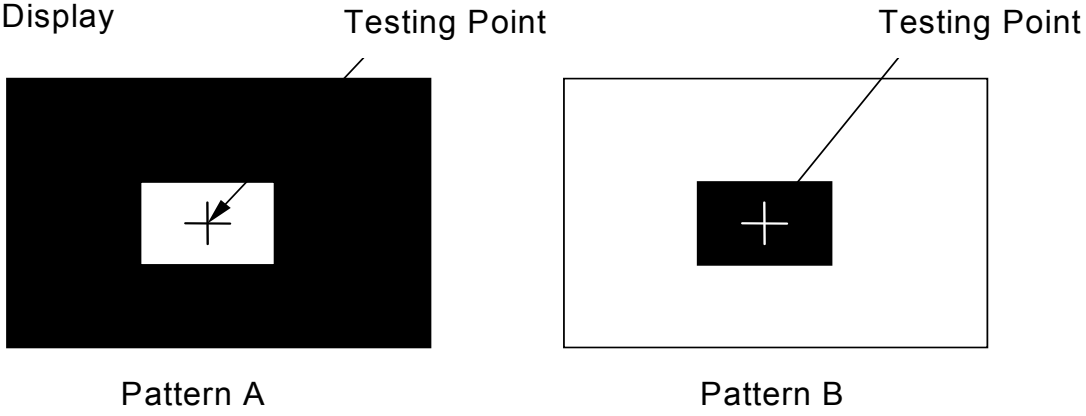
Note 10-6 : Constant current 20mA for each loop , and the center brightness must more than 50% of initial brightness value .

10-2 Testing configuration

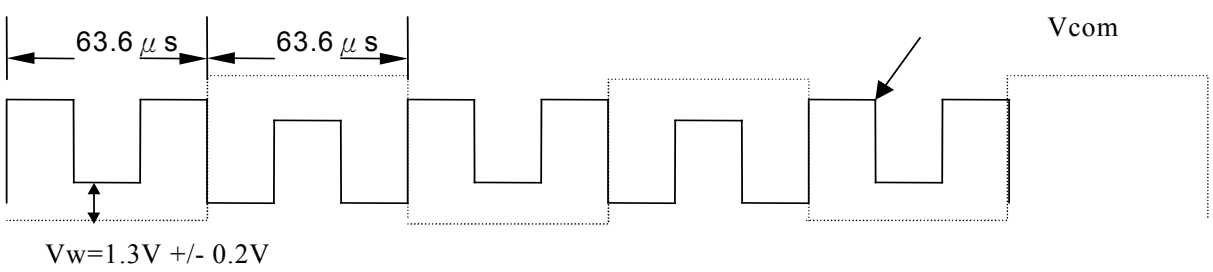


Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

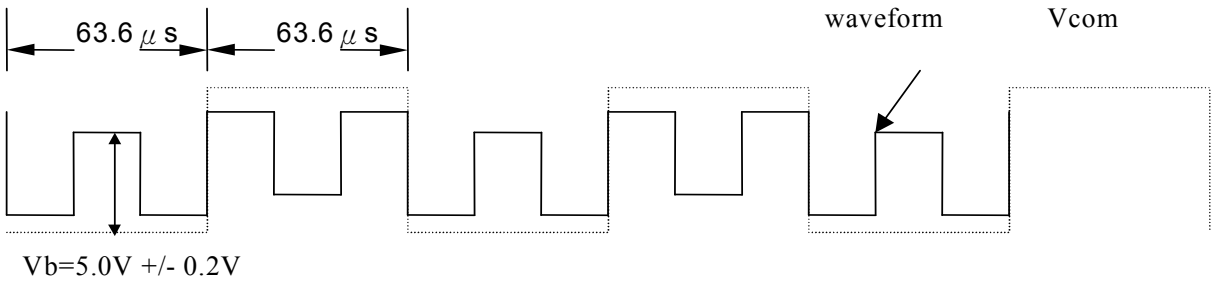
- LCD Display



- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



11. Handling Cautions

11-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground surely. If the connection is not perfect, some following problems may happen possibly.
1.The noise from the backlight unit will increase.
2.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

12. Reliability Test

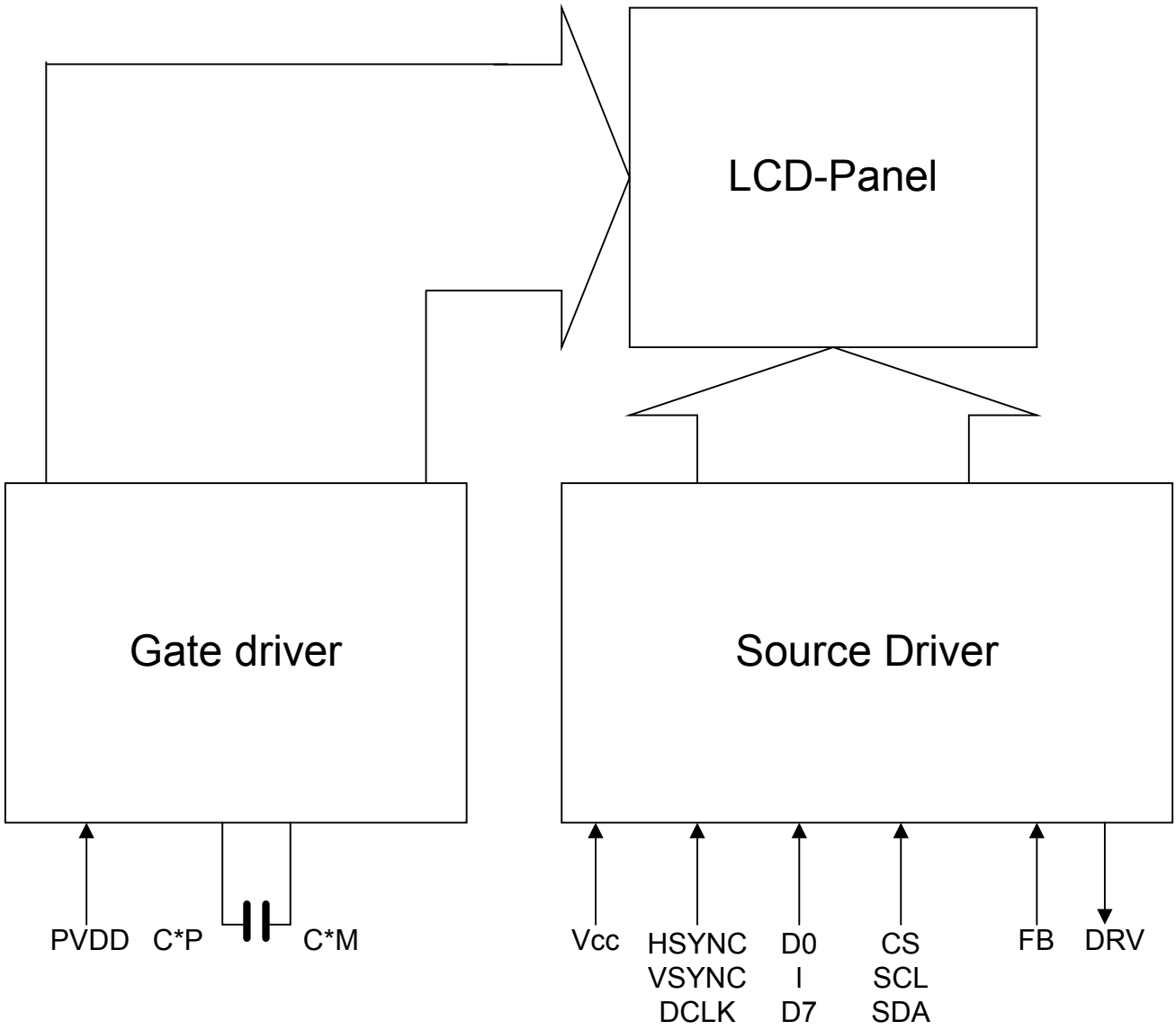
No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70℃ , 240 hrs
2	Low Temperature Storage Test	Ta = -20℃ , 240 hrs
3	Low Temperature Operation Test	Ta = 0℃ , 240 hrs
4	High Temperature & High Humidity Operation Test	Ta = +60℃ , 90%RH , 240 hrs
5	Thermal Cycling Test (non-operating)	-20℃ → +70℃, 200 Cycles 30 min 30 min
6	Vibration Test (non-operating)	Frequency : 10 ~ 55 H_Z Amplitude : 1.0 mm Sweep time : 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
7	Shock Test (non-operating)	100G , 6ms Direction : ±X , ±Y , ±Z Cycle : 3 times
8	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

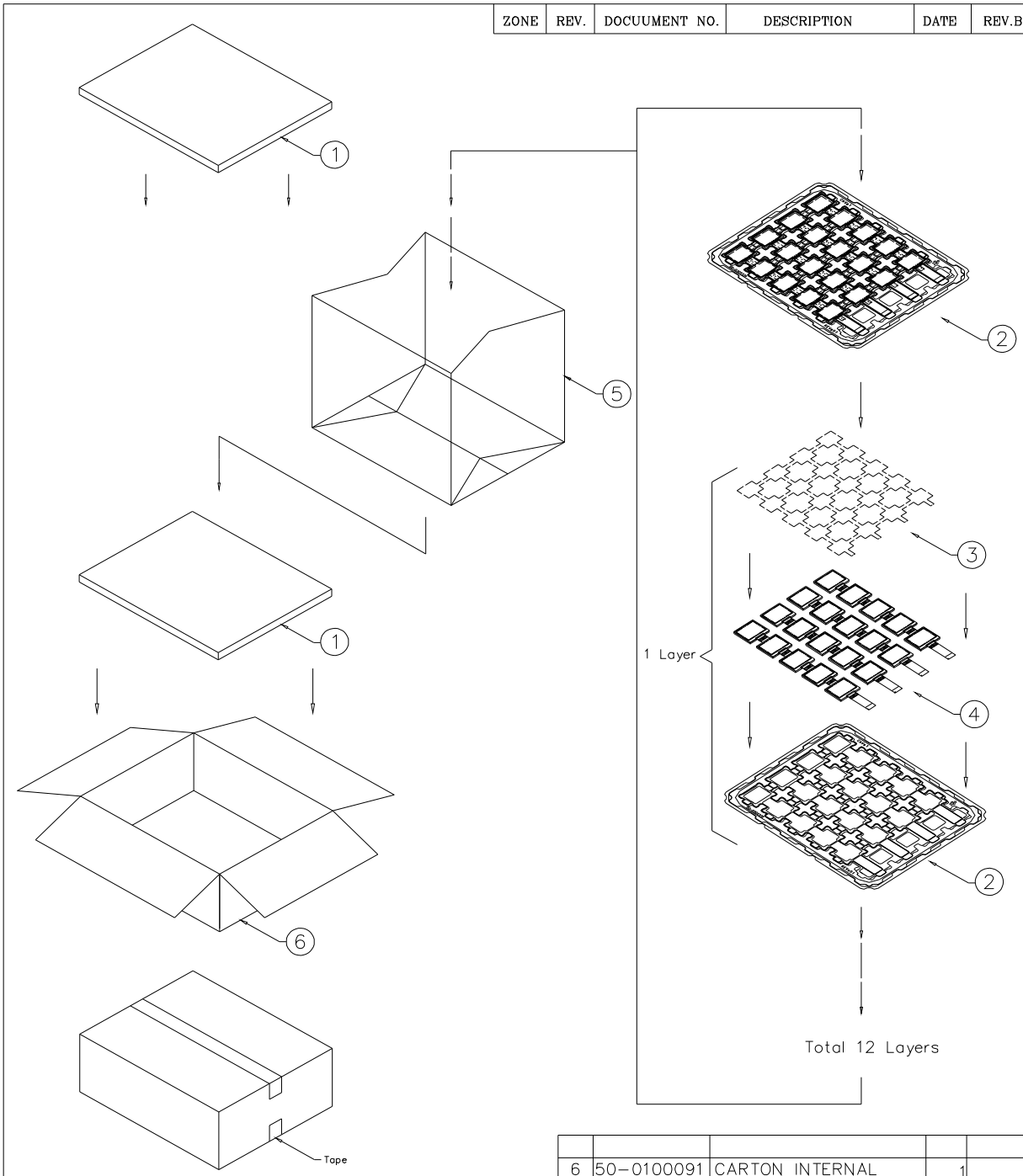
[Criteria]
Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

13. Block Diagram



14. Packing

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:

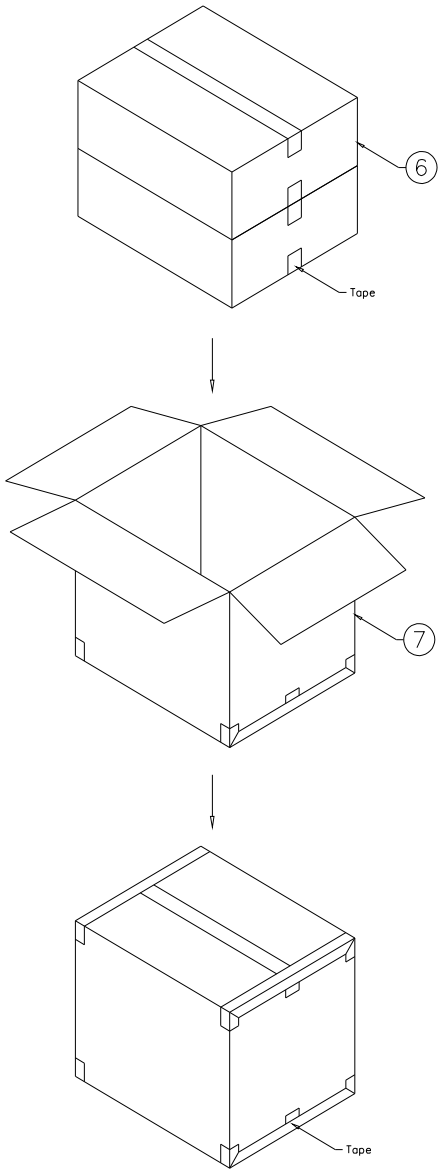
1. One layer include: 1 piece of cushion sheet, 20pcs panel & 1 piece of tray.
2. Q'TY: 220 pcs panel/carton.
3. Dimension: 455*375*190mm
4. Weight: 6.0 KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PD024OX4	220	
3	50-0200071	EPE CUSHION SHEET	11	抗靜電
2	50-0301331	TRAY	12	抗靜電
1	50-0300491	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View Internation Co.,ltd.

			SCALE	UNIT	SHEET	DWG.TITLE	
APPROVE		. .	1:1	mm	1 OF 2	PD024OX4 PACKING Dim	
CHECK		. .					
DESIGN	Dennis	'05.05.19	MTL.NO.		DWG.NO.	REV. 01	A4 SIZE

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:

1.Q'TY: 440 pcs panel/carton.
2.Dimension: 480*396*405mm
3.Weight: 13 KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
7	50-0100101	CARTON EXTERNAL	1	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View Internation Co.,ltd.

			SCALE	UNIT	SHEET	DWG.TITLE
APPROVE		. .	1:1	mm	2 OF 2	PD024OX4 PACKING Dim
CHECK		. .				
DESIGN	Dennis	'05.05.19	MTL.NO.		DWG.NO.	REV. 01 / A4 SIZE

Revision History

Rev.	Issued Date	Revised Contents
0.1	Jan. 03, 2005	Preliminary
0.2	May. 15, 2005	Modify Page 10: R05h (VBP2 is fixed to high). Page 13: VSY change to Typ. 60Hz, and others relative parameters.
0.3	Jun. 15, 2005	Modify Page 03: Weight tolerance change to 15±1.5g. Page 06: Value of C1 P/M, C2 P/M, C3 P/M. Page 12: Add LED B/L power consumption. Page 15: Change Tr Typ. to 6ms; Tf Typ. to 15ms. Page 21: Add packing drawing.

