

DESCRIPTION

The LX13088A is a highly integrated dual output voltage regulator ideal for low power applications that require minimal board space. The two current mode buck converters include integrated high side control switches, synchronous rectifiers, and internal compensation. The outputs of each converter are both rated for up to 1A, and the output voltages are adjustable using external resistive dividers.

The LX13088A step down converters operate at 1.3MHz fixed switching frequency under normal load, reducing external output filter component values and size. Under light load conditions, the converters operate in a pulse-skipping mode for improved efficiency.

The LX13088A incorporates out of phase switching, where converter 2 switches 180° out of phase from converter 1 in order to minimize the input ripple effects. The controller also features an E/S pin that provides an enable input function, or allows the

converter to be synchronized to an external clock. With the E/S input held low, the LX13088A draws less than 10uA.

Both converters have controlled soft start, in addition to power up sequencing. In the start-up sequence, the output of converter 1 is designed to precede the output of converter 2.

Power On Reset function is provided by means of an open-drain output at the POR pin. The Power On Reset function monitors the voltages at the V_{MON}, FB1 and FB2 pins, and pulls low if any of these voltages drop below the stated POR threshold. The POR is internally deglitched and provides a delayed recovery and reset time.

The LX13088A provides peak over current protection, short circuit protection and thermal shutdown. Discharge-Before-Turn-On discharges the outputs completely before soft starting to always bring them up in the proper sequence at start up or after a POR event.

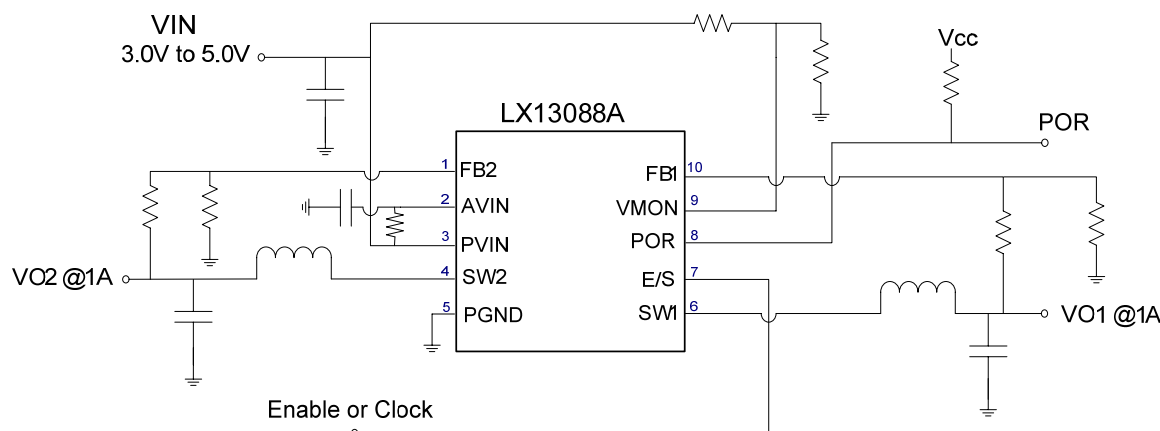
KEY FEATURES

- Outputs Can Be Set From 1V to 3.6V @ 1A, VIN Dependent
- 3.0V to 5.5V Operating Input Voltage Range
- No Rectifier Diode required
- 1.3MHz Switching
- 180° Phase Shifted Switching
- Optional External Clocking (2x clock required)
- Light load Pulse Skipping
- Enable/Sleep state
- Internal Soft Start
- Open-drain Power On Reset Monitors Input and Outputs
- Discharge Before-Turn-On
- Peak Over-Current Protection
- Short Circuit Protection
- Over Temperature Shutdown

APPLICATIONS

- Hard Disk Drives
- Set- Top Boxes

IMPORTANT: For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

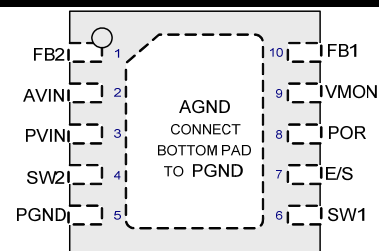
Product Highlight

PACKAGE ORDER INFO
THERMAL DATA

T_A (°C)	LD	Plastic 3x3 mm DFN 10-pin	θ_{JA} = 33 °C/W
	RoHS Compliant / Pb-free		
0 to +70	LX13088ACLD		Junction Temperature Calculation: T _J = T _A + (P _D × θ _{JA}).
Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX13088ACLD-TR)			The θ _{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

ABSOLUTE MAXIMUM RATINGS

PVIN, AVIN to AGND, PGND.....	-0.3 to +7.0 V
SW1 and SW2 to AGND, PGND	PGND -2V to xVIN+2V
All other pins to AGND.....	-0.3V to xVIN + 0.3V
Operating Junction Temperature Range	0°C to 150°C
Storage Temperature Range.....	-65°C to 150°C
Package Peak Temp. for Solder Reflow (40 seconds maximum exposure) ..	260°C (+0 -5)°C

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal. PGND must be wired to AGND externally.

PACKAGE PIN OUT

LD PACKAGE
(Top View)

Marking

088A
Date/Lot Code
MSC

RoHS / Pb-free 100% Matte Tin Finish

FUNCTIONAL PIN DESCRIPTION

Name	Pin #	Description
FB2	1	Feedback from VO2. Connect voltage divider to the load side of VO2 output inductor-capacitor filter.
AVIN	2	Analog Input. Input to power the internal circuitry of the device, connect to PVIN through a 10Ω resistor and bypass through a 1μF ceramic capacitor between this pin and PGND, as close to the LX13088A as possible.
PVIN	3	Control MOSFET switch power inputs. Connect a 10μF ceramic capacitor between this pin and PGND, as close to the LX13088A as possible.
SW2	4	Converter 2 synchronous buck switching output. Connect to VO2 inductor.
PGND	5	Power Ground Connection. Synchronous rectifier MOSFET source. Provide a star connection between this pin, VO1, VO2 filter capacitor returns, VIN input capacitor return, and AGND. Keep the star connection as close to the LX13088A IC as possible.
SW1	6	Converter 1 synchronous buck switching output. Connect to VO1 inductor.
E/S	7	Enable/Synchronization. Pulling this pin high statically enables the LX13088A and pulling the pin low statically will shut down the LX13088A. Applying a pulse to this pin will synchronize SW1 and SW2 switching frequency to ½ the external clock frequency.
POR	8	Power On Reset output pin. Monitors FB1, FB2 output voltage levels and VIN. POR is pulled low if an output voltage droop is detected on FB1 or FB2 or VIN, and is Hi-Z during normal operation.
VMON	9	Voltage Monitor – Supervisor for one external voltage (could be input voltage). The POR output is triggered if this output falls below the VMON threshold.
FB1	10	Feedback from VO1. Connect voltage divider to the load side of VO1 output inductor-capacitor filter.
AGND	PAD	Analog Ground. Connect the exposed pad on the bottom of the package to the GND plane for a thermal heat sink.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature of $0^{\circ}\text{C} < \text{Temp} < 70^{\circ}\text{C}$, and the following test conditions: $3.0 \leq V_{\text{VIN}} \leq 5.5\text{V}$, $V_{\text{PGND}} = V_{\text{AGND}}$; E/S = High (Static)

Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
Input Circuitry						
Operating Input Voltage	V_{VIN}		3.0		5.5	V
Under Voltage Lockout	$V_{\text{VIN-UVLO}}$	V_{VIN} Rising	2.4	2.7	2.85	V
UVLO Hysteresis			200	300	400	mV
Input Supply Current	I_{VIN}	$T_{\text{A}} = 25^{\circ}\text{C}$; not switching; $1.2\text{V} = V_{\text{FB1}} = V_{\text{FB2}}$	0.01	0.6	1	mA
		E/S = low		0.1	10	μA
VMON Input						
POR Threshold VMON	$V_{\text{VMON-POR}}$	V_{VMON} Falling (hysteresis = 20mV)	0.97	1.00	1.03	V
VMON input current	I_{VMON}	$V_{\text{VMON}} = 1.25\text{V}$	-100	0	100	nA
VO1 Output						
Feedback Voltage	V_{FB1}		0.975	1.000	1.025	V
Peak Current Limit Threshold	$I_{\text{SW1-CT}}$	$V_{\text{VIN}} = 3.0\text{V}$	1.0	1.4		A
		$V_{\text{VIN}} = 5.0\text{V}$	1.2	1.6		
PWM Switching Frequency	F_{SW1}	E/S = static logic high		1.3		MHz
Upper FET On Resistance	$R_{\text{DS}_{\text{SW1-U}}}$	$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=3.3\text{V}$		315		m Ω
		$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=5\text{V}$		282		
Lower FET On Resistance	$R_{\text{DS}_{\text{SW1-L}}}$	$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=3.3\text{V}$		255		
		$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=5\text{V}$		226		
Soft Start Time	$t_{\text{SS_FB1}}$		0.5	1	2	ms
POR Threshold FB1	$V_{\text{FB1-POR}}$	FB1 Falling (hysteresis = 2% V_{FB1})	87	89.5	92	% V_{FB1}
Discharge Complete Threshold	$V_{\text{FB1-DCT}}$	FB1 level where discharge cycle is terminated	50	75	100	mV
VO2 Output						
Feedback Voltage	V_{FB2}		0.975	1.000	1.025	V
Peak Current Limit	$I_{\text{SW2-CT}}$		1.2	1.6		A

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Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
PWM Switching Frequency	F_{SW2}	E/S = static logic high		1.3		MHz
Upper FET On Resistance	$R_{\text{DS}_{\text{SW2-U}}}$	$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=3.3\text{V}$		290		m Ω
		$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=5\text{V}$		255		
Lower FET On Resistance	$R_{\text{DS}_{\text{SW2-L}}}$	$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=3.3\text{V}$		170		m Ω
		$T_{\text{J}} = 25^{\circ}\text{C}$, $V_{\text{in}}=5\text{V}$		151		
Soft Start Time	$t_{\text{SS}_{\text{FB2}}}$		0.5	1	2	ms
POR Threshold FB2	$V_{\text{FB2-POR}}$	FB2 Falling (hysteresis = 2% V_{FB2})	87	90	92	% V_{FB2}
Discharge Complete Threshold	$V_{\text{FB2-DCT}}$	FB2 level where discharge cycle is terminated	50	75	100	mV
E/S						
E/S Threshold	$V_{\text{E/S-H}}$		1.5			V
	$V_{\text{E/S-L}}$				0.6	V
E/S Leakage Current	$I_{\text{E/S}}$	$0 < V_{\text{E/S}} < V_{\text{VIN}}$	-100		100	nA
Frequency lock in range	$F_{\text{E/S-MIN}}$	Switching frequency is $\frac{1}{2}$ E/S frequency when externally clocked.			1.5	MHz
	$F_{\text{E/S-MAX}}$		3.0			
Shutdown delay	$t_{\text{E/S-SHDN}}$	Shutdown initiated if logic low is of longer duration than delay.	2	4	10	μs
POR						
POR Assert Delay Time	$t_{\text{POR_DELAY}}$	Fault Flag set to POR pull low		25		μs
POR Release Delay Time	$t_{\text{POR_HOLD}}$	Fault Flag reset to POR Hi-Z state	10	20	30	ms
POR Low Voltage	$V_{\text{POR_LOW}}$	POR sinking 4mA		200	400	mV
POR High Leakage	$I_{\text{POR_HI}}$	POR High Level		0.003	1	μA
Power Up Sequencing						
VO2 Start Threshold	$V_{\text{FB1-ST}}$	FB1 rising voltage for FB2 to initiate soft start	87	90	93	% V_{FB1}
Brown Out Discharge						
SW1, SW2 Discharge Resistance	$R_{\text{STOP-SW1,2}}$	Discharge Resistance for SW1 and VO2	15	30	45	Ω

ELECTRICAL CHARACTERISTICS

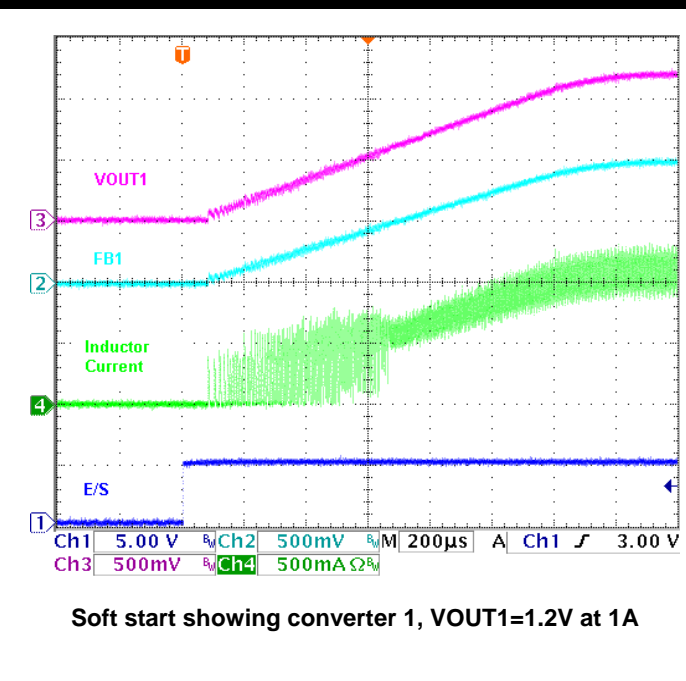
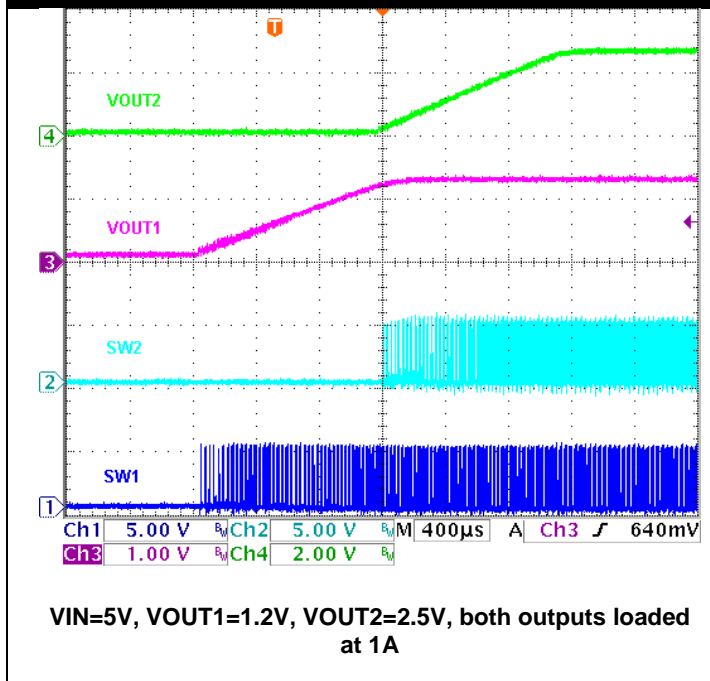
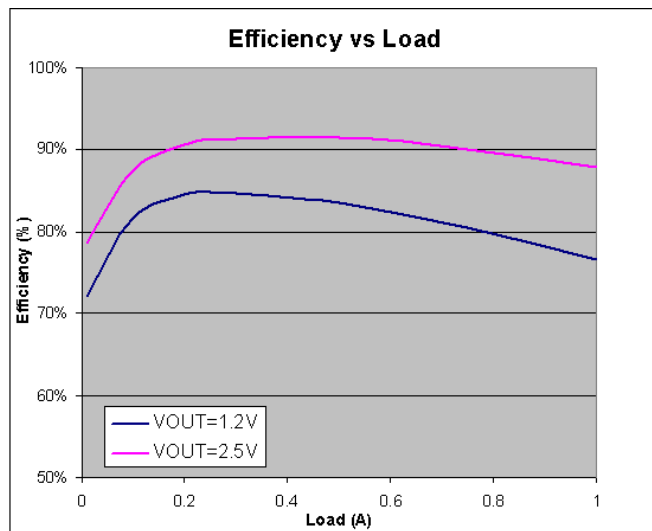
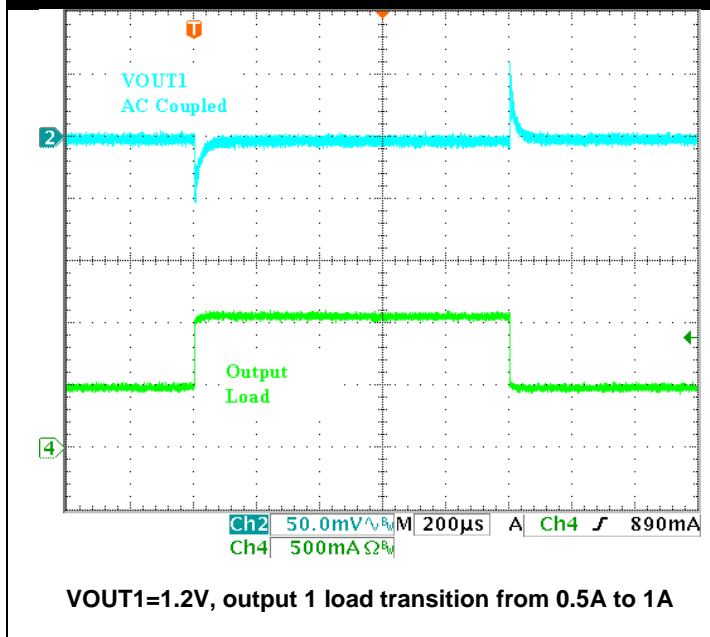
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Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
SW1, SW2 Discharge Resistance matching	$R_{\text{STOP-SW1}} / R_{\text{STOP-SW2}}$		0.90	1	1.1	

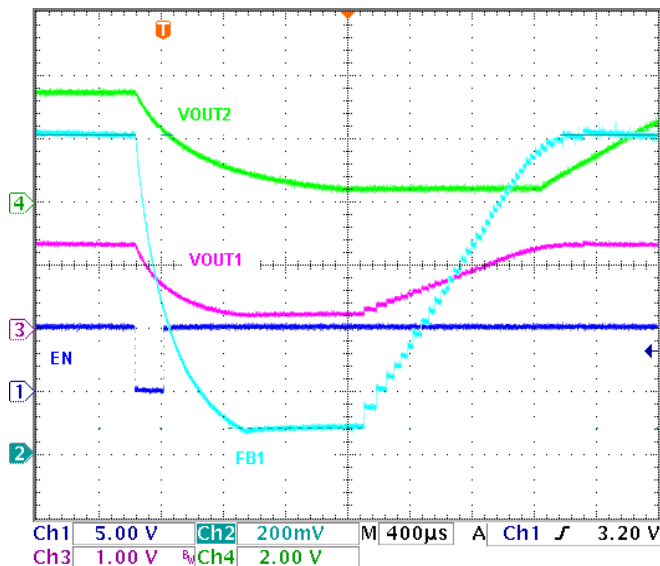
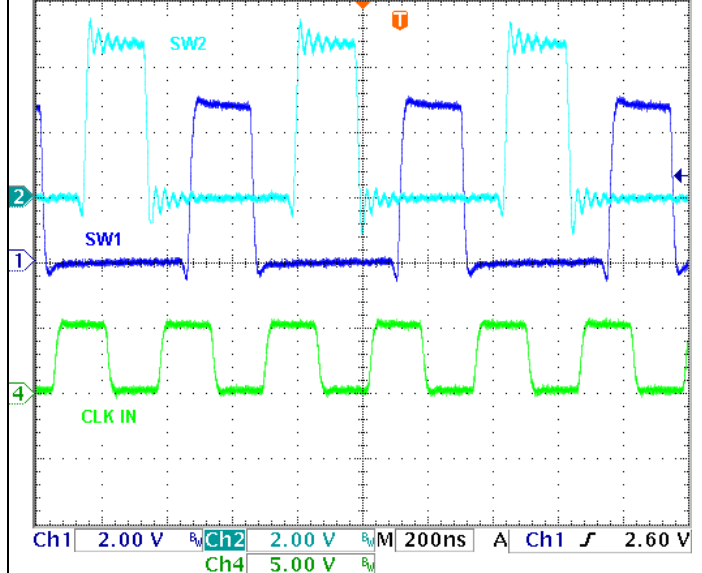
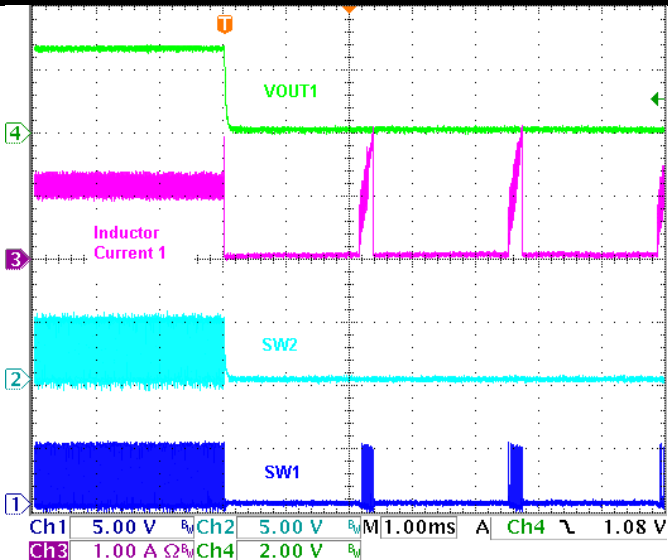
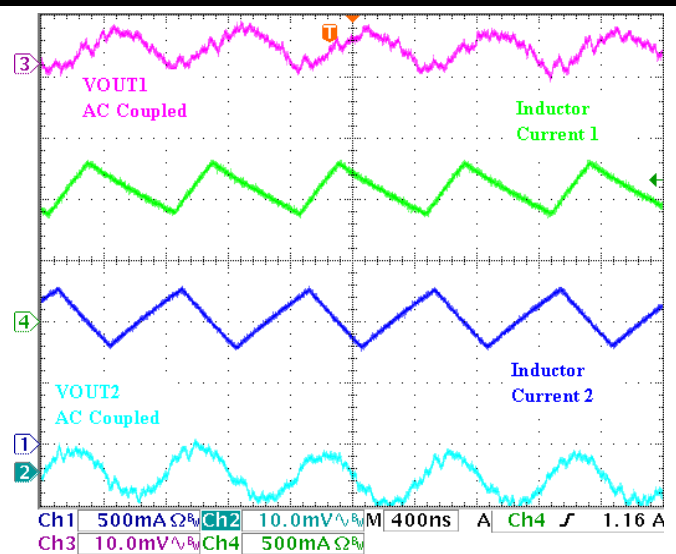
SYSTEM CHARACTERISTICS

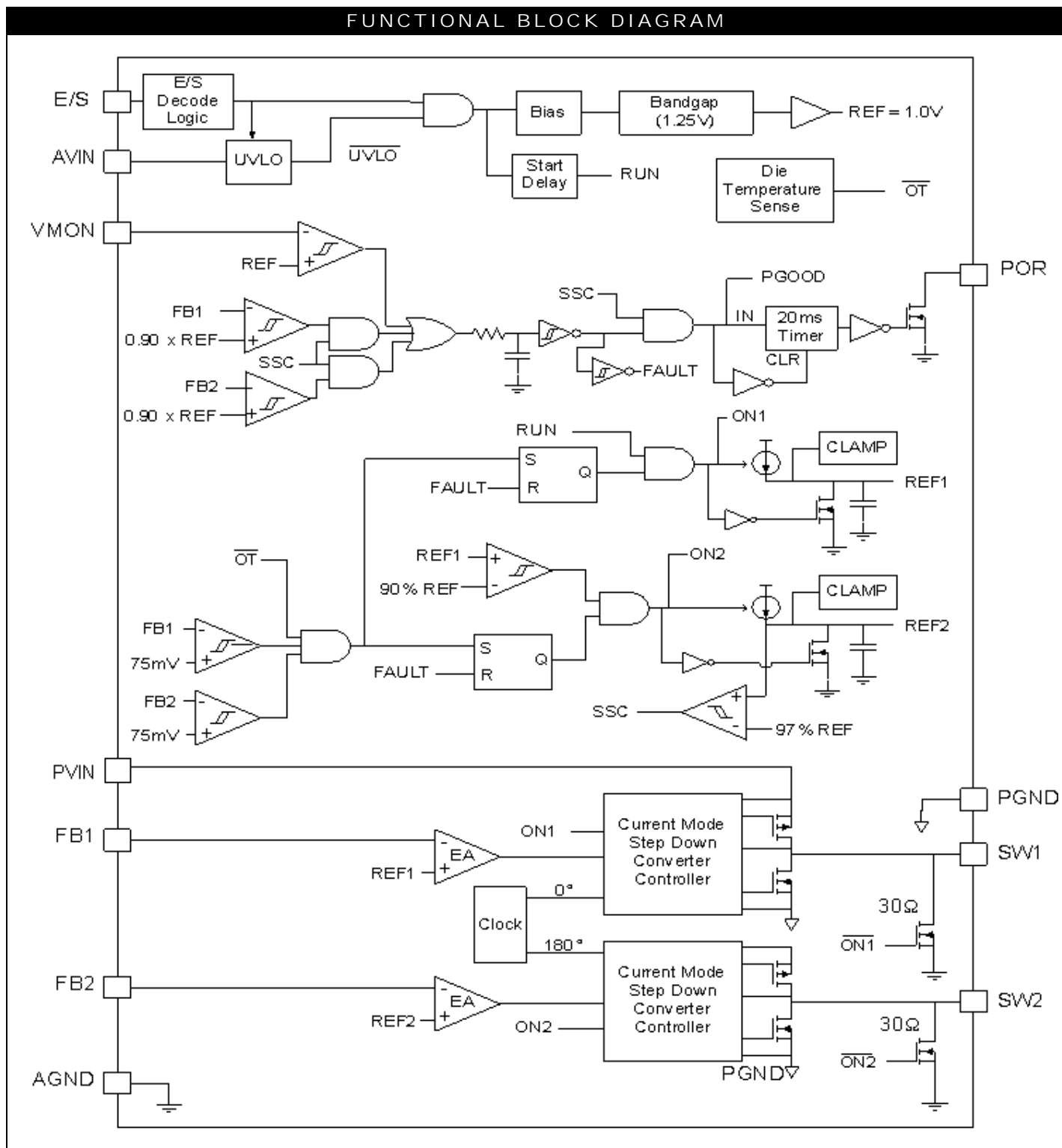
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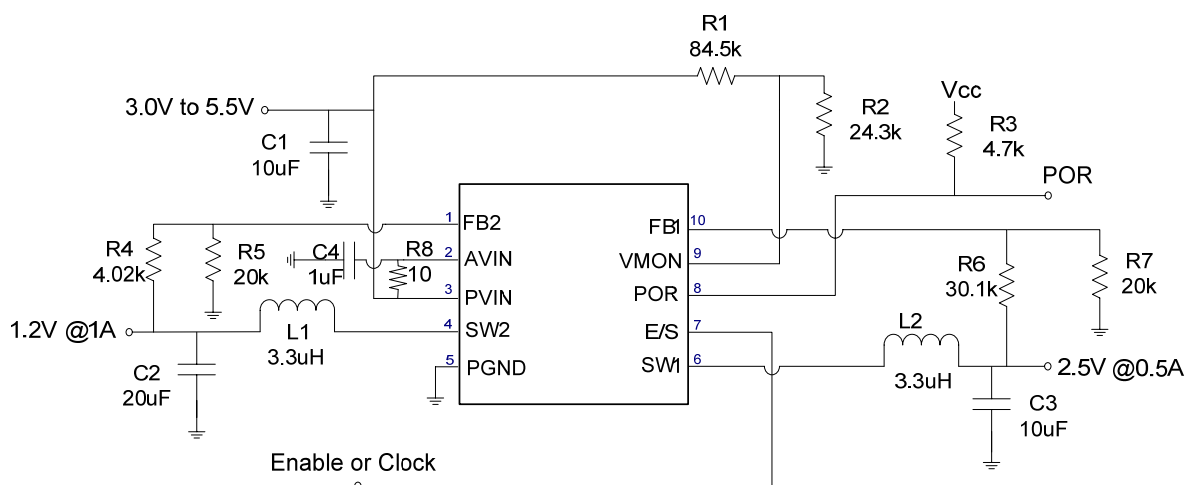
Parameter	Symbol	Test Conditions / Comment	Min	Typ	Max	Units
VO1 Output						
Line Regulation	VO1	$I_{\text{SW1(ave)}} = 300\text{mA}$; $3.0\text{V} < V_{\text{VIN}} < 5.50\text{V}$		0.1		%
Load Regulation	VO1	$5\text{mA} \leq I_{\text{SW1(ave)}} \leq 1000\text{mA}$		0.5		%
Efficiency (L_1 DCR = $44\text{m}\Omega$) $V_{\text{in}}=5\text{V}$ Figure 2 Schematic	η_{VO1}	$I_{\text{SW1(ave)}} = 1000\text{mA}$; $\text{VO1} = 2.5\text{V}$		87		%
		$I_{\text{SW1(ave)}} = 200\text{mA}$; $\text{VO1} = 2.5\text{V}$		94		
		$I_{\text{SW1(ave)}} = 10\text{mA}$; $\text{VO1} = 2.5\text{V}$		82		
VO2 Output						
Line Regulation	VO2	$I_{\text{SW2(ave)}} = 300\text{mA}$; $3.0\text{V} < V_{\text{VIN}} < 5.50\text{V}$		0.1		%
Load Regulation	VO2	$5\text{mA} \leq I_{\text{SW2(ave)}} \leq 1000\text{mA}$		0.5		%
Efficiency (L_2 DCR = $44\text{m}\Omega$) $V_{\text{in}}=5\text{V}$ Figure 2 schematic	η_{VO2}	$I_{\text{SW2(ave)}} = 1000\text{mA}$; $\text{VO2} = 1.2\text{V}$		80		%
		$I_{\text{SW2(ave)}} = 200\text{mA}$; $\text{VO2} = 1.2\text{V}$		90		
		$I_{\text{SW2(ave)}} = 10\text{mA}$; $\text{VO2} = 1.2\text{V}$		75		
Thermal Shutdown						
Thermal Shutdown Threshold				160		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis				20		$^{\circ}\text{C}$

STARTUP SEQUENCING
SOFTSTART

DYNAMIC LOAD
EFFICIENCY


Efficiency for 2.5V and 1.2V output voltages, VIN=5V

STARTUP AFTER OUTPUT DISCHARGE

Outputs must discharge to <10% before repeat startup
SYNCHRONIZATION

Synchronization & out of phase, 3MHz CLK IN at E/S Input
CURRENT LIMIT & SHORT CIRCUIT

VOUT1 shorted to ground continuously after normal regulation
OUTPUT RIPPLE

Both outputs loaded at 1A, peak to peak output ripple is ~10mV


Figure 1. Functional Block Diagram

TYPICAL APPLICATION

Figure 2. Typical Application Circuit

THEORY OF OPERATION**DC-DC SWITCHING STEP DOWN CONVERTERS**

The LX13088A dual DC-DC converters are current mode buck converters with integrated high side switch, synchronous rectifier and internal compensation. They are designed to be stable with a 3.3 μ H inductor value and 10 μ F to 22 μ F output capacitor. Both output voltages are resistor divider programmable. The switching frequency of the converter is fixed and the switches turn on at alternating 180° phase intervals.

The converters operate in 3 possible modes: continuous mode (CM), discontinuous mode (DM), and pulse skipping mode (PSM). CM is the default mode under normal loading. DM occurs under light loads, where switching still occurs at the programmed frequency. In DM, a zero crossing detector shuts off the synchronous rectifier to prevent reverse rectifier current; this results in a portion of the switch period where neither switch is on. Under very light loads, PSM mode occurs, where switching cycles are skipped if the current demand is low in order to provide better efficiency. Both outputs are capable of providing a minimum of 1A output current capability when V_{in} is within 4.5 to 5.5V. However as V_{in} drops below this range, Output VO1 current capability drops to 800mA.

SOFTSTART

The DC-DC converters contain a soft start function that brings the output voltages up via a slowly increasing ramp with any resistive load from open circuit to 1A. The output voltage waveform shall not vary by more than 50mV from a straight line drawn from the initial voltage to the final steady state voltage. During soft start, the peak inductor current shall not exceed 750mA until the output voltage reaches 25% of its final value. Current limit shall be active but not trip during soft start into a rated resistive load. Overshoot voltage during soft start is limited to 1%.

ENABLE AND POWER UP SEQUENCING

When power is applied at V_{IN} and if the E/S input is asserted (High) or is toggling, the DC-DC converters will enter RUN mode after a short settling period. If the E/S pin is a static low, the IC will enter a SLEEP state where it draws very little input current, less than 10 μ A.

When in RUN mode, if there is no fault condition, the VO1 output of converter will be the first output to begin soft start. When the reference voltage for FB1 reaches approximately 90% of the final value, the VO2 output of converter will begin soft start.

POR

Under-voltage comparators are provided to monitor the output voltages and the voltage at V_{MON} which could be the input supply voltage. If any of these voltages falls below its POR threshold, the POR open drain output will turn on which pulls the POR pin low. Note that the fault to POR assert delay time is approximately 20 μ S. If the POR fault condition is cleared, there is a delay of 20ms before the POR output transistor is turned off; when off the POR pin is high Z and may be pulled up high via a resistor.

The POR function has built in deglitching. Once the POR is detected, the power supply outputs will be discharged prior to a restart condition, where soft start and power up sequencing will occur.

OUTPUT DISCHARGE

After the occurrence of a POR situation, and the POR fault condition is immediately cleared, startup and soft start is delayed until the outputs are discharge to <10%. During the discharge phase, the soft start internal reference voltages (REF_x) are shorted to ground to quickly discharge it. The output capacitors are discharged via an internal 30 Ω pull down switch on each of the SW1 and SW2 pins. When the FB_x voltage and the REF_x voltage are fully discharged and if there is not an OT condition, the outputs are then allowed to begin the normal soft start power up sequence. During the discharge phase, the control high side and synchronous rectifier MOSFETs are in the high-Z off state.

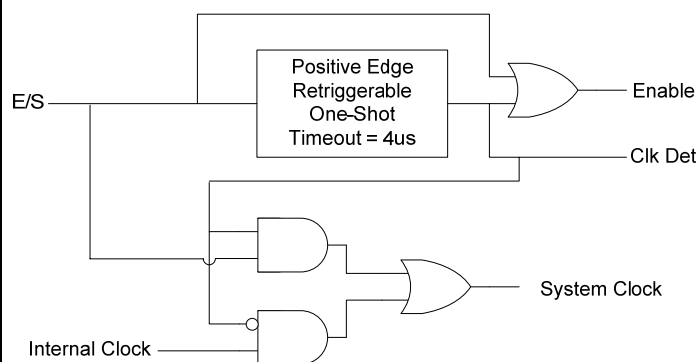
OVER CURRENT AND SHORT CIRCUIT PROTECTION

The DC-DC converters have over current and short circuit protection. During any mode of operation, any value of load resistance (including 0 ohms) can be applied to the DC-DC outputs instantaneously and held in place indefinitely without the switch current exceeding the peak current limit and without the IC suffering any permanent damage or loss of performance. The output voltage is allowed to drop under over current or short circuit conditions. Both converters will stop switching if either one experiences an over current condition for various cycles.

Recovery to output voltage regulation occurs within 10ms of the instant the loading is reduced to maximum allowable rated load; the output voltage shall not exceed the dynamic load excursion limits (+/-5% excursion) upon recovery.

OPERATION
E/S DECODER LOGIC

The E/S pin serves a dual purpose. It will enable the IC if it detects either a valid clock signal or a static high logic level. A static low logic level for longer than 4μs is determined to be a shutdown signal. The decode logic is shown below. The One-shot function will produce a logic high output (Clock Detect) as long as the E/S pin is toggling. Clock Detect is used to keep ENABLE high and to select the E/S clock as the system clock. If E/S is a static high (non-toggling) input, the retriggerable one-shot will go low after 4μs; this will set Clk Det low and select the internal oscillator as the system clock.


SYNCHRONIZATION

The converters can be synchronized to an external system clock present at the E/S input pin. During synchronization, the converter's switching frequency will be ½ the frequency of the external clock, and the two converters will still be 180 degrees out of phase. The lock in frequency for synchronization is specified to be between 1.5MHz to 3MHz, minimum sync pulse width is 100ns.

OVER TEMPERATURE PROTECTION

If an over temperature fault occurs, the DC-DC converter will stop switching and the SW# outputs will become high impedance. Note that the temperature fault occurs at a die temperature of approximately 160°C. When the IC cools down, it will attempt to resume switching. If a POR is activated as a result of the OT situation, restart will be subject to the soft start/sequencing routine and will not occur until the OT condition has been corrected.

The device junction temperature is a function of the device's total power dissipation, the junction to ambient thermal resistance, and the ambient temperature:

$$T_J = T_A + (P_{TOTAL} \times \theta_{JA})$$

The total power dissipated by the LX13088A device, P_{TOTAL} , will be comprised of the power dissipated by the RMS current flowing through the internal high-side FET during the duty cycle D time, by the RMS current flowing through the synchronous rectifier during 1-D time, by the switching or transitioning of the FET, and of the power dissipated by the device supply current.

INDUCTOR SELECTION

A 3.3μH ±20% inductor is suggested as the internal compensation has been optimized around this inductor value. A 3.3μH is a good compromise, since for an output voltage ranging from $V_{OUT} = 1V$ to $V_{OUT} = 4V$, loaded at 1A, the LIR or the ratio of inductor ripple current to output load will range from about 20% to 30%, assuming $V_{IN} = 5V$ and the converter switching at 1.3MHz.

OUTPUT CAPACITOR

To ensure stability and good load transient response, use at least a 10μF output capacitor at VO1 output, and a 20μF or greater at VO2 output. Output ceramics capacitors with low ESR are suitable.

SETTING THE OUTPUT VOLTAGE

The LX13088A converter's maximum duty cycle is approximately 90%. For a 5V input, 90% duty cycle will be achieved for an output voltage of about 4V loaded at 1A.

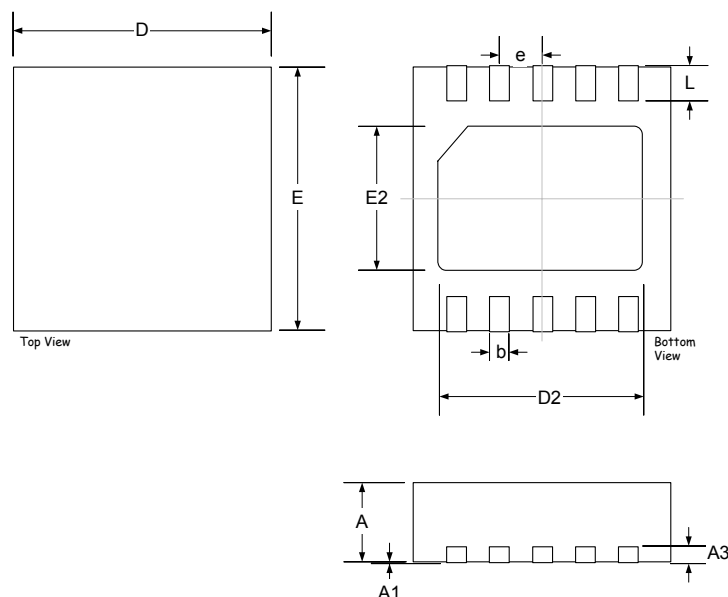
To set the output voltage, connect a resistive divider from the output to the FBx pin to signal ground. Note that the feedback voltage is 1.0V. For the desired output voltage V_{OUT} , the upper resistor from V_{OUT} to FB (R_{UPPER}) is calculated by the following equation:

$$R_{UPPER} = R_{LOWER} \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

R_{LOWER} , or the resistor from FBx pin to ground, is selected to be 20kΩ. $V_{FB} = 1V$, and V_{OUT} is chosen by the designer for the given application.

MAXIMUM DUTY CYCLE

Device maximum duty cycle is typically 89%. The output capability of the device will be limited to the maximum duty cycle. For example, for $V_{IN}=3.3V$, $V_{OUT}=2.5V$ at 1A load, the device will be near its maximum duty cycle. Thus, lowering the input voltage below 3.3V will cause the converter's duty cycle to become unstable and jump to 100% duty cycle. For $V_{IN}=3.0V$, $V_{OUT}=2.5V$, output load capability will be reduced since maximum duty cycle will occur at an output load level below 1A.

PACKAGE DIMENSIONS
LD
10-Pin Plastic MLP Dual Exposed Pad


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.0315	0.0394
A1	0	0.05	0	0.0019
A3	0.20 REF		0.0079 REF	
b	0.18	0.30	0.0071	0.0118
D	3.00 BSC		0.1181 BSC	
D2	2.23	2.48	0.0878	0.0976
e	0.50 BSC		0.0197 BSC	
E	3.00 BSC		0.1181 BSC	
E2	1.49	1.74	0.0587	0.0685
L	0.30	0.50	0.0071	0.0197

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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