

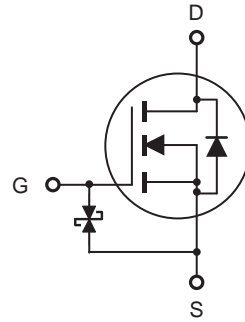


# CED01N6/CEU01N6

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 650V, 0.9A,  $R_{DS(ON)} = 15 \Omega$  @  $V_{GS} = 10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous	$I_D$	0.9	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	3.6	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above $25^\circ\text{C}$	$P_D$	31	W
		0.25	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy <sup>d</sup>	$E_{AS}$	60	mJ
Avalanche Current	$I_{AS}$	0.8	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$



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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			10	$\mu A$
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-10	$\mu A$
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 0.4A$		12	15	$\Omega$
<b>Dynamic Characteristics <sup>c</sup></b>						
Forward Transconductance	$g_{FS}^b$	$V_{DS} = 20V, I_D = 0.4A$		0.5		S
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		136		pF
Output Capacitance	$C_{oss}$			46		pF
Reverse Transfer Capacitance	$C_{rss}$			19		pF
<b>Switching Characteristics <sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300V, I_D = 0.4A, V_{GS} = 10V, R_{GEN} = 4.7\Omega$		19	38	ns
Turn-On Rise Time	$t_r$			13	26	ns
Turn-Off Delay Time	$t_{d(off)}$			24	48	ns
Turn-Off Fall Time	$t_f$			35	70	ns
Total Gate Charge	$Q_g$	$V_{DS} = 480V, I_D = 0.8A, V_{GS} = 10V$		6	8	nC
Gate-Source Charge	$Q_{gs}$			1.0		nC
Gate-Drain Charge	$Q_{gd}$			4.4		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				0.8	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 0.8A$			1.6	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing. d.L = 190mH, $I_{AS} = 0.8A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25^\circ\text{C}$ .						



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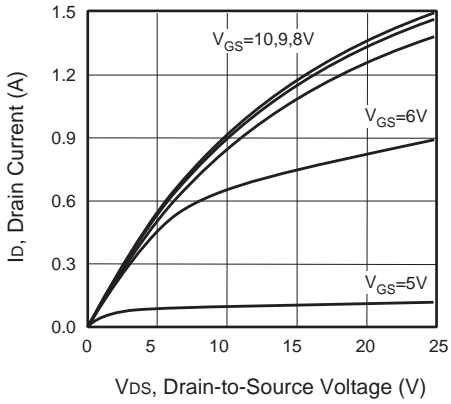


Figure 1. Output Characteristics

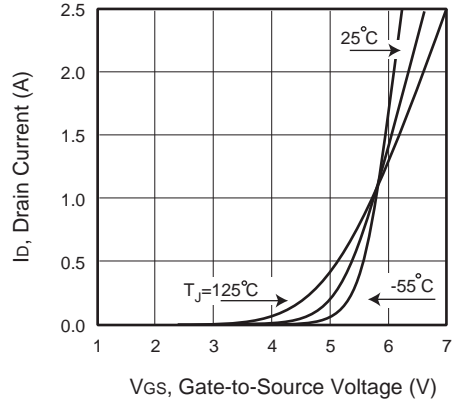


Figure 2. Transfer Characteristics

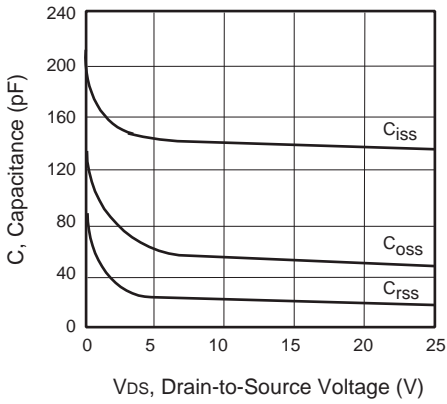


Figure 3. Capacitance

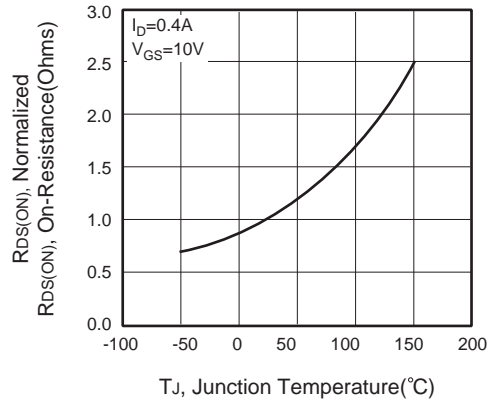


Figure 4. On-Resistance Variation with Temperature

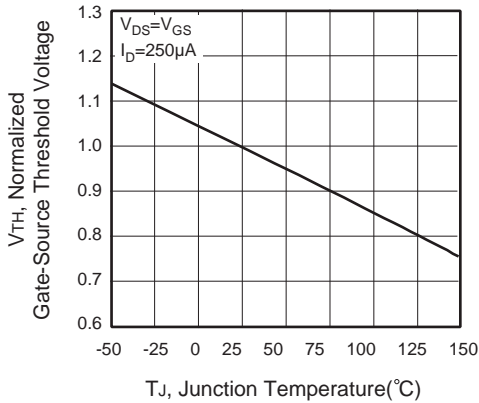


Figure 5. Gate Threshold Variation with Temperature

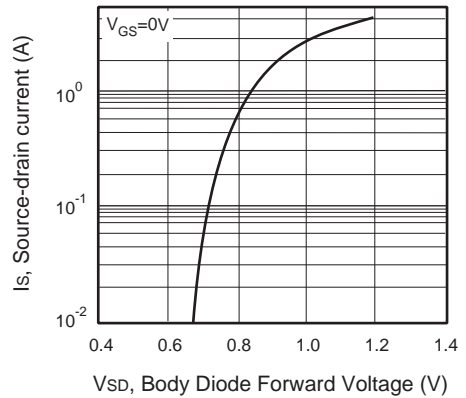


Figure 6. Body Diode Forward Voltage Variation with Source Current



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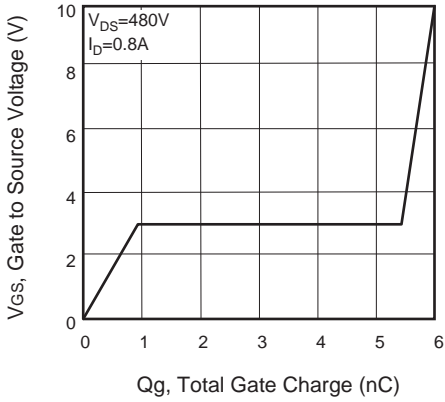


Figure 7. Gate Charge

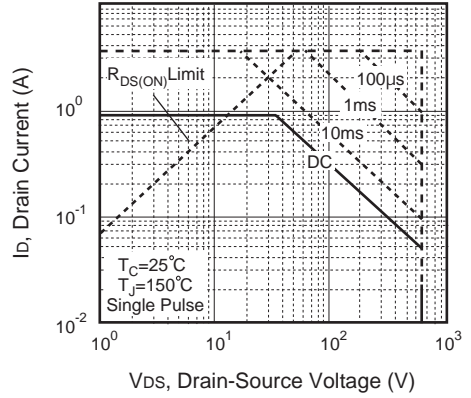


Figure 8. Maximum Safe Operating Area

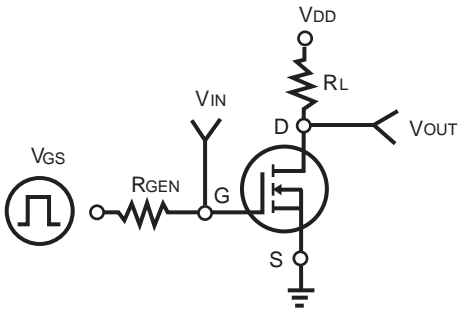


Figure 9. Switching Test Circuit

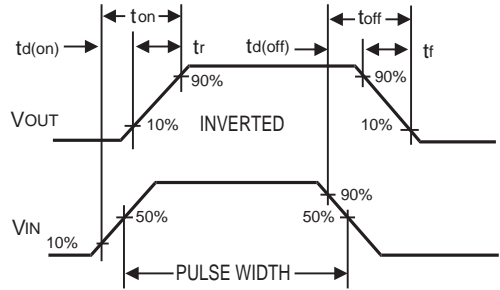


Figure 10. Switching Waveforms

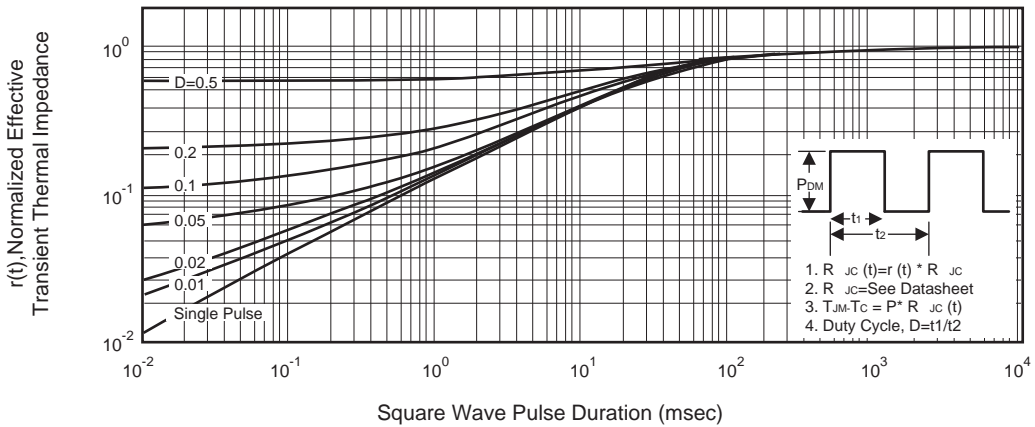


Figure 11. Normalized Thermal Transient Impedance Curve