Equator Hardware Reference

MAP-CA DSP Datasheet

Equator Technologies, Inc.

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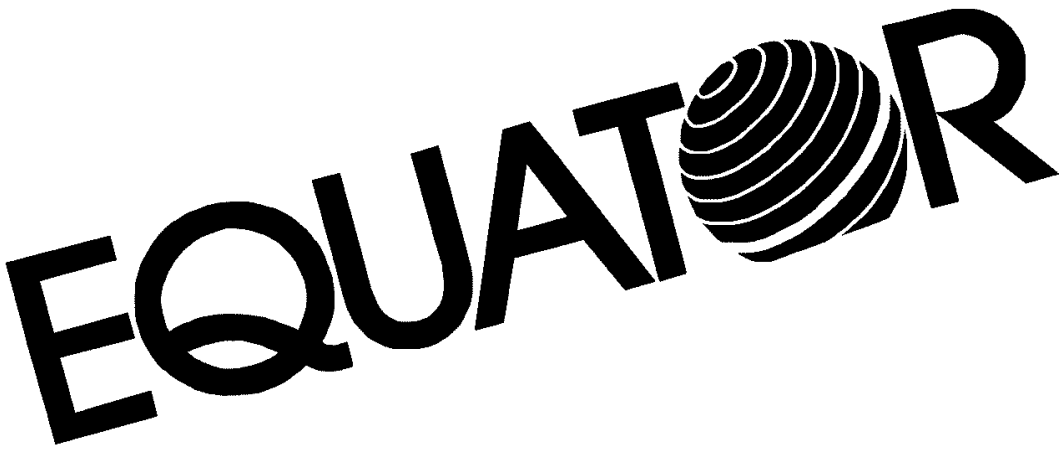

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`Italicized Courier New` text is used for any portion of a path name, including individual file names.

`Bold Courier New` text is used for any placeholder for a set of text input or output items for a program.

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Introduction to the MAP-CA Digital Signal Processor Chip

The MAP-CA digital signal processor offers a highly integrated single chip solution for broadband products such as set-top boxes, digital TVs, video conferencing systems, medical imaging products, digital video editing equipment, and office automation products. The MAP-CA DSP is a member of the MAP Series VLIW processors. A parallelizing C compiler, linker, source level debugger, simulators, and libraries are available. Reference software modules, including MPEG-2 encode and decode, JPEG encode and decode, video post-filtering, audio, telephony, and video teleconferencing codecs are also available to accelerate customer product development. Because core media applications can be delivered in software on the MAP-CA DSP platform, it is easy to add, remove or enhance the functions of final products. The MAP-CA DSP provides the proven and effective solution for rapidly evolving broadband applications.

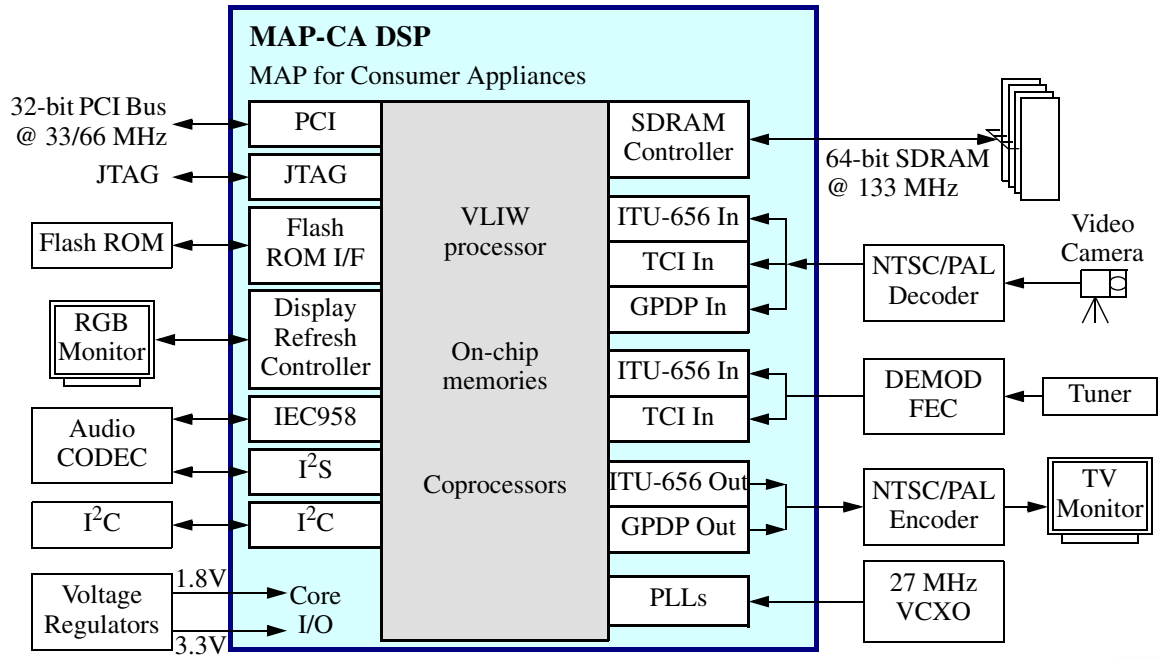
VLIW Core

- Highly pipelined Very Long Instruction Word processor that issues four operations per clock cycle
  - four 32-bit integer ALUs, two 64-bit shuffle/partitioned add units, and two 128-bit multimedia units
  - 128 32-bit general purpose registers, which can be treated as sixty-four 64-bit general purpose registers
  - thirty-two 1-bit predicate registers
  - eight special 128-bit registers
- 11+ GOPS sustained 16-bit SIMD operations @300 MHz
- 24+ GOPS sustained 8-bit SIMD operations @300 MHz
- 30+ GOPS @ 300 MHz for sum of absolute differences block matching
- 1800 MIPS @ 300 MHz in 32-bit integer arithmetic
- Bi-endian support

Memory Hierarchy

- 32 KB two way set associative, LRU replacement policy, compressed format instruction cache
- 32 KB four way set associative, four bank interleaved, true LRU, write-back data cache
- Separate MMUs for instruction, data and DMA with fully associative sixteen entry TLB for each MMU
- Glueless high speed 133 MHz SDRAM/SGRAM interface, supporting up to 128 MB

System Diagram



Coprocessors

- Programmable VLx (16-bit RISC processor) with acceleration for variable length decoding and encoding with 4 KB data memory and 4 KB instruction memory
- 4 (vertical) × 5 (horizontal) / 3 × 5 / 2 × 5 tap Video Filter with 6KB line buffer memory
- Programmable DataStreamer (64 channel DMA engine) with 8 KB buffer memory
- DES support

IO Interfaces

- 33 MHz/66 MHz 32-bit PCI bus
- IEC958 audio interfaces
- I^2S audio interfaces
- Video input:
  - two DVB compliant transport channel interfaces

    or
  - one DVB compliant transport channel interface and one ITU-R BT.601/656 input

    or
  - two ITU-R BT.601/656 inputs

    or
  - one of any of the above and one general data port
- One ITU-R BT.601/656 video output or one general data port
- Display Refresh Controller (DRC) with on-chip color space conversion, palette table lookup, alpha-blending, and hardware cursor
- 110 MHz RAMDAC with sync on green for analog RGB monitor
- I^2C master/slave interface
- Flash ROM (EEPROM) interface

Data Sheet Overview

This data sheet provides the following information:

- An overview of the MAP-CA DSP architecture
- A description of the software development platform
- A description of the hardware development platform
- Packaging information
- Electrical specifications

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Chapter 1 Architecture Overview

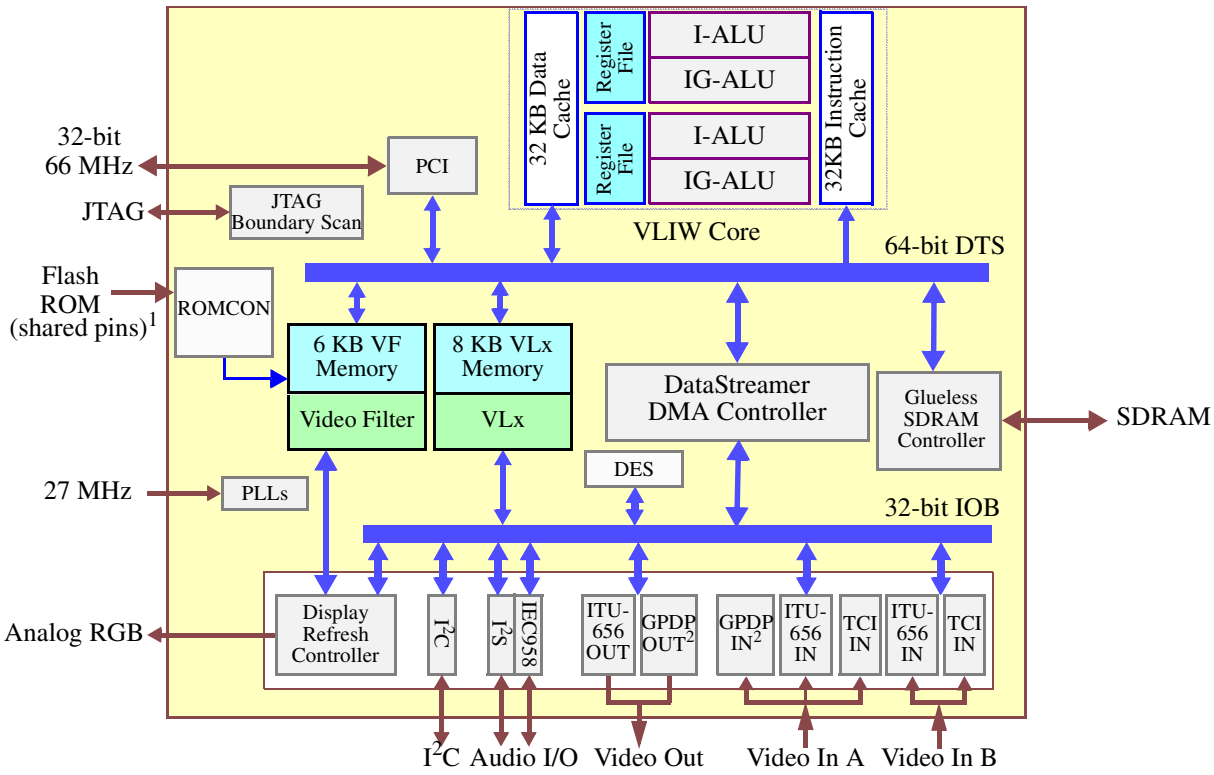


Figure 1-1: MAP-CA DSP Block Diagram

1. Some pins have multiple uses. See Chapter 3, Chapter 4, and Chapter 6 for more information
2. ITU-656 Out is unavailable for use when GPDP In is enabled due to sharing of interface signals.

The MAP-CA digital signal processor is a high performance processor providing broadband applications with solutions addressing the convergence of communications, consumer appliances and computing. The MAP-CA DSP combines general purpose RISC-like processing with high performance signal and image processing. The MAP-CA DSP supports programmable video, image, and signal processing software implementations of compression and decompression algorithms. The MAP-CA DSP matches the cost and performance features of dedicated fixed function chips, with the added flexibility to rapidly respond to evolving standards. Figure 1-1 shows a block diagram of the MAP-CA DSP. The MAP-CA DSP consists of a VLIW core, programmable coprocessors, on-chip memories, and I/O interfaces.

The VLIW core executes four operations in parallel and supports partitioned SIMD operations for 8, 16, 32, and 64-bit data types. Coprocessors on the MAP-CA digital signal processor help accelerate serial operations like variable length encoding/decoding and video filtering.

Several audio/video interfaces are supported, including ITU-R BT.601/656 input and output; MPEG-2 transport channel interface (TCI); IEC958 and I^{2}S digital audio interfaces. Two video inputs can be used at the same time. The Display Refresh Controller (DRC) supports RGB computer screen refresh and also has hardware support for overlay-

ing a hardware cursor and graphics/text or a secondary video channel on the primary video channel. An I^2C bus interface is also provided.

These I/O functions execute in parallel with the CPU and eliminate the need for several external ASICs with their associated cost and bandwidth issues.

A glueless SDRAM controller supports access up to a 133 MHz SDRAM. The MAP-CA digital signal processor supports a 128 MB memory size. A 32-bit 33/66 MHz PCI bus interface is also supported. The MAP-CA DSP boots from either the PCI bus or the Flash ROM interface.

There are three on-chip PLLs (core/SDRAM, pixel, audio) that generate all the internal clocks from a single 27 MHz external clock input (`pclk`). The `tci_vdac` pin can be used to output a controlling signal that can be used to drive a one bit sigma-delta modulator for an external VCXO which in turns modulates the frequency on `pclk`.

1.1 The VLIW Core

Real-time handling of multimedia data stresses processor performance. There are three basic ways to increase a processor's performance: decrease the cycle time, decrease the number of cycles required to execute an instruction, and execute more instructions per cycle. The first two are becoming increasingly difficult to improve beyond process scheduling, while the last is now receiving more attention. Executing more instructions per cycle exploits the natural parallelism available in most software. Very Long Instruction Word (VLIW) processors use this parallelism by packing multiple operations into a single instruction word, which is then executed as a unit.

VLIW architectures differ from superscalar architectures in that the grouping and scheduling of instructions for execution is done at compile time, rather than execution time. The iMMediaC compiler searches for eligible operations, checks for dependencies and resource conflicts, and packages these eligible operations into VLIWs. The compiler can explore beyond the limited search window seen in superscalar architectures and cross natural boundaries, such as branches, to search for opportunities for parallelism. The iMMediaC compiler uses a technique known as "trace scheduling" to search a whole routine for eligible operations.

By moving the difficult task of finding parallelism into software, VLIW techniques dramatically simplify the CPU design by reducing gate count and freeing valuable die area for other performance enhancements or lower costs. While VLIW is primarily designed to exploit parallelism, its simplification of the processor architecture allows for reduced cycle times as well.

1.1.1 Execution Units

The MAP-CA DSP operations are primarily 3-operand RISC operations. As in a typical RISC architecture, load and store operations are the only means of referencing memory. The MAP-CA DSP has four functional units: two I-ALUs, and two IG-ALUs. Each I-ALU contains a load-store unit, an integer ALU, and a branch unit. Each IG-ALU contains an integer/graphics unit and a multimedia operation unit. The I-ALU and IG-ALU support different operations, but many integer and logical operations are implemented in both units. This overlap allows the compiler to schedule more operations in parallel and make more efficient use of all the functional units.

There are 128 32-bit registers usable separately or in pairs as 64-bit registers, 32 1-bit predicate registers, and eight special 128-bit registers. The 128-bit (PLC/PLV) registers are used for FIR filter, SAD, FFT, ADD, DCT, and other specialized partitioned integer operations. The large register files help minimize unnecessary instruction dependencies caused by logically distinct register reuses.

Each MAP-CA digital signal processor instruction contains four operations. The Media Intrinsics operations include partitioned operations over these data types. Load and store operations can perform one, two, four, and eight byte accesses, with support for both little-endian and big-endian byte orderings. Dynamic address translation and virtual memory protection are fully supported. The 1-bit logical values are also used to support predicated execution, which substantially enhances available parallelism by allowing partial speculation and eliminating branching.

1.1.1.1 I-ALU

The I-ALU performs the following operations:

- 32-bit integer arithmetic operations including compare
- Logical and bitwise logical operations whose results can be sent to general or predicate registers
- Address calculations for indexed addressing
- Memory reference
- Branching
- System control operations

1.1.1.2 IG-ALU

The IG-ALU performs the following operations:

- 32-bit integer arithmetic operations (same as the I-ALU)
- Logical and bitwise logical operations (same as the I-ALU)
- 64-bit integer arithmetic operations
- Shift/extract/merge operations
- 64-bit SIMD operations (with 8-bit, 16-bit, and 32-bit partitions) including selection, comparison, selection of maximums and minimums, addition, multiply-add, complex multiplication, inner product, and sum of absolute differences
- 128-bit partitioned (with 8-bit, 16-bit, and 32-bit partitions) SIMD operations including inner-product with new partition shift-in for efficient FIR operation and sum of absolute differences with new partition shift-in for efficient block matching operation

1.1.1.3 Simple Interlocks

Certain operations require more than one cycle to complete. No hardware interlocks are needed to prevent issue of an operation that attempts to read a result not yet completed. The iMMediaC compiler is responsible for correct scheduling, not hardware. Register scoreboarding is supported for outstanding loads.

1.1.1.4 Extensive Predication

Nearly all operations can have their effect controlled by the value of a selected (1-bit) predicate register. A predicate register is tested to determine whether or not the operation should be performed. This allows the compiler to aggressively convert control flow into data flow, enabling a substantially higher degree of instruction-level parallelism. This also greatly helps to reduce any penalties for branching, without the cost and complexity of hardware branch prediction.

1.1.2 Register Resources

There are several types of registers on the MAP-CA digital signal processor. These include system registers, breakpoint registers, general purpose registers, predicate registers, and special purpose 128-bit registers.

1.1.2.1 Global Registers

Global registers on the MAP-CA DSP consist of system registers and implementation-dependent I/O registers (PIO registers). Dedicated operations manipulate the system registers; conventional load and store operations manipulate the I/O registers.

1.1.2.2 Breakpoint Registers

MAP-CA DSP has two sets of breakpoint registers: instruction-breakpoint and data-breakpoint registers. These registers provide hardware breakpoint capability for various debugging tools. Instruction-breakpoint registers cause an exception when an operation in the specified address is about to be executed. Similarly, the data-breakpoint registers cause an exception when the data at the specified address is about to be accessed. In both cases, a mask can be used to specify a range of addresses.

By registering an exception handling routine associated with either of these exceptions, a software developer can control what happens when a hardware breakpoint occurs. For example, the exception handling routine may be used to signal an external application such as a source-level debugger that a breakpoint has occurred.

1.1.2.3 General Registers

There are 128 32-bit registers that can be treated as 64-bit general registers using even-odd pairs of the 32-bit registers.

1.1.2.4 Predicate Registers

There are 32 1-bit predicate registers. Predicate registers are used in predicated operations, logical operations, and branches. They provide a destination for operations with a judged condition.

1.1.2.5 PLC/PLV 128-bit registers

The IG-ALU has eight special 128-bit registers – two pairs of Partitioned Local Constant (PLC) registers and two pairs of Partitioned Local Variable (PLV) registers. These registers are used for powerful SIMD digital signal processor partitioned operations. The registers can be configured as sixteen 8-bit operation partitions, eight 16-bit operation partitions, or four 32-bit operation partitions. For numerous digital signal processing and compression algorithms, this allows MAP-CA DSP to match the cost/performance of fixed-function chips without the loss of re-programmability.

1.2 Interrupts and Exceptions

The MAP-CA DSP has a flexible interrupt structure. Interrupts and exceptions internal to the core are reflected directly in system registers. All other interrupts from on-chip devices and PCI interrupts from external devices are gathered by an on-chip interrupt controller. The interrupt controller also provides a number of software interrupts.

Routing, masking, and prioritization of interrupts is completely software programmable. Each of the interrupts handled by the interrupt controller can be individually masked, or routed to one of four core interrupts or to one of two PCI interrupt signals.

1.2.1 Core Interrupts and Exceptions

Table 1-1 and Table 1-2 list the events that can trigger interrupts or exceptions within the core. When an event occurs, a bit is set in an “Event Seen” system register. If the event is not masked (or not maskable), the address for a handler will be fetched from one of nine Event Vector system registers, depending on the event.

Table 1-1: System Events

Name	Event	Maskable
IO0..IO3	I/O interrupts (from interrupt controller)	Yes
SINT0..SINT1	Software interrupts	Yes
FCNT	Free running counter overflow	Yes
INTV0..INTV1	Interval timers	Yes
ILPC	Illegal program counter	No
IBPT	Instruction address break	Yes
BPOP	Breakpoint operation	No
SYS	System call (trap instruction)	No
ITLBAA	ITLB application access	No
ITLBR	ITLB reference	No
ITLBM	ITLB miss	No

Table 1-2: Operation Events

Name	Event	Maskable
ILLO	Illegal operation	No
PLV	Privilege violation	No
DBPT	Data address break	Yes
DALN	Data alignment error	No
DTLBKW	DTLB kernel write	No
DTLBAW	DTLB application write	No
DTLBAA	DTLB application access	No
DTLBR	DTLB reference	No
DTLBM	DTLB miss	No

1.2.2 Interrupt Controller

The MAP-CA digital signal processor interrupt controller supports multiple maskable interrupts from outside of the core. Non-core interrupt sources include on-chip devices such as TCI, the DRC, the

DataStreamer DMA Controller, and PCI interrupts from external devices or hosts. Software-generated shoulder-tap interrupts are provided for multiprocessing or inter-process communication support.

MAP-CA DSP interrupts can be examined and controlled via PIO registers in the ROMCON control block. Routing and masking of interrupts is programmable. Each interrupt can be individually masked or routed to one of four core interrupts or to one of two PCI interrupt signals. Software interrupts can be similarly masked and routed. They may be asserted or de-asserted under software control.

Table 1-3 shows the supported interrupts.

Table 1-3: Supported Interrupts

Name	Interrupt
IrqAlwaysOne	debug interrupt, always asserted
IrqIIC	I^2C
IrqTCI0	primary TCI
IrqDRC	display refresh controller
IrqNTSCIn0	primary ITU-R BT.601/656 in
IrqNTSCIn1	secondary ITU-R BT.601/656 in
IrqTCI1	secondary TCI
IrqPCIAA	PCI interrupt pin A
IrqPCIAB	PCI interrupt pin B
IrqNTSCOut	ITU-R BT.601/656 output
IrqIEC958	IEC958 audio
IrqIIS	I^2S audio
IrqPCIAPME	PCIA power management event
IrqDS0	DataStreamer interrupt 0
IrqDS1	DataStreamer interrupt 1
IrqDSTLB	DataStreamer TLB miss
IrqDSBufOvrFlow	DataStreamer I/O input overflow
IrqSoftWare	Software-controlled interrupts

1.3 Timers

The MAP-CA digital signal processor has two independent programmable interval timers plus a free-running counter. Each interval timer has a 32-bit counter register and period register. The counter is incremented once per cycle. When the counter reaches the period value, the counter is reloaded, a bit is set in the system Event Seen Register (ESR), and a maskable interrupt is asserted. The free-running counter counts up once per cycle as well. When it overflows to zero, a bit is set in ESR and a maskable interrupt is asserted.

The transport channel interface also has a programmable timer that counts at a rate of 27 MHz and can be used to generate an interrupt upon rollover.

1.4 Memory Hierarchy

The MAP-CA DSP supports several on-chip memories and access to SDRAM and other memories via the PCI bus. The VLIW is equipped with a 32 KB instruction cache and 32 KB data cache used for caching instructions and data from SDRAM. In addition to supporting I-ALU ports, the data cache supports a port to the DTS (Data Transfer Switch), which makes data in the data cache available to the DataStreamer controller.

A 4 KB instruction memory and a 4 KB data memory are used by the VLx coprocessor. The Video Filter uses a 6 KB line buffer memory. These memories, totaling 14 KB, are also accessible by the VLIW core through un-cached load/store operations. In addition, these memories are also available to the DataStreamer DMA controller and for external use via PCI. The line buffer memory is used to store the content of Flash ROM at system boot up.

1.4.1 Caches

The MAP-CA DSP has a 32 KB instruction cache and a separate, multi-bank 32 KB data cache. Both caches are physically addressed, so that problems of aliasing and context switching do not arise. For fast address translation, the cache index is virtual but the tags are physical.

The instruction cache holds instructions in a compressed form. It is organized as a two-way set associative cache with a LRU replacement algorithm.

The data cache is a 32 KB, four-way set-associative (with true LRU replacement), write-back cache. The data cache supports four simultaneous 64-bit data accesses per cycle. The cache is non-blocking; up to 8 outstanding misses to different cache lines and up to 48 outstanding misses overall are allowed.

1.4.2 Address Translation

The MAP-CA DSP provides memory management support in the form of separate TLBs for the instruction stream, each I-ALU data access, and the DataStreamer DMA controller. The four TLBs

(ITLB, two DTLBs, and DSTLB) can be programmed independently.

The DTS-ID is part of the virtual address and can be used to direct accesses when the TLBs are disabled.

Each TLB has sixteen fully-associative entries. Each entry contains a Virtual Page Number (VPN), an 8-bit Address Space Identifier (ASID), access protection bits, and page size information. Each entry can map a page of any valid size, where the valid sizes are 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, 256 MB, and 1 GB.

When a TLB miss occurs, an exception is generated. The exception handler can modify a TLB entry and retry the failed operation. Separate exception handlers can be installed for data, instruction, and DataStreamer controller TLB misses.

1.5 Databuses and Controllers

The various buses and controllers on the MAP-CA digital signal processor are described in the following sections.

1.5.1 Memory Interface Controller

The Memory Controller Unit allows customers to easily build high-performance, external memory up to 128 MB using SDRAM/SGRAM without any external glue logic. Local memory supports externally initiated PCI accesses through the Address Translation Unit within the PCI module.

The Memory Controller Unit also includes hardware that queues, prioritizes, and transfers data from memory to memory or from memory to cache asynchronously to the initiating software.

The on-chip core PLL generates the clock for the memory controller and provides clock synchronization between the MAP-CA DSP and external SDRAM. This provides support for various combinations of CPU core and memory speeds.

1.5.2 Data Transfer Switch (DTS)

The DTS is a split-transaction bus. The DTS contains the data and address buses, a high speed bridging system, and a bus arbiter. The bridge, arbiter, and bus arrangement is a very high-speed communication solution that allows multiple media applications to be executed concurrently.

The arbiter can handle multiple requestors using priority based scheduling.

1.5.3 DataStreamer DMA Controller

The DataStreamer DMA controller is a high performance, programmable DMA engine that performs buffered data transfer between different MAP-CA DSP memory subsystems or between memories and I/O devices. The DataStreamer controller is programmed and controlled by software. The DataStreamer controller then performs the requested transfer without further intervention from the core.

The DataStreamer controller can perform the following classes of transfers:

- memory-to-memory: perform block transfers, preload data into the cache, fill a memory region with 0 or 1 bits
- memory-to-I/O and I/O-to-memory: perform I/O transfers

The DataStreamer DMA controller features include:

- an 8 KB internal memory that can be partitioned into as many as 64 variable-sized buffers. Each buffer is simultaneously the sink for an input I/O or memory channel and the source for an output I/O or memory channel.
- sixty-four independent programmable channels for transfers between various memories and the DataStreamer controller's internal buffer,
- Channel programs, called Descriptor Lists, allow transfers of arbitrary or infinite length to be specified. Regular and irregular patterns of contiguous or non-contiguous transfers are easy to specify.
- Memories that can be read or written include SDRAM, on-chip memories, and PCI bus accessible memories. Cache preloading can also be performed.
- Interrupts can be triggered by descriptors, allowing end-of-transfer or mid-stream interrupts to be generated.

1.5.4 PCI Bus

The PCI unit implements a 32-bit PCI 2.1 interface with speed up to 66 MHz. The PCI interface is a single function device with two BARs. Certain fields in the configuration registers may be initialized on power-up through ROM control. As a PCI target, the PCI interface allows access to the MAP-CA digital signal processor SDRAM (coherently or non-coherently with respect to the data

cache). The PCI interface also allows access to several programmer-visible control registers, PIO space and SDRAM. As a PCI master, the PCI interface allows the VLIW core, the DataStreamer DMA controller, and coprocessors to initiate PCI bus requests. The PCI unit can initiate memory, I/O and configuration commands on the PCI bus.

The MAP-CA digital signal processor can act as a host on the PCI bus. There are three pairs of request/grant lines for other devices on a PCI bus. This enables a multi-processor configuration to connect up to four MAP-CAs together on a PCI bus without a bridge.

The PCI interface implements two separate interrupt lines. If the MAP-CA DSP is not the host, any internal interrupt can be routed to any of these PC interrupts. If the MAP-CA DSP is the host, the PCI interrupts are sampled by the MAP-CA DSP and can be routed to the MAP-CA DSP VLIW core.

The MAP-CA DSP is a 3.3V-only I/O device. If the MAP-CA DSP is used in a system with a 5V PCI bus architecture, then a 5V-to-3.3V level translator is required.

1.5.5 I/O Bus

All on-chip peripheral devices are connected via the internal I/O Bus (IOB). This is a 32-bit internal bus running at one half of the VLIW core frequency. The IOB connects to the DTS through the DataStreamer controller. The IOB can handle real-time requests.

1.6 Coprocessors

Coprocessors on the MAP-CA DSP help off-load "serial" tasks from the VLIW core or accelerate special purpose processing for video operations. The coprocessors operate in parallel with the VLIW core resulting in improved video processing.

1.6.1 VLx

The Variable Length Encoder/Decoder (Figure 1-2) or VLx is a 16-bit RISC coprocessor with thirty-two 16-bit registers. The VLx off-loads the bit sequential tasks of variable length encoding and variable length decoding (VLE/VLD) from the VLIW CPU core and accelerates applications such as JPEG, MPEG, H.263, JBIG, and DV. The VLx includes special purpose hardware for bitstream processing, hardware-accelerated MPEG-2 table lookup, and general purpose variable length decoding.

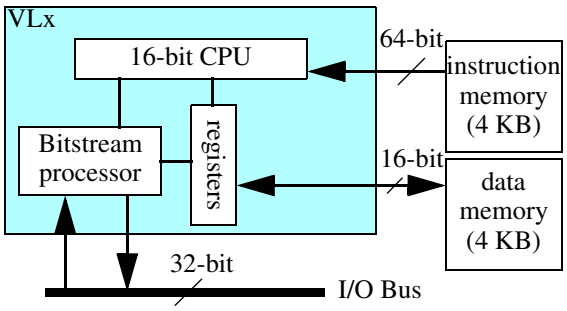


Figure 1-2: The VLx Coprocessor

1.6.2 Video Filter

A polyphase (8 phase) 2D Video Filter takes 4:2:0 or 4:2:2 YUV stream as input and scales either up or down as required. 4 (vertical) × 5 (horizontal) filters support up to 768 horizontal pixels, 3 × 5 up to 1024 horizontal pixels, and 2 × 5 up to 1536 horizontal pixels. The Video Filter pumps out scaled 4:4:4 YUV data to the DRC through the video bus. The Video Filter can also pump out 4:4:4 YUV data to the SDRAM for debug purposes. Its features are described below.

- Supports 8-bit coefficients.
- Supports both interspersed and co-sited pixel positioning.
- Supports vertical 4-tap polyphase (8-phase) filters for luminance and chrominance.
- Supports horizontal 5-tap polyphase (8-phase) filters for luminance and chrominance.
- Can scale up to a maximum resolution of 2047×2047 (depends upon memory bandwidth available for the video scaling operation).
- Can scale up from a minimum resolution of 17×4.
- The maximum scale down ratio is 1:7.

1.6.3 DES Module

The MAP-CA digital signal processor includes hardware support for encryption and decryption of data according to the *National Bureau of Standards Data Encryption Standard* and certain implementations thereof as defined in *FIPS Publications 46-2, 46-3, 74, and 81* and *ANSI Publication X9.52-1998*. For more information on this support, contact your Equator Technologies or Hitachi Sales Representative.

1.7 I/O Interfaces

1.7.1 Audio Interfaces

1.7.1.1 IEC958 Audio Interface

This interface supports several audio standards:

- Sony/Philips Digital Interface (S/PDIF)
- Audio Engineering Society/European Broadcast Union (AES/EBU) interface
- TOSLINK interface (requires external IR devices)

The MAP-CA DSP IEC958 interface can insert even or odd parity on each sub-frame of the output bit stream.

1.7.1.2 I^2S Interface

The Inter-IC Sound (I^2S) interface drives high quality audio D/A converters for home theater. The MAP-CA digital signal processor interface meets the requirements of the standard serial data protocol and provides connection for up to three stereo DACs and one ADC. The interface supports 48 kHz, 44.1 kHz, and 32 kHz audio sample rates. Simultaneous input and output must be at the same sample rate. The MAP-CA DSP IIS supports both master and slave mode interface. In slave mode there is the choice of using either external inputs or internally generated signals for the sample rate clock and serial bit clock.

1.7.2 Video Interfaces

The MAP-CA DSP provides two video input ports and one video output port. Each input port supports either transport channel interface input or ITU-R BT.601/656 input. The output port supports an ITU-R BT.601/656 compliant output.

In addition, the primary video input port and/or the output port can be used in a general purpose mode for transferring data (general purpose data port) for input or output respectively.

1.7.2.1 Transport Channel Interfaces

The video input unit implements two DVB compliant transport channel interfaces which receive demodulated channel data in transport layer format. The transport channel interface (TCI) accepts MPEG-2 system transport packets in either byte parallel or, by default, bit serial form. Data rates up to 80Mbps (serial) or 30 MB/s (byte-wide parallel) are supported. By default, serial data is input on `tci_data[0]` and parallel data is input on `tci_data[7:0]` with bit 7 the most significant. These orientations can be reversed by PIO programming.

The TCI synchronizes packet data received in broadcast applications such as satellite or cable. The TCI can detect inline sync bytes, which are the first byte of every transport header. Alternatively, the TCI can utilize the external `tci_sync` signal. Once byte-sync has been detected, the TCI moves byte-aligned data into the MAP-CA DSP's memory using the DataStreamer DMA controller.

The number of bytes in each packet is programmable. At the end of every packet, the TCI appends an eight-byte postscript that includes time stamps from the local clock counters. This information can be used in conjunction with the Program Clock References embedded in the transport stream to track the timing reference. This is accomplished by using a software loop filter to implement a 1-bit sigma-delta modulator to provide a controlling voltage for the external VCXO that drives `pclk`. The sigma-delta data stream is output at 1.5 MHz on the `tci_vdac` pin via the primary TCI.

In addition to the local clock counters, there is a programmable 27 MHz timer in each TCI module that generates an interrupt on overflow (rollover).

1.7.2.2 ITU-656 Input Interface

This interface provides direct connection to an ITU-R BT.601/656 format NTSC/PAL video input decoder. The external decoder can be controlled using the I^2C Serial Bus.

1.7.2.3 ITU-656 Output Interface

A glueless interface to a NTSC/PAL video encoder is provided, enabling the MAP-CA digital signal processor to directly generate high-quality NTSC or PAL video-output signals. This interface supports 8-bit 525 and 625 line resolutions with either separate H/Vsync (ITU-R BT. 601) or inline sync (ITU-R BT.656). Advanced video post-filtering on the MAP-CA DSP processor via software can produce flicker-free output when converting interlace-to-progressive output. The external NTSC/PAL encoder can be controlled using the I^2C Serial Bus.

1.7.2.4 General Purpose Data Port (GPDP)

The general purpose data port provides an 8-bit parallel input/output port. Together with a clock and a

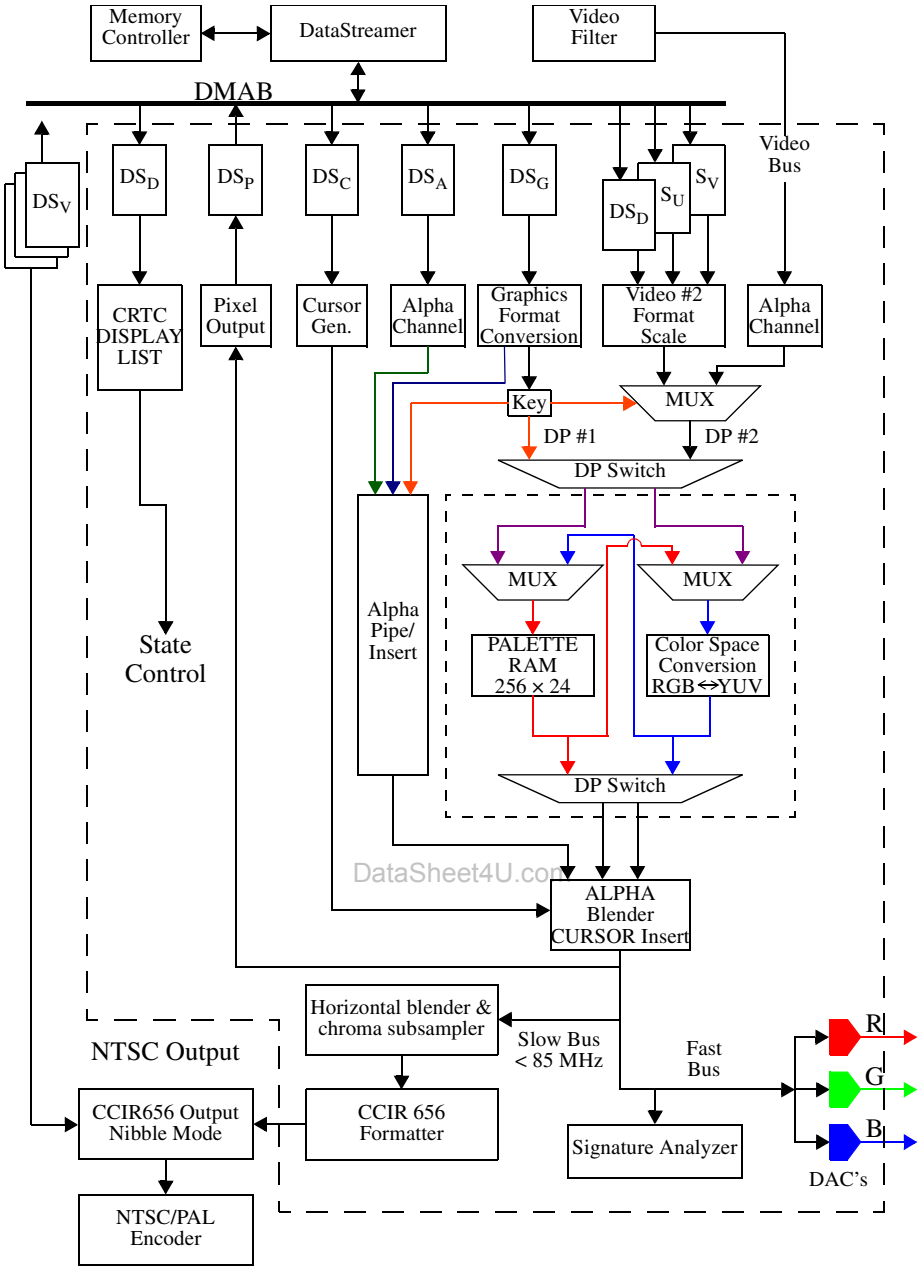


Figure 1-3: Display Refresh Controller

couple of handshake signals, this provides an alternative to PCI for multiple MAP chips to communicate. The data bandwidth supported is up to 60 MB/s depending upon other system activity.

1.7.3 Display Refresh Controller

Sophisticated video blending, 2D graphics with alpha blending, PIP, and hardware cursor overlays for EPGs (Electronic Program Guides) and navigation services have been designed into the Display Refresh Controller. Color space conversion, Gamma correction, and choice of YCbCr or RGB output format is supported. See Figure 1-3 on page 9.

The DRC supports a maximum screen resolution of 1280 × 1024. This monitor resolution requires a minimum pixel clock frequency of 108 MHz to support a rate of 16 bits per pixel.

1.7.4 DACs

The MAP-CA DSP RGB DACs (digital-to-analog converters) are part of the Display Refresh Control-

ler block. The 8-bit DACs allow pixel clock rates up to 110 MHz. The MAP-CA DSP generates RS-343A compatible monitor signals into doubly-terminated 75 Ω load and is capable of driving standard SVGA monitors.

The full scale output level is determined by an external reference voltage V_{ref} at 1.235V and an external resistor $R_{nominal}$ = 1117 Ω. The full scale level can be adjusted by adjusting the resistor value.

The DACs output the three primary analog color signals – red video, green video and blue video – with the video sync information superimposed on the green video output. Also, separate `hsync` and `vsync` reference signals are provided.

1.7.5 I²C Interface Unit

The Inter-IC (I^2C) bus was originally developed by Philips to facilitate communications and control among integrated circuits in consumer electronics. Using this two-wire serial interface, the MAP-CA DSP can function as a master or slave device to relay status and control information to external devices.

The I^2C interface unit has an additional output signal, `iic_select` that allows MAP-CA DSP software to control an external analog multiplexer/level converter that can switch between a regular I^2C bus and any other external bus (such as DDC for a monitor interface). This signal can also be used as a general purpose output.

1.7.6 ROM Controller

The ROM Controller (ROMCON) unit performs four distinct functions.

- The Chip Configuration and ROM Boot Sequencer is a state machine for reading chip configuration and boot code at system startup.
- The Flash ROM Interface controls the actual reading and writing of an off-chip flash ROM device.
- The Interrupt Controller/Collector provides a means for enabling, setting, and clearing hardware and software interrupts to the VLIW core and PCI bus controller.
- The PLL I/O provides PIO access to the programmable registers related to the various on-chip PLLs. The three PLLs for the core/SDRAM, pixel, and audio clocks are programmed indirectly via PIO registers within the ROMCON unit.

The purpose of the Configuration/Boot Sequencer is to control the boot up process of the chip. During reset, the resistor straps connected to the `ntsc_out_data[7:0]` pins are examined to determine how MAP-CA digital signal processor will configure itself and boot. If the resistor straps indicate to boot from ROM, the Boot Sequencer directs the Flash ROM Interface Controller to transfer bytes from the external ROM device to the MAP-CA DSP configuration registers and to the PCI configuration registers. The 6 KB line buffer memory of the Video Filter is then used to store the bootstrap program for system boot up. ROMCON copies the next 6 KB from ROM into the Video Filter memory (VfMem) through an 8-bit configuration bus. After the boot code has been loaded, ROMCON unstalls (restarts) the VLIW CPU, which in turn begins to execute the boot code out of VfMem. The ROMCON unit operates at 27 MHz during the configuration loading, since the core PLL cannot be programmed to be taken out of bypass mode until after the VLIW core has been unstalled.

Alternatively, for booting via the PCI interface, ROMCON plays a mostly passive role. In this case, an external host loads the VfMem with boot code and initiates boot of the VLIW core via a PIO write to unstall the VLIW CPU.

ROMCON also runs power-on diagnostics during the boot and may be paused at various points for status testing. ROMCON requires minimal chip resources so that standard power-on diagnostics can run without having to bring up all portions of the chip, allowing the chip to be tested in more manageable stages.

1.7.7 Reset Strap

During reset, the eight `ntsc_out_data` pins are used as inputs to read pre-boot configuration settings. These are settings that must be known before the actual boot process begins – namely, whether the system should boot from ROM and whether PCI should serve as host for its bus. There are also four straps available whose meaning can be defined in software.

Each pin strap is pulled high (to Vdd33) or low (to GND) through a 4.7 KΩ resistor. The pins are sampled into flip-flops until reset is de-asserted and then saved in the software-visible StrapBits field of PIO register ConfigBusControl. For more information see Section 4.8.6, “Reset Straps,” on page 27.

Chapter 2 Software Development

The iMMediaTools software toolkit includes

- iMMediaC optimizing, parallelizing C-language compiler
- FIRtree Media Intrinsic C-language extensions
- Assembler
- Linker
- Source-level debugger
- Assembly-level debugger
- Profiling, translating simulator
- Two virtual-machine simulators, one nearly cycle-accurate
- Assorted libraries

The iMMediaC compiler supports development in a host environment that differs from the target environment. The virtual-machine simulators allow testing and debugging on your host system. The supported host development environments are Microsoft Windows NT and Red Hat Linux.

2.1 The C Compiler

The MAP-CA digital signal processor development system includes the iMMediaC compiler with FIRtree Media Intrinsic extensions. The FIRtree extensions are proprietary SIMD-style high-speed media processing extensions.

The iMMediaC compiler uses aggressive optimization and global scheduling technology (including trace scheduling) to deliver full hardware performance without using laborious assembly language programming. The compiler allows programmers to focus efforts on algorithm optimization versus assembly scheduling, resource allocation, and debugging.

Unlike existing DSPs or dedicated-function devices which have heretofore been used to meet media processing requirements, the MAP-CA DSP is programmed in a high-level language (C). Benefits of programming in C include

- Reduced development costs
- Reduced time to market
- Lower system costs
- Reduced maintenance time
- Software-based upgrades

The compiler uses complex inline expansion, assertions, and loop unrolling with trace frequency estimation algorithms to maximize C code efficiency. The optimizations include

- Uncover instruction-level parallelism
- Manage registers, pipelines and functional units
- Generate instruction operation schedules that exploit parallelism
- Support extensive global optimization, analysis and scheduling
- Provide local scheduling and optimization
- Support media-oriented machine facilities
- Manages all timing dependencies to maximize scheduling efficiency

The iMMediaC compiler shell program lets you compile, examine, test, profile, assemble, and link source programs with a single command, by using various options.

2.1.1 The FIRtree Media Intrinsics Extensions

The FIRtree Media Intrinsics C-language extensions read 128-bit words of data memory, which contain multiple data items, and perform operations simultaneously on each of the items within the word. The FIRtree Media Intrinsics extensions perform operations on partitioned native data types within 32-bit or 64-bit operands, making use of the PLV and PLC registers on the IG-ALU to store intermediate values.

2.2 Libraries

The iMMediaTools Software Development Toolkit includes standard C runtime libraries and libraries specifically designed to support MAP-CA digital

signal processor resources, such as the DataStreamer DMA controller and VLx coprocessor for media applications.

2.3 Assembler

The MAP-CA DSP assembler lets the programmer take the assembly language source files generated by the compiler, and convert them into object code files, ready for the linker. Developers will not typically write assembly language modules themselves.

2.4 Linker

The linker combines object code files into an executable module, accepting both object files and libraries as input. During linking, the linker resolves all external references.

2.5 Debugger

The development environment includes a source-level debugger based on gdb (GNU debugger). The extended gdb (egdb) runs on both the Windows NT and Red Hat Linux platforms. The egdb debugger allows the user to:

- load a MAP-CA DSP application from the host PC file system onto the MAP-CA DSP and run it
- set, list, and clear software and hardware breakpoints
- single step through both C source code and assembly instructions
- source level debug of optimized C code
- examine and deposit values into local variables, global variables and PIO space
- examine and deposit values into all registers
- examine the stack, including stack backtracing

Numerous freeware or low-cost gdb GUI front ends exist on both the Windows NT and Linux platforms that will transparently layer on egdb's command line interface and provide a window-based debugging environment.

2.6 Simulators

The software developer's toolkit includes three software simulators: trsim, sim, and casim.

Trsim is a high speed, instruction level simulator of the MAP-CA digital signal processor core unit. This simulator works on an intermediate representation of a software program and can be used to initially develop applications and experiment with the performance of different algorithms and use of compiler options.

Sim is also a high-speed, instruction-level simulator. This simulator works off actual MAP-CA DSP binaries. Sim is a functional simulator of the MAP-CA DSP core unit with data cache, DataStreamer controller, and a subset of I/O devices. It provides runtime checks against resource constraints and all MAP-CA DSP features necessary to simulate a MAP-CA DSP running a real-time operating system and applications.

Casim is a nearly cycle-accurate software simulator for the MAP-CA DSP and models more accurately the core, DataStreamer DMA controller, VLx, instruction and data caches, memories, and buses. Like sim, this simulator operates off actual MAP-CA digital signal processor binaries. Casim provides more detailed runtime checks against resource constraints. Casim provides visibility into internal machine state and bandwith and augments debugging and tuning of interactions between VLIW core, DataStreamer controller, and VLx programs.

Sim and casim work in conjunction with the source-level debugger.

2.7 Boot

Software must contain boot code for execution on MAP-CA DSP. This boot code configures TLBs and caches. Equator software tools can automatically add boot code when building an application.

Chapter 3 BGA PIN_OUT Assignments

Signal assignment on the BGA352 package is shown here. Figure 3-1 shows the bottom view, with the balls facing the viewer. Figure 3-2 shows the top view of the chip with pin assignments..

In Table 3-1, pins marked with an (b) have multiple functions assigned (see Chapter 4)

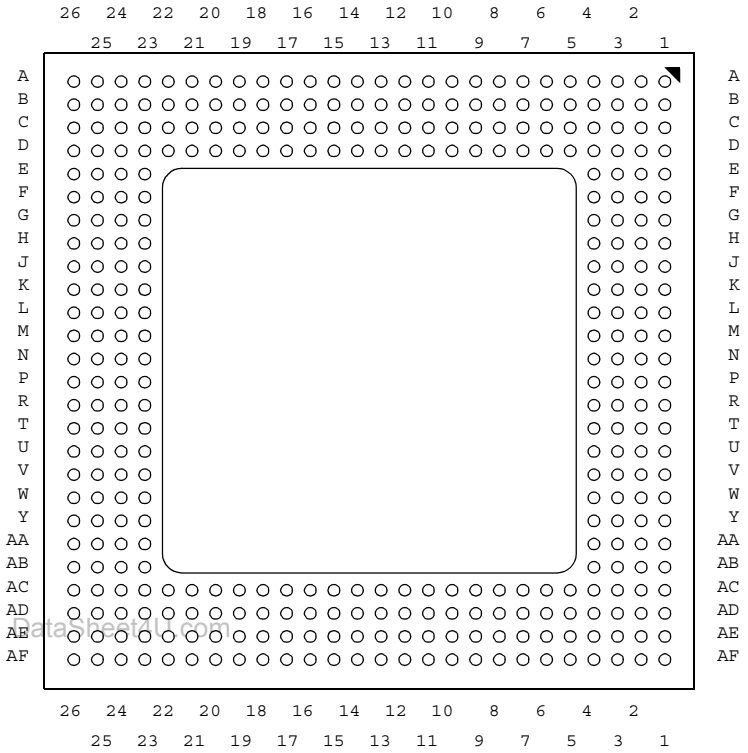


Figure 3-1: View of balls from the bottom

Table 3-1: Pin Assignments

Signal Name	Ball
audioclk_byp_in	A2[a]
aVdd18	B3
aVss	C4
aVdd18	D5
aVss	A3
pixelclk_byp_in	B4[b]
ntsc_out_data[3]	C5[b]
ntsc_out_data[4]	B5[b]
ntsc_out_data[5]	A4[b]
ntsc_out_data[6]	C6[b]
ntsc_out_data[7]	D7[b]
video_ina[0]	B6[b]
video_ina[1]	C7[b]
video_ina[2]	D8[b]
video_ina[3]	A6[b]
video_ina[4]	B7[b]
video_ina[5]	A7[b]
video_ina[6]	C8[b]
video_ina[7]	D9[b]
video_ina[8]	B8[b]
video_ina[9]	C9[b]
tcia_inuse	A8
tcia_sync	A9
tcia_clk	C10
tcia_vdac	B10
ntsc_ina_clk27	A10[b]
video_inb[0]	C11[b]
video_inb[1]	B11[b]
video_inb[2]	A11[b]
video_inb[3]	D12[b]
video_inb[4]	C12[b]
video_inb[5]	B12[b]
video_inb[6]	A13[b]
video_inb[7]	C13[b]
video_inb[8]	D13[b]
video_inb[9]	B13[b]
tcib_inuse	A14
tcib_sync	B14
tcib_clk	C14
ntsc_inb_clk27	D14
vsync	A16
hsync	B15
tms	B16
trst	C15
aVss	A17
gdac_fscale	B17
gdac_comp	C16
aVdd33	D16
gdac_green	C17
gdac_blue	A18
gdac_red	A19
gdac_cvgg(aVss)	C18

Signal Name	Ball
aVddx (aVdd18)	D17
aVssx (aVss)	B19
tdi	A20
tck	B20
tdo	C19
no connection	A21
sddata[0]	B21
sddata[1]	C20
sddata[2]	D19
sddata[3]	A23
sddqm[0]	B22
sddata[4]	C21
sddata[5]	A24
sddata[6]	B23
sddata[7]	C22
sddata[8]	D21
sddata[9]	A25
sddata[10]	B24
sddata[11]	C23
sddqm[1]	D22
sddata[12]	D24
sddata[13]	B26
sddata[14]	C25
sddata[15]	E24
sddata[16]	D25
sddata[17]	D26
sddata[18]	E25
sddata[19]	F24
sddqm[2]	F26
sddata[20]	G24
sddata[21]	G25
sddata[22]	H25
sddata[23]	H24
sddata[24]	H26
sddata[25]	J24

Signal Name	Ball
sddata[26]	J25
sddata[27]	K24
sddqm[3]	K26
sddata[28]	L24
sddata[29]	L25
sddata[30]	M25
sddata[31]	M24
sdcs_[0]	M26
sdcs_[1]	N24
sdcs_[2]	N25
sdcs_[3]	P26
sdrtnclk	P24
sdclk	R25
sdclk1	R24
sdclk2	T26
sdras_	T25
sdcas_	T24
sdwe_	U25
sdadr[0]	U24
sdadr[1]	V26
sdadr[2]	V24
sdadr[3]	W25
sdadr[4]	Y26
sdadr[5]	W24
sdadr[6]	Y25
sdadr[7]	Y24
sdadr[8]	AA25
sdadr[9]	AA24
sdadr[10]	AB26
sdadr[11]	AD26
sdadr[12]	AB24
sdadr[13]	AD25
sddata[32]	AC24
sddata[33]	AB23
aVss	AC22

Signal Name	Ball
aVssq (aVss)	AD23
aVddq (aVdd18)	AE24
aVdd18	AF25
sdclk_byp_in	AC21[c]
pclk	AD22[d]
coreclk_byp_in	AE23[c]
pci_clk	AF24
sddata[34]	AD21
sddata[35]	AF23
sddqm[4]	AF22
sddata[36]	AE21
sddata[37]	AC19
sddata[38]	AD20
sddata[39]	AF21
sddata[40]	AF20
sddata[41]	AC18
sddata[42]	AD19
sddata[43]	AE19
sddqm[5]	AD18
sddata[44]	AF19
sddata[45]	AE18
sddata[46]	AD17
sddata[47]	AE17
sddata[48]	AF17
sddata[49]	AD16
sddata[50]	AF16
sddata[51]	AC15
sddqm[6]	AD15
sddata[52]	AE15
sddata[53]	AF15
sddata[54]	AD14
sddata[55]	AE14
sddata[56]	AF13
sddata[57]	AD13

Signal Name	Ball
sddata[58]	AF12
sddata[59]	AE12
sddqm[7]	AD12
sddata[60]	AC12
sddata[61]	AF11
sddata[62]	AD11
sddata[63]	AF10
pci_ad[0]	AE10
pci_ad[1]	AD10
pci_ad[2]	AE9
pci_ad[3]	AF8
pci_ad[4]	AD9
pci_ad[5]	AE8
pci_ad[6]	AC9
pci_ad[7]	AD8
pci_cbe_[0]	AF7
pci_ad[8]	AF6
pci_ad[9]	AD7
pci_ad[10]	AC8
pci_ad[11]	AE6
pci_ad[12]	AF5
pci_ad[13]	AF4
pci_ad[14]	AD6
pci_ad[15]	AF3
pci_cbe_[1]	AE4
pci_par	AD5
pci_serr_intb_	AC6
pci_stop_	AF2
pci_devsel_	AE3
pci_trdy_	AD4
pci_irdy_	AC5
Vss	AD2
Vdd18	AE1
Vdd18	AC3
Vss	AB3

Signal Name	Ball
pci_frame_	AC2
pci_cbe_[2]	AC1
pci_ad[16]	AB1
pci_ad[17]	AA2
pci_ad[18]	AA3
pci_ad[19]	AA1
pci_ad[20]	Y3
pci_ad[21]	Y2
pci_ad[22]	W1
pci_ad[23]	W2
pci_idsel	W3
pci_cbe_[3]	V1
pci_ad[24]	V3
pci_ad[25]	U1
pci_ad[26]	U4
pci_ad[27]	U3
pci_ad[28]	U2
pci_ad[29]	T3
pci_ad[30]	T2
pci_ad[31]	R3
pci_req_[0]	R2
pci_req_[1]	R1
pci_req_[2]	P3
pci_gnt_[0]	P1
pci_gnt_[1]	N1
pci_gnt_[2]	N2
pclk_out	N3[e]
pci_rst_	M2
pci_inta_	M3
pci_pme_	L1
iic_sda	L2
iic_sck	L3
iic_select	K1
iis_in_data	K3
iis_in_lr	J1

Signal Name	Ball
iis_in_bclk	K4
iis_out_data[0]	J2[b]
iis_out_data[1]	J3[b]
iis_out_data[2]	H2[b]
iis_out_lr	G1
iis_out_bclk	H3
iec958_in	G2
iec958_out	G3
rom_cs_	F1
ntsc_out_hsync	F3[b]
ntsc_out_vsync	E1[b]
ntsc_out_data[0]	E2[b]
ntsc_out_data[1]	E3[b]
ntsc_out_data[2]	C1[b]
audioclk_out	C2
pixelclk_out	D3[f]
Vdd18	D6
Vdd18	D11
Vdd18	D15
Vdd18	D20
Vdd18	E23
Vdd18	G23
Vdd18	H23
Vdd18	K23
Vdd18	M23
Vdd18	P23
Vdd18	T23

Signal Name	Ball
Vdd18	V23
Vdd18	W23
Vdd18	AA23
Vdd18	AC20
Vdd18	AC16
Vdd18	AC11
Vdd18	AC7
Vdd18	AB4
Vdd18	AA4
Vdd18	W4
Vdd18	T4
Vdd18	P4
Vdd18	N4
Vdd18	M4
Vdd18	J4
Vdd18	G4
Vdd18	F4
Vdd33	C3
Vdd33	D4
Vdd33	E4
Vdd33	D10
Vdd33	D18
Vdd33	C24
Vdd33	D23
Vdd33	F23
Vdd33	J23
Vdd33	L23
Vdd33	N23

Signal Name	Ball
Vdd33	R23
Vdd33	U23
Vdd33	Y23
Vdd33	AD24
Vdd33	AC23
Vdd33	AC17
Vdd33	AC14
Vdd33	AC13
Vdd33	AC10
Vdd33	AD3
Vdd33	AC4
Vdd33	Y4
Vdd33	V4
Vdd33	R4
Vdd33	L4
Vdd33	H4
Vss	A1
Vss	B1
Vss	B2
Vss	A5
Vss	B9
Vss	A12
Vss	A15
Vss	B18
Vss	A22
Vss	A26
Vss	B25
Vss	C26

Signal Name	Ball
Vss	E26
Vss	F25
Vss	G26
Vss	J26
Vss	K25
Vss	L26
Vss	N26
Vss	P25
Vss	R26
Vss	U26
Vss	V25
Vss	W26
Vss	AA26
Vss	AB25
Vss	AC26
Vss	AC25
Vss	AE26
Vss	AE25
Vss	AF26
Vss	AE22
Vss	AE20
Vss	AF18
Vss	AE16
Vss	AF14
Vss	AE13
Vss	AE11
Vss	AF9
Vss	AE7

Signal Name	Ball
Vss	AE5
Vss	AF1
Vss	AE2
Vss	AD1
Vss	AB2
Vss	Y1
Vss	V2
Vss	T1
Vss	P2
Vss	M1
Vss	K2
Vss	H1
Vss	F2
Vss	D1
Vss	D2

a. If unused, NCi (Vss) and tie to ground

b. Multi-function pins

c. connect to 27 MHz or lower clock

d. connect to 27 MHz clock

e. If unused, NCo and floating

f. Leave floating

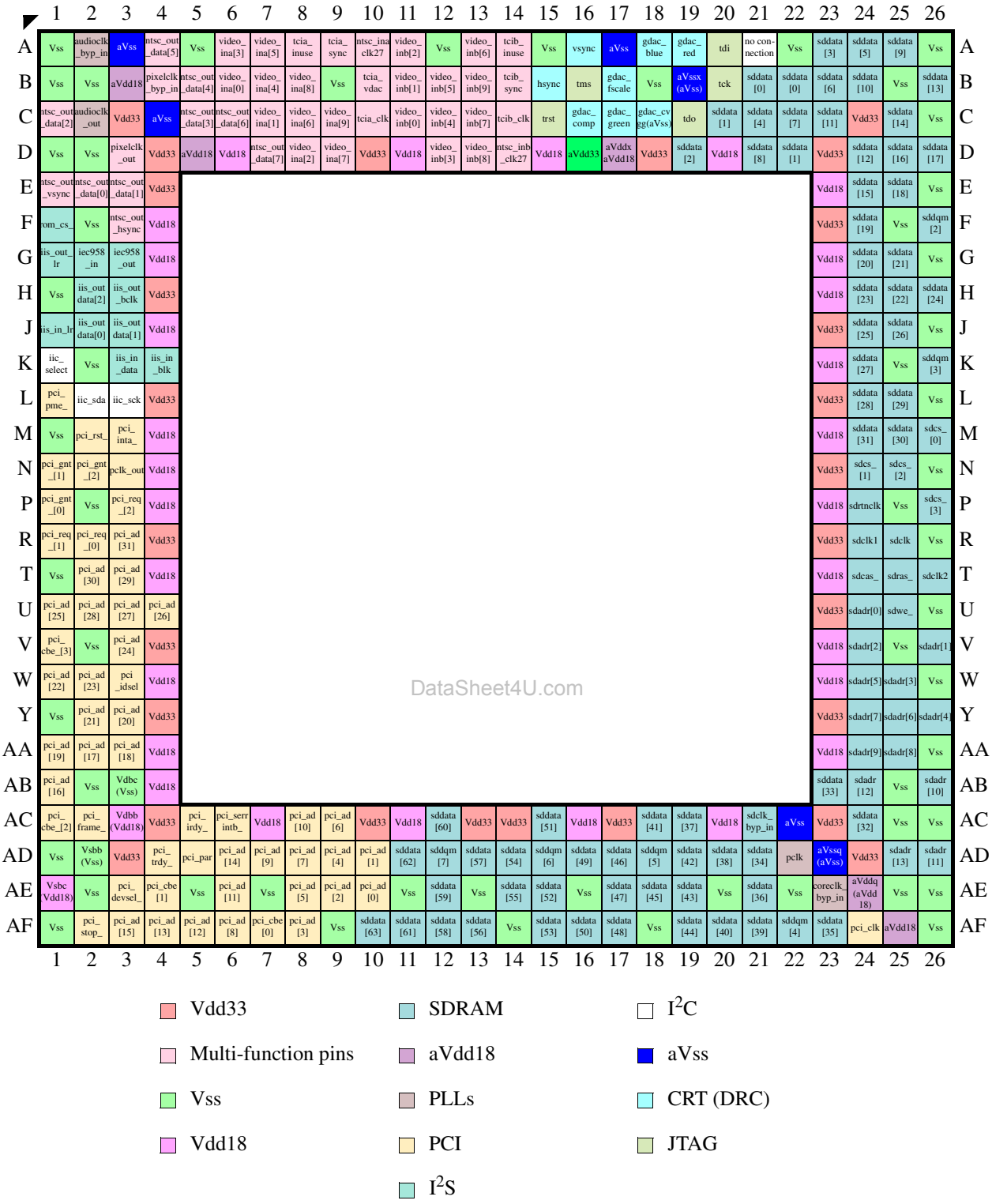


Figure 3-2: MAP-CA DSP pins viewed from top

Chapter 4 Signal Descriptions

4.1 Interface Summary

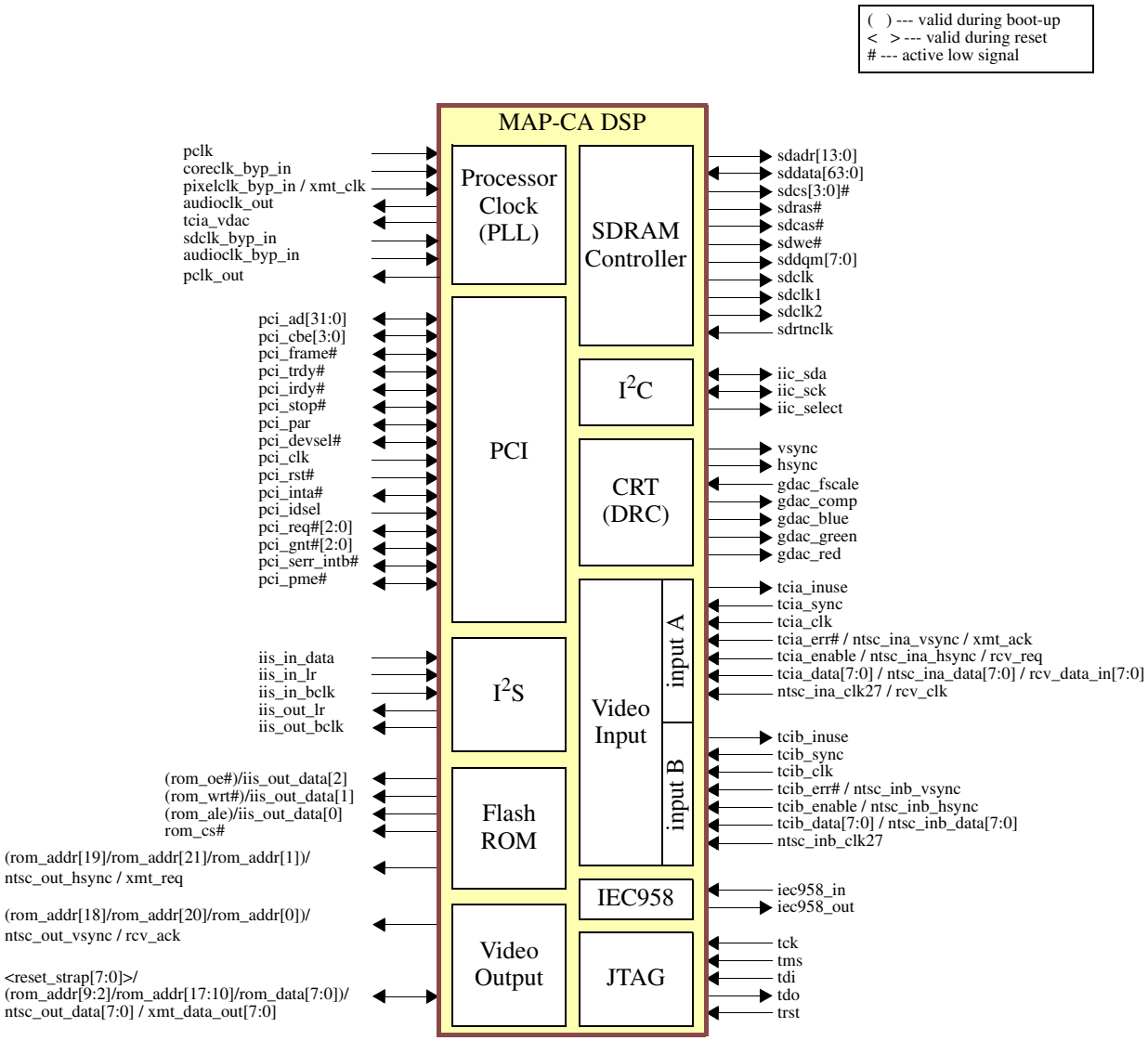


Figure 4-1: MAP-CA DSP Interface

4.2 Legend

All tables in this section use the following abbreviations:

A .....analog signal
B.....bi-directional
I.....input
O .....output
od .....open drain or active pull down
trailing "_" .....active low
().....parentheses indicate number of shared signal pins

4.3 Processor Clock

There is a single 27 MHz reference clock signal for generating internal clocks.

Signal	# of Pins	I/O	Description
pclk	1	I	27 MHz VCXO input that serves as the reference signal to the three on-chip PLLs. It is also a reference clock for the video output and the I^2C interface
coreclk_byp_in	1	I	Bypass input for the core clock
sdclk_byp_in	1	I	Bypass input for the SDRAM clock.
pixelclk_byp_in	1	I	Transmit clock for GPDP (xmt_clk) or PLL-bypass input for pixel clock
audioclk_byp_in	1	I	Bypass input for the audio clock.
pclk_out (coreclk_out)	1	O	Output for the core clock.
pixelclk_out	1	O	Output for the pixel clock.
audioclk_out	1	O	Audio clock output used for I^2S interface master MCLK
tcia_vdac	1	O	Sigma-delta output from software loop filter for controlling external VCXO for pclk
TOTAL	9		

Table 4-1: Processor Clock Signal Description

4.4 SDRAM

The MAP-CA DSP supports either SDRAM or SGRAM memory system using the signals shown in Table 4-2. The MAP-CA digital signal processor supports a memory system of 64-bit or 32-bit data width. The MAP-CA DSP supports DRAM widths of 8-bit, 16-bit or 32-bits.

Signal	# of Pins	I/O	Description
sdadr[13:0]	14	O	Address lines indicate row addresses when sdras_ is active and indicate column addresses when sdcas_ is active
sddata[63:0]	64	B	Data Input/Output lines transfer data between the memory and the MAP-CA DSP. These are also input mask bits for Write-per-Bit. When block write is activated, these lines provide column address mask
sdcs_[3:0]	4	O	Chip Select signal lines indicate that the command on the output lines is for each memory chip. If this signal is high, the output command(s) will be ignored by each corresponding memory chip
sdras_	1	O	sdras_ is part of the output command to the SDRAM/SGRAM
sdcas_	1	O	sdcas_ is part of the output command to the SDRAM/SGRAM
sdwe_	1	O	Write enable (sdwe_) is part of the output command
sddqm[7:0]	8	O	During read, sddqm=1 turns off the output buffers of SDRAM/SGRAM. During write, sddqm=1 prevents a write to the current memory location
sdclk,sdclk1,sdclk2	3	O	sdclk, sdclk1 and sdclk2 are driven by the MAP-CA DSP SDRAM clock. All SDRAM/SGRAM input signals are sampled on the positive edge of sdclk
sdrtnclk	1	I	sdrtnclk is driven by sdclk. This signal is used for latching the data from SDRAM/SGRAM
TOTAL	97		

Table 4-2: Memory Interface Signals

4.5 PCI Bus

The MAP-CA DSP provides the PCI bus as the primary system interface. Table 4-3 lists the PCI signals.

Signal	# of Pins	I/O	Description
pci_ad[31:0]	32	B	PCI multiplexed address and data lines. The address is driven when pci_frame_ is first asserted. Data is transferred on this bus in subsequent clocks.
pci_cbe_[3:0]	4	B	For PCI cycles, the bus command and byte enables are used to transfer the PCI command during the address phase and are used to transfer byte lane enables during subsequent data phases.
pci_frame_	1	B	Transaction framing for PCI transfers. The initial assertion indicates the address phase and the start of a PCI transaction. Continued assertion determines the burst size of the transaction.
pci_trdy_	1	B	The target ready signal is asserted when the PCI target is ready for a data transfer.
pci_irdy_	1	B	The initiator ready signal is asserted when the PCI master is ready for a data transfer.
pci_stop_	1	B	pci_stop_ is asserted by the target to request the master to stop the current transaction.
pci_par	1	B	A single parity bit is calculated over pci_ad[31:0], and pci_c_be[3:0] and transferred over this signal.
pci_devsel_	1	B	A target asserts the pci_devsel_ signal line to indicate it has decoded the address on the pci_ad[31:0] bus and will participate in (claim) the current transaction. The PCI bus master must monitor the pci_devsel_ signal line to determine if a target bus has claimed the transaction or if it will execute a Master Abort termination. pci_devsel_ will be tri-stated from the leading edge of pci_rst_. pci_devsel_ remains tri-stated until driven by the target.
pci_clk	1	I	pci_clk provides timing for all PCI transactions on the PCI bus. All other PCI signals are sampled on the rising edge of pci_clk, and all timing parameters are defined with respect to this edge. NOTE: The MAP-CA DSP core clock PLL does not use this clock as a core PLL reference clock.
pci_rst_	1	I	This signal indicates a reset of all PCI resources. In addition, the internal MAP-CA DSP CPU core, etc. are reset by the assertion of this signal. PCI pad cell drivers are disabled by the assertion of this signal, as specified in the PCI 2.1 document.

Table 4-3: PCI Interface Signals

Signal	# of Pins	I/O	Description
pci_inta_	1	B (od)	When the MAP-CA digital signal processor is not designated as the PCI bus "HOST", then this signal is the open drain output generating an asynchronous level sensitive interrupt on the PCI bus. The MAP-CA DSP pad cell does not contain a pull up for this signal. When the MAP-CA DSP is designated as the PCI bus "HOST" then this signal is an interrupt request input from PCI devices. The MAP-CA DSP sees and utilizes this interrupt.
pci_idsel	1	I	The initialization device select is used as a slot addressed chip select input during configuration read and write transactions. This signal is inactive in a self-hosted configuration.
pci_req_[2:0]	3	B	The assertion of pci_req_ in a non-self-hosted configuration indicates that the MAP-CA DSP desires the use of the PCI bus.
pci_gnt_[2:0]	3	B	The assertion of pci_gnt_ in a non-self-hosted environment indicates that the MAP-CA DSP has been granted the use of the PCI bus.
pci_serr_intb_	1	B (od)	This open drain output may generate either an asynchronous level sensitive interrupt or the PCI bus or optionally signal SYSTEM ERROR. See the MAP-CA digital signal processor configuration control register for the signal's current use. When the MAP-CA DSP is not designated as the PCI bus "HOST", then this signal is the open drain output generating an asynchronous level sensitive interrupt on the PCI bus. The MAP-CA DSP pad cell does not contain a pull up for this signal. When the MAP-CA DSP is designated as the PCI bus "HOST" , then this signal is an interrupt request input from PCI devices. The MAP-CA DSP sees and utilizes this interrupt.
pci_pme_	1	B (od)	When MAP-CA DSP is not in PCI host mode, this signal is an open drain output used to request a change in power management state. When MAP-CA DSP is in PCI host mode, this is an input signal to which PCI devices indicate changes in power management state.
TOTAL	54		

Table 4-3: PCI Interface Signals

4.6 IEC958

The MAP-CA DSP provides an IEC958 interface as shown in Table 4-4.

Signal	# of Pins	I/O	Description
iec958_in	1	I	Serial input line for IEC958 digital audio.
iec958_out	1	O	Serial output line for IEC958 digital audio.
TOTAL	2		

Table 4-4: IEC958 Interface Signals

4.7 I^2S

The MAP-CA DSP provides interfaces for I^2S digital audio input and output as shown in Table 4-5.

Signal	# of Pins	I/O	Description
iis_in_data	1	I	Serial data input
iis_in_lr	1	I	Select left/right channel in the serial input
iis_in_bclk	1	I	I^2S input bit clock
iis_out_data[2:0]	3	O	Serial output data (3 stereo lines)
iis_out_lr	1	O	Select left/right channel in serial output lines
iis_out_bclk	1	O	I^2S output bit-rate clock
TOTAL[a]	8		

Table 4-5: I^2S Interface Signals

a. audioclk_out, defined in Section 4.3 on page 18, serves as the output MCLK in master mode.

4.8 Multi-Function Signal Pins

Table 4-6 lists the pin name and pin number of the shared pins on the MAP-CA digital signal processor, along with the signal name associated with each mode-specific function.

Ball #	Pin Name	ITU-656 Mode	TCI Mode	GPDP Mode	ROM Boot Mode	Reset Mode
B4	pixelclk_byp_in	-	-	xmt_clk	-	-
C5	ntsc_out_data[3]	-	-	xmt_data_out[3]	rom_addr[5,13]/rom_data[3]	reset_strap[3]
B5	ntsc_out_data[4]	-	-	xmt_data_out[4]	rom_addr[6,14]/rom_data[4]	reset_strap[4]
A4	ntsc_out_data[5]	-	-	xmt_data_out[5]	rom_addr[7,15]/rom_data[5]	reset_strap[5]
C6	ntsc_out_data[6]	-	-	xmt_data_out[6]	rom_addr[8,16]/rom_data[6]	reset_strap[6]
D7	ntsc_out_data[7]	-	-	xmt_data_out[7]	rom_addr[9,17]/rom_data[7]	reset_strap[7]
B6	video_ina[0]	ntsc_ina_data[0]	tcia_data[0]	rcv_data_in[0]	-	-
C7	video_ina[1]	ntsc_ina_data[1]	tcia_data[1]	rcv_data_in[1]	-	-
D8	video_ina[2]	ntsc_ina_data[2]	tcia_data[2]	rcv_data_in[2]	-	-
A6	video_ina[3]	ntsc_ina_data[3]	tcia_data[3]	rcv_data_in[3]	-	-
B7	video_ina[4]	ntsc_ina_data[4]	tcia_data[4]	rcv_data_in[4]	-	-
A7	video_ina[5]	ntsc_ina_data[5]	tcia_data[5]	rcv_data_in[5]	-	-
C8	video_ina[6]	ntsc_ina_data[6]	tcia_data[6]	rcv_data_in[6]	-	-
D9	video_ina[7]	ntsc_ina_data[7]	tcia_data[7]	rcv_data_in[7]	-	-
B8	video_ina[8]	ntsc_ina_hsync	tcia_enable	rcv_req	-	-
C9	video_ina[9]	ntsc_ina_vsync	tcia_err#	xmt_ack	-	-
A10	ntsc_ina_clk27	-	-	rcv_clk	-	-
C11	video_inb[0]	ntsc_inb_data[0]	tcib_data[0]	-	-	-
B11	video_inb[1]	ntsc_inb_data[1]	tcib_data[1]	-	-	-
A11	video_inb[2]	ntsc_inb_data[2]	tcib_data[2]	-	-	-
D12	video_inb[3]	ntsc_inb_data[3]	tcib_data[3]	-	-	-
C12	video_inb[4]	ntsc_inb_data[4]	tcib_data[4]	-	-	-
B12	video_inb[5]	ntsc_inb_data[5]	tcib_data[5]	-	-	-
A13	video_inb[6]	ntsc_inb_data[6]	tcib_data[6]	-	-	-
C13	video_inb[7]	ntsc_inb_data[7]	tcib_data[7]	-	-	-
D13	video_inb[8]	ntsc_inb_hsync	tcib_enable	-	-	-
B13	video_inb[9]	ntsc_inb_vsync	tcib_err#	-	-	-
J2	iis_out_data[0]	-	-	-	rom_ale	-
J3	iis_out_data[1]	-	-	-	rom_wrt#	-
H2	iis_out_data[2]	-	-	-	rom_ole#	-
F3	ntsc_out_hsync	-	-	xmt_req	rom_addr[21,19,1]	-
E1	ntsc_out_vsync	-	-	rcv_ack	rom_addr[20,18,0]	-
22	ntsc_out_data[0]	-	-	xmt_data_out[0]	rom_addr[2,10]/rom_data[0]	reset_strap[0]
E3	ntsc_out_data[1]	-	-	xmt_data_out[1]	rom_addr[3,11]/rom_data[1]	reset_strap[1]
C1	ntsc_out_data[2]	-	-	xmt_data_out[2]	rom_addr[4,12]/rom_data[2]	reset_strap[2]

Table 4-6: Multiple Signal Pins

4.8.1 Transport Channel Interfaces (TCI)

The MAP-CA digital signal processor provides two parallel/serial TCI interfaces. See Table 4-7 and

Signal	# of Pins	I/O	Description
tcia_data[7:0]	(8)	I	TCI data input: All 8 bits of input are used in parallel mode. Only tci_data[0] is used in serial mode
tcia_enable	(1)	I	Transport channel enable: 1 = accept a TCI input sample 0 = ignore TCI input sample
tcia_inuse	1	O	Video input port external mux select. This pin can also be used as a general purpose output if dynamic muxing of the video input is not required.
tcia_sync	1	I	Demodulator/FEC has marked the synchronization point in the MPEG2 transport stream packet. The packet size is programmable.
tcia_err_	(1)	I	This active low signal indicates that the Demodulator/FEC has detected an uncorrectable error in the current packet.
tcia_clk	1	I	Transport channel clock
TOTAL	3(10)		

Table 4-7: Primary TCI Interface Signals

Table 4-8.

Signal	# of Pins	I/O	Description
tcib_data[7:0]	(8)	I	TCI data input: All 8-bits of input are used in parallel mode. Only tci_data[0] is used in serial mode.
tcib_enable	(1)	I	Transport channel enable: 1 = accept a TCI input sample 0 = ignore TCI input sample
tcib_inuse	1	O	Video input port external mux select. This pin can also be used as a general purpose output if dynamic muxing of the video input is not required.
tcib_sync	1	I	Demodulator/FEC has marked the synchronization point in the MPEG2 transport stream packet. The packet size is programmable.
tcib_err_	(1)	I	This active low signal indicates that the Demodulator/FEC has detected an uncorrectable error in the current packet.
tcib_clk	1	I	Transport channel clock
TOTAL	3(10)		

Table 4-8: Secondary TCI Interface Signals

4.8.2 ITU-656 Inputs

Analog video can be digitized according to ITU-R BT.601/656 via a NTSC, PAL or SVIDEO decoder and then input to the MAP-CA DSP. The interface signals for the primary and secondary video inputs are shown in Table 4-9 and Table 4-10.

Signal	# of Pins	I/O	Description
ntsc_ina_clk27	1	I	27MHz clock from video decoder
ntsc_ina_hsync	(1)	I	Horizontal sync
ntsc_ina_vsync	(1)	I	Vertical sync
ntsc_ina_data[7:0]	(8)	I	ITU-R BT.601/656 formatted video input stream
TOTAL	1(10)		

Table 4-9: Primary ITU-R BT.601/656 Input Interface Signals

Signal	# of Pins	I/O	Description
ntsc_inb_clk27	1	I	27MHz clock from video decoder
ntsc_inb_hsync	(1)	I	Horizontal sync
ntsc_inb_vsync	(1)	I	Vertical sync
ntsc_inb_data[7:0]	(8)	I	ITU-R BT.601/656 formatted video input stream
TOTAL	1(10)		

Table 4-10: Secondary ITU-R BT.601/656 Input Interface Signals

4.8.3 ITU-656 Output

The MAP-CA digital signal processor has a digital ITU-R BT.601/656 output interface as shown in Table 4-11.

Signal	# of Pins	I/O	Description
pclk	(1)	I	27MHz pixel clock from VCXO clock input. See Section 4.3.
ntsc_out_hsync	1	O	Horizontal sync
ntsc_out_vsync	1	O	Vertical sync
ntsc_out_data[7:0]	8	B	ITU-R BT.601/656 formatted NTSC/PAL output data configured as input only when used for ROM interface or reset strap
TOTAL	10(1)		

Table 4-11: ITU-R BT.601/656 Output Interface Signals

4.8.4 General Purpose Data Port (GPDP)

The primary video input port and the video output port can be coupled together to function as a general purpose 8-bit duplex data port.

Signal	# of Pins	I/O	Description
xmt_clk	(1)	I	transmitter output clock, shared with pixelclk_byp_in
xmt_req	(1)	O	GPDP on MAP-CA digital signal processor is ready to transmit data. Shared with ntsc_out_hsync
xmt_ack	(1)	I	output source is ready to accept data, shared with video_ina[9]
xmt_data_out[7:0]	(8)	O	Parallel data output on ntsc_out_data[7:0]
rcv_clk	(1)	I	Receiver input clock shared with ntsc_ina_clk27
rcv_req	(1)	I	Input source is ready to send data. Shared with video_ina[8]
rcv_ack	(1)	O	GPDP on MAP-CA DSP is ready to accept data, shared with ntsc_out_vsync
rcv_data_in[7:0]	(8)	I	Parallel data input on video_ina[7:0]
TOTAL	(22)		

Table 4-12: GPDP Interface Signals

4.8.5 Flash ROM

A Flash ROM (EEPROM) interface is provided on the MAP-CA digital signal processor to assist in boot-up. The Flash ROM is active during the boot up process and must be disabled through its chip-select signal. See Section 3.3.2, *Equator Hardware Reference Manual, Volume 4, MAP-CA I/O Interfaces* for information about programming the timing parameters of the ROM interface.

Signal	# of Pins	I/O	Description
rom_cs_	1	O	This pin is the chip enable signal.
rom_oe_	(1)	O	This active low signal is asserted on ROM read cycles. This signal is multiplexed with iis_out_data[2].
rom_wrt_	(1)	O	This active low signal is asserted on ROM write cycles. This signal is multiplexed with iis_out_data[1].
rom_ale	(1)	O	Address latch enable: rom_addr[9:2] and rom_addr[19:18] are latched on the falling edge, rom_addr[17:10] and rom_addr[21:20] are latched on the rising edge; this signal is multiplexed with iis_out_data[0].
rom_addr[19:18]/ rom_addr[21:20]/ rom_addr[1:0]	(2)	O	rom_addr[19]/rom_addr[21]/rom_addr[1] is muxed with ntsc_out_hsync. rom_addr[18]/rom_addr[20]/rom_addr[0] is muxed with ntsc_out_vsync.
rom_addr[9:2]/ rom_addr[17:10]/ rom_data[7:0]	(8)	B	ROM data and address bus. These signals are multiplexed with ntsc_out_data[7:0].
TOTAL	1(13)		

Table 4-13: ROM Interface Signals

4.8.6 Reset Straps

The board resistor straps are sampled on the de-assertion (rising edge) of pci_rst_.

Signal	# of Pins	I/O	Description
reset_strap[7:4] (sw_strap[3:0])	(4)	I	Resistor straps for use by software. These signals are multiplexed with rom_data[7:4] and ntsc_out_data[7:4].
reset_strap[1] (pci_host)	(1)	I	VDD = 1 = MAP-CA DSP is hosting the primary PCI bus GND = 0 = MAP-CA DSP is not hosting The signal is multiplexed with rom_data[1] and ntsc_out_data[1].
reset_strap[0] (rom_boot)	(1)	I	VDD = 1 = Flash ROM is used for boot GND = 0 = ROMless boot The signal is multiplexed with rom_data[0] and ntsc_out_data[0].
TOTAL	(6)		

Table 4-14: Reset Straps

4.9 Analog CRT

An RGB monitor can be directly driven by the MAP-CA digital signal processor.

Signal	# of Pins	I/O	Description
vsync	1	O	Vertical synchronization signal for CRT
hsync	1	O	Horizontal synchronization signal for CRT
gdac_fscale	1	A	Full scale current adjusting resistor
gdac_comp	1	A	Vref bypass and compensation capacitor
gdac_blue	1	A	Analog blue output
gdac_green	1	A	Analog green output
gdac_red	1	A	Analog red output
TOTAL	7		

Table 4-15: CRT Interface Signals

4.10 I^2C

The MAP-CA DSP provides an I^2C interface to communicate with external peripherals such as NTSC decoders, NTSC encoders, and demodulators. The pin description is shown in Table 4-16.

Signal	# of Pins	I/O	Description
iic_sda	1	B (od)	I^2C data line
iic_sck	1	B (od)	I^2C clock line
iic_select	1	O	I^2C-bus external mux select. This pin can also be used as general purpose output
TOTAL	3		

Table 4-16: I^2C Interface Signals

4.11 Boundary Scan (JTAG)

MAP-CA DSP supports boundary scan interface based on *IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture* for testing the MAP-CA DSP and other devices on the board. A BSDL (Boundary Scan Description Language) file is available from Equator.

Signal	# of Pins	I/O	Description
t_{ck}	1	I	Reference clock. This specifies the timing for all the transactions of JTAG interface.
t_{ms}	1	I	Test interface mode select signal.
t_{di}	1	I	Test interface data input
t_{do}	1	O	Test interface data output
t_{rst}	1	I	Active-low reset for the circuitry. It must be low at power up.
TOTAL	5		

Table 4-17: JTAG Interface Signals

4.11.1 Pull Up Resistors

The *IEEE 1149.1* requires that TDI, TMS, and TRST have internal pull-up resistors. In the MAP-CA digital signal processor, TRST has an internal pull-down resistor and TRST, as well as other TAP pins, can be left unconnected if the system does not use Boundary Scan.

4.11.2 TAP State Machine

Figure 4-2 shows the internal states of the TAP (Test Access Port) state machine. These conform to the state transitions specified by *IEEE 1149.1*. The state changes according to the value on TMS at the rising edge of TCK. The TDI value is sampled at the rising edge of TCK, and shifted at the falling edge. The TDO value changes at the falling edge of TCK. When not in the Shift-DR or Shift-IR state, TDO has a high-impedance. If TRST is zero, TDO goes to the Test Logic Reset state asynchronously.

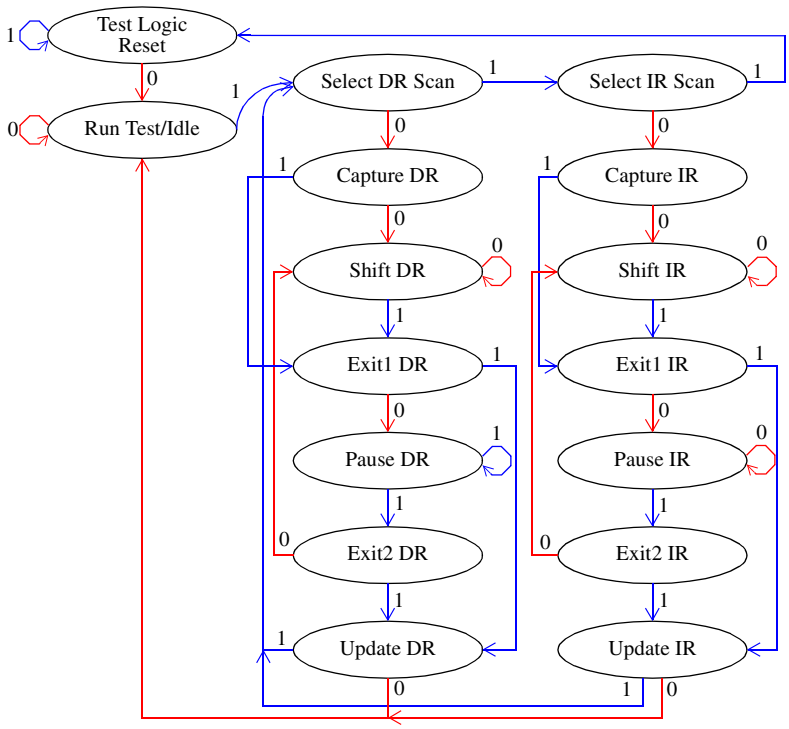


Figure 4-2: TAP State Transition Diagram

4.11.3 Instruction Registers

The MAP-CA digital signal processor supports public instructions defined in *IEEE 1149.1*. Encoding of the Boundary Scan instructions are listed in Table 4-18. The instruction register is five bits long and instruction bit combinations not listed here are reserved.

Instruction	Code	Description
BYPASS	0b11111	connects TDI and TDO with one bit shift register
EXTEST	0b00000	The instruction connects the boundary scan registers and the MAP-CA digital signal processor system pins.
SAMPLE/ PRELOAD	0b11100	sample the MAP-CA DSP output or load the MAP-CA DSP input, without affecting the MAP-CA DSP system pins
IDCODE	0b11001	connects the MAP-CA DSP device with the Device Identification Register between TDI and TDO
INTEST	0b11011	The instruction connects boundary scan registers and MAP-CA DSP internals.
CLAMP	0b11101	sets all system output pins to the value previously loaded by boundary scan instruction.
HIGHZ	0b11110	places all system output pins in a high-impedance state.

Table 4-18: JTAG Instructions

4.11.4 Test Data Registers

Figure 4-3 illustrates the structure of the boundary scan logic..

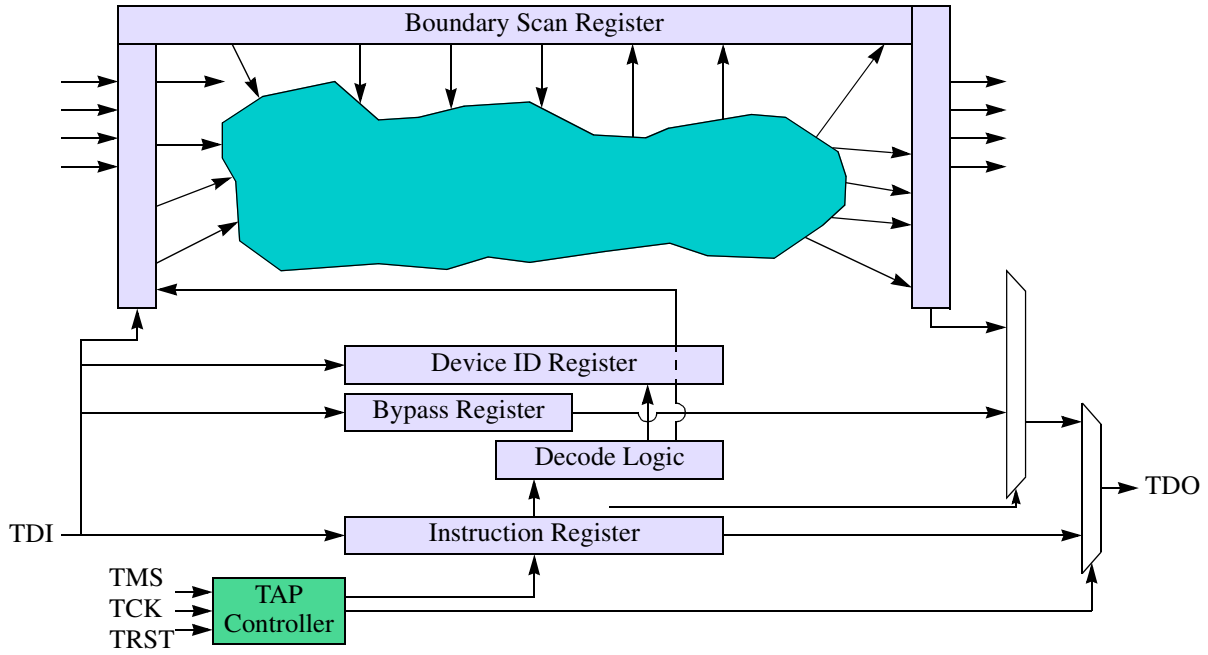


Figure 4-3: Boundary Scan Block Diagram

4.11.5 Boundary Scan Register

The boundary scan register is a shift register on the PAD for controlling the MAP-CA digital signal processor's system pins. Using EXTEST and SAMPLE/PRELOAD commands, it can perform a JTAG (IEEE 1149.1) compliant boundary scan test. The relation between the MAP-CA DSP pins and the boundary scan register can be found in the BSDL.

4.11.6 Device Identification Register

Figure 4-4 shows the format of the Device Identification Register. For the MAP-CA DSP, the Manufacturer's ID is a twelve bit value equal to b000000001111. The upper twelve bits of the Part Number are b010001010011. The lower four bits of the Part Number and the Version Number varies according to the major or minor revision of the MAP-CA DSP.

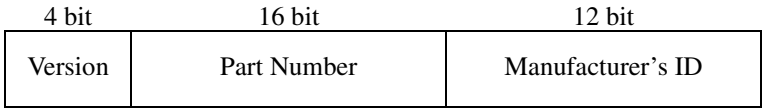


Figure 4-4: Device Identification Register

4.12 Power/Ground Pins

The following power and ground pins are provided on MAP-CA digital signal processor.

Name	# of Pins	Description
Vdd18	30	Digital Core Vdd
Vdd33	27	I/O Power Supply 3.3V
Vss	57	Digital Vss
aVdd18	3	Clean analog Vdd
aVss	4	Clean analog Vss
aVdd33	1	Clean analog Vdd
aVddq	1	Clean analog Vdd for Core PLL
aVssq	1	Clean analog Vss for Core PLL
aVddx	1	Clean analog Vdd for Video DAC
aVssx	1	Clean analog Vss for Video DAC
gdac_cvgg	1	Clean analog Vss for Video DAC
TOTAL	127	

Table 4-19: Power/Ground Pins

4.13 Signal List Summary

Interface	Frequency	Pin Count	Remarks
MAP-CA DSP clocks	Various	9	reference clocks including bypass clocks
PCI	66/33 MHz	54	host/system interface
SDRAM	133 MHz	97	memory interfaces (SDRAM, EEPROM)
Flash ROM	5 MHz	1(13)	
Reset straps	-	(6)	configuration inputs
IEC958	32/44.1/48 kHz sample rate	2	digital audio I/O
I^2S	32/44.1/48 kHz sample rate 1.536/2.116 MHz bit rate	8	digital audio I/O
ITU-R BT.601/656 In	27 MHz	28 (22)[a]	two video input streams: 2 TCI or 2 ITU-656, or 1 TCI and 1 ITU-656, or GPDP and 1 video input (TCI or ITU-656)
Parallel/Serial TCI	30/80 MHz		
GPDP	60 MHz		
ITU-R BT.601/656 Out	27 MHz	10(1)	digital video out or GPDP
CRT out	25-110 MHz	7	analog video out
I^2C	100/400 kHz	3	peripheral control
Test	25 MHz	5	boundary scan (JTAG)
Signal pins total	-	220	
Power/Ground	-	127	
Miscellaneous	-	2	reserved (tie to ground)
	-	3	no connection (leave floating)
TOTAL		352	

Table 4-20: MAP-CA DSP Pin List

a. See Section 4.8.4 for more information about the GPDP shared pins.

Chapter 5 External Connection Examples

5.1 SDRAM

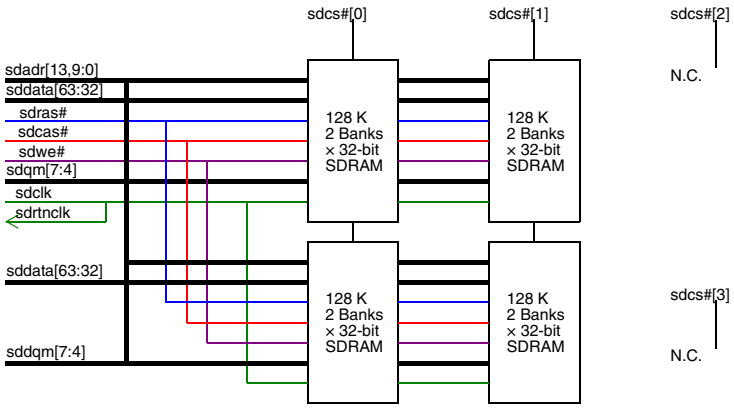


Figure 5-1: 64-bit, 4MB configuration using ×32, 8Mb parts

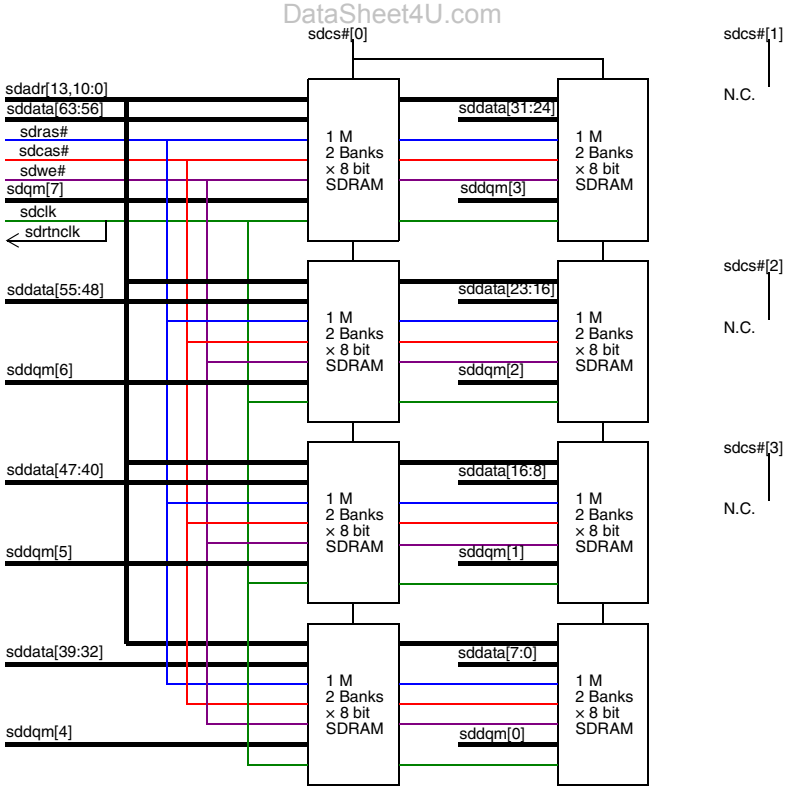


Figure 5-2: 64-bit, 16 MB configuration using ×8, 16 Mb parts

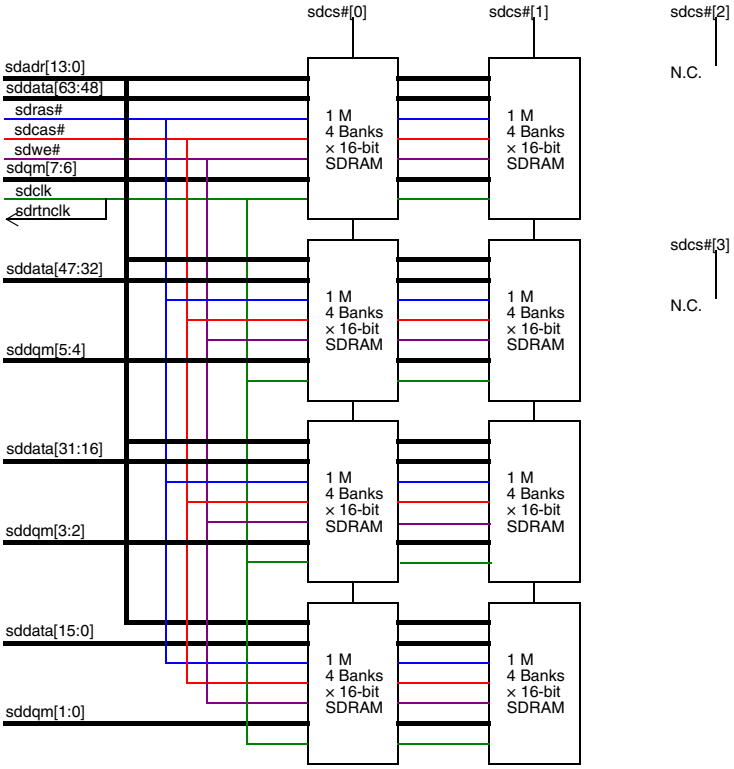


Figure 5-4: 64-bit, 64 MB configuration using ×16, 64 Mb parts

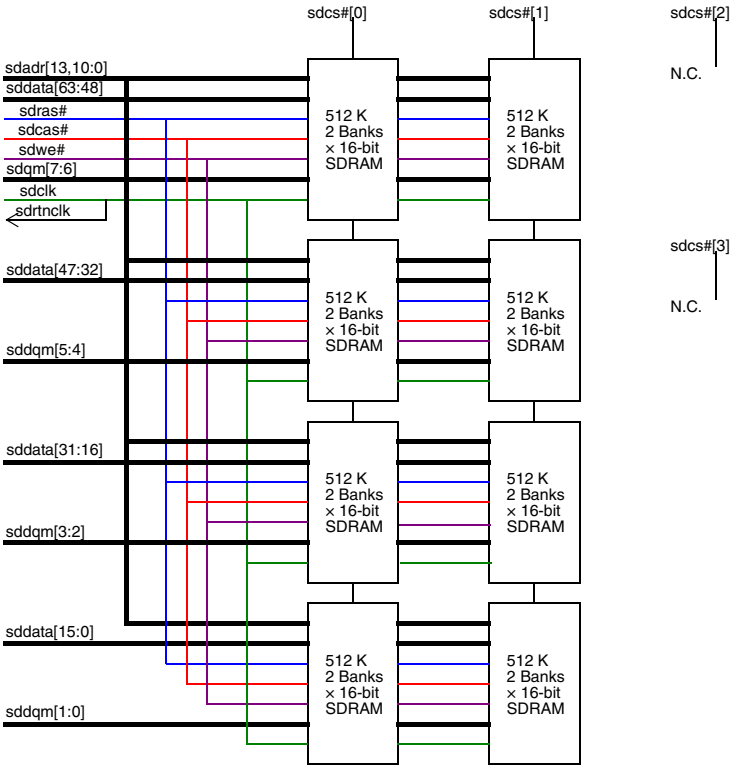


Figure 5-3: 64-bit, 16 MB configuration using ×16 16Mb parts

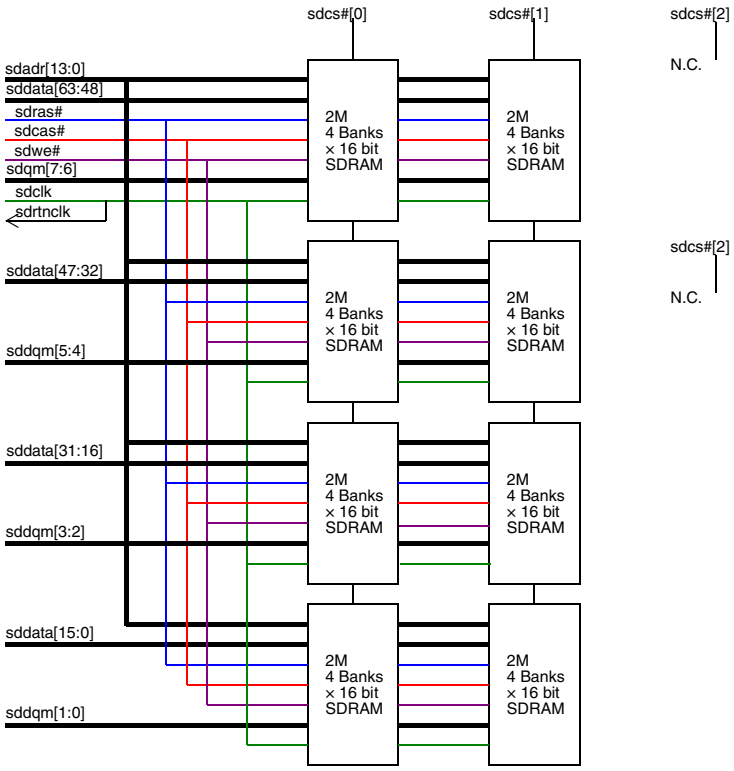


Figure 5-6: 64-bit, 128MB configuration using ×16, 128Mb parts

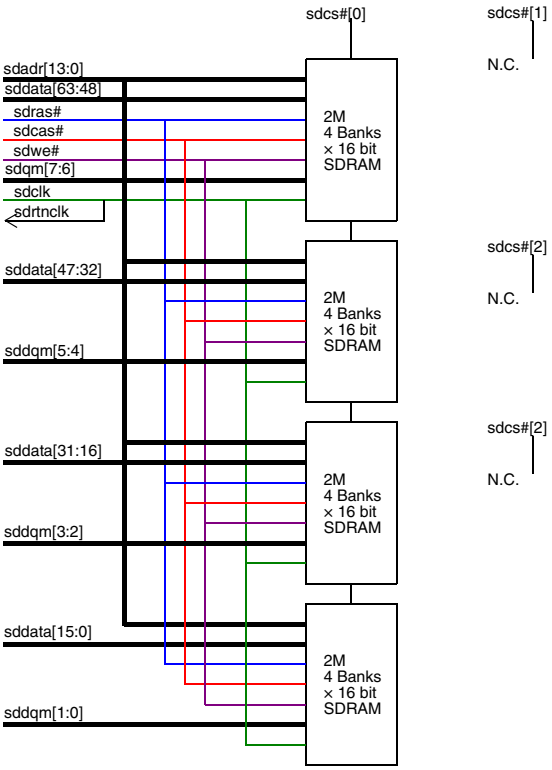


Figure 5-5: 64-bit, 64MB configuration using ×16, 128Mb parts

5.2 IEC958

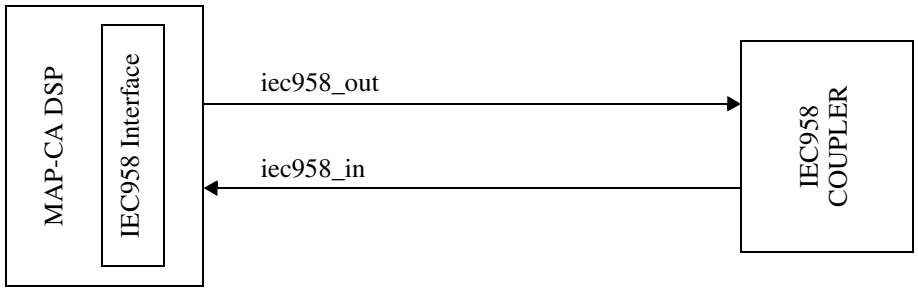


Figure 5-7: IEC958 Interface

5.3 I2S

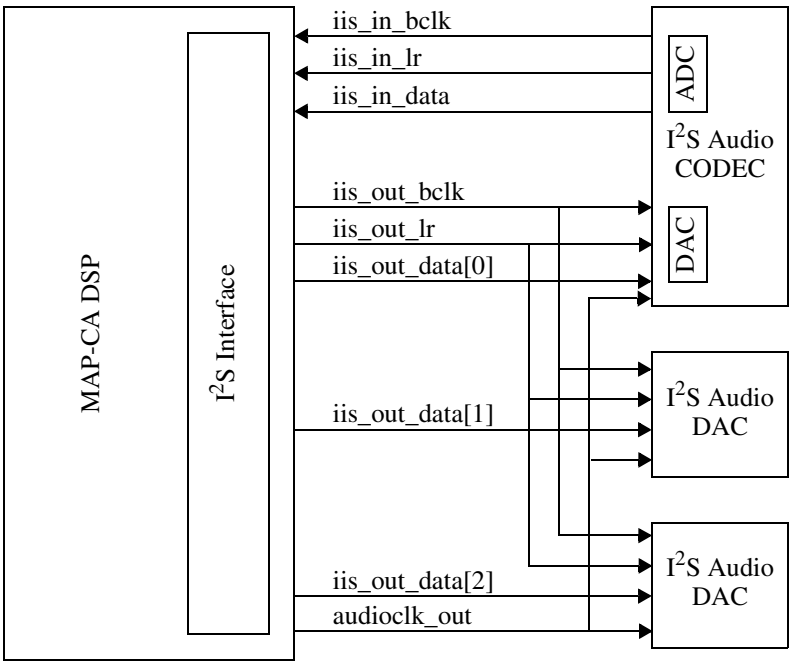


Figure 5-8: I2S Interface

NOTE: Reference designs may use iis_out_bclk and iis_out_lr as input clocks. See the reference board documentation.

5.4 Transport Channel Interface (TCI)

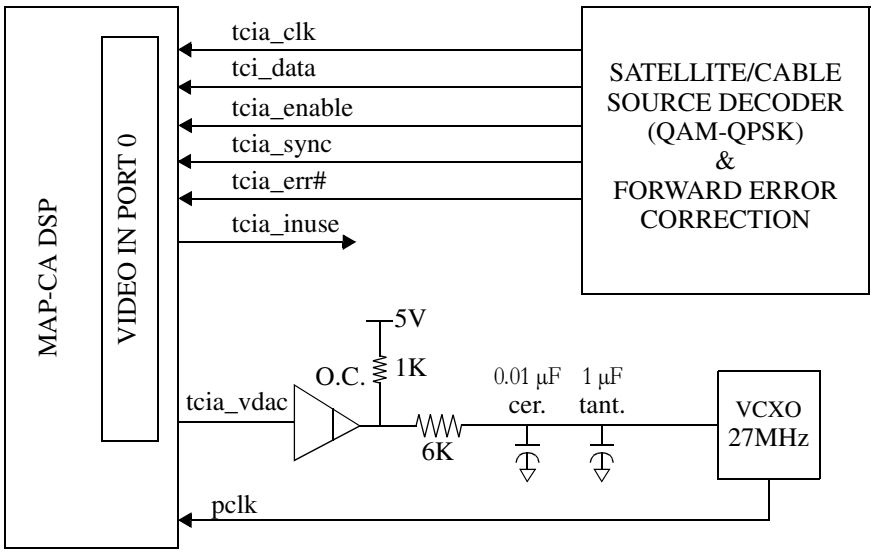


Figure 5-9: Transport Channel Interface

5.5 NTSC Decoder

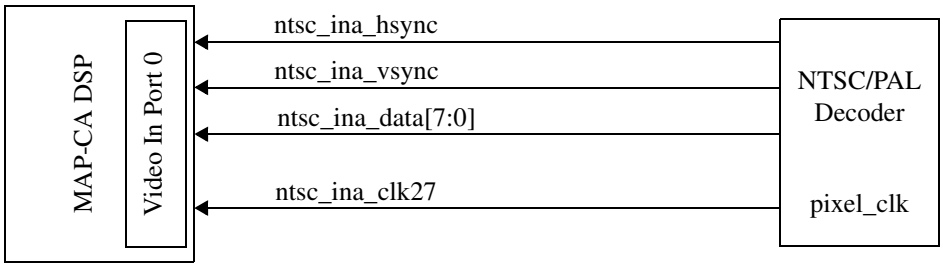


Figure 5-10: ITU-R BT.656 NTSC/PAL Decoder Interface

5.6 NTSC Encoder

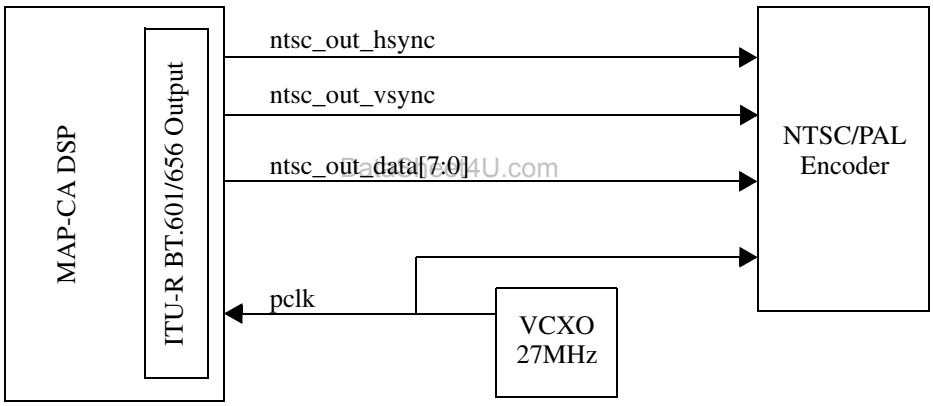


Figure 5-11: NTSC/PAL Encoder Interface

5.7 CRT

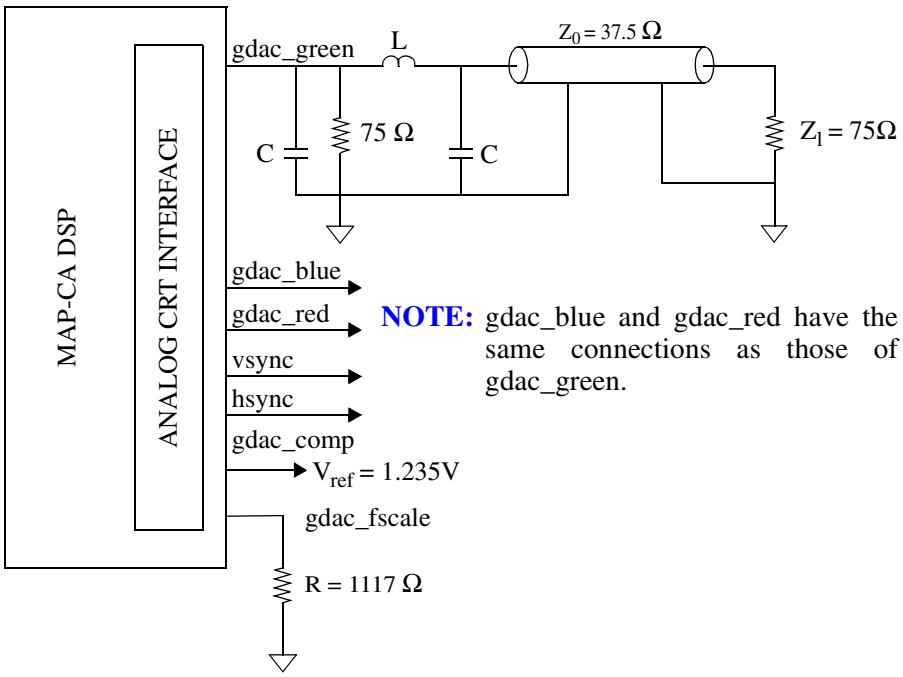


Figure 5-12: CRT

5.8 I^2C

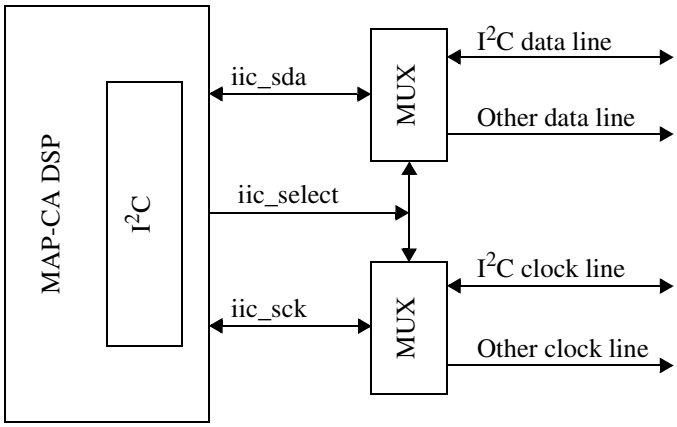


Figure 5-13: I^2C Interface

5.9 ROM

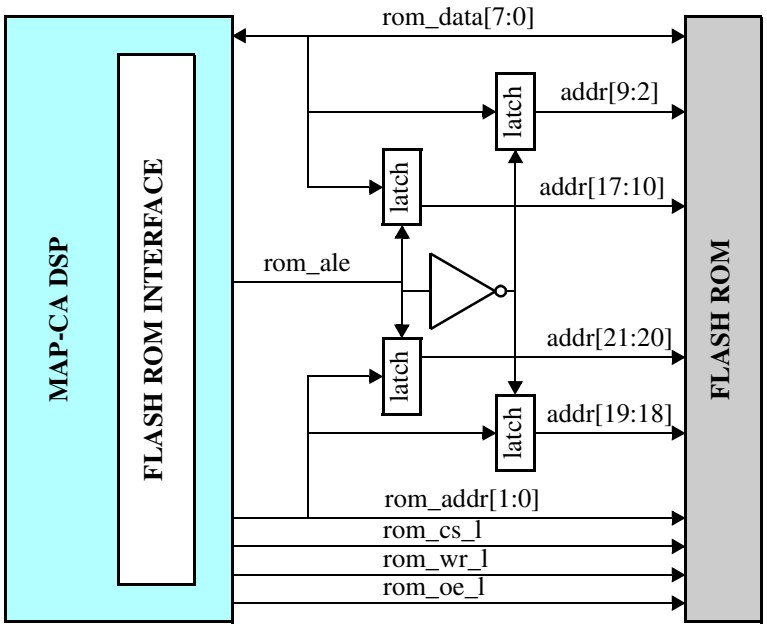


Figure 5-14: ROM Connections

Chapter 6 Electrical Specifications

6.1 Absolute Maximum Ratings

Stresses which occur above or below those listed in Table 6-1 may cause permanent damage to the MAP-CA digital signal processor. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Max	Unit
Vdd18 (measured to Vss)	-0.5	2.5	V
Vdd33 (measured to Vss)	-0.5	4.6	V
aVdd18 (measured to aVss)	-0.5	2.5	V
aVdd33 (measured to aVss)	-0.5	4.6	V
aVddq (measured to aVssq)	-0.5	2.5	V
aVddx (measured to aVss)	-0.5	2.5	V
Voltage on any signal pin[a]	- 0.5	Vdd33 + 0.5	V
Storage Temperature	-55	125	ºC
Junction Temperature	0	85	ºC

Table 6-1: Absolute Maximum Ratings

a. This device employs CMOS devices on all signal pins. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

6.2 Power Supply Specifications

Power Supply	Nominal Voltage	Voltage Variation
Vdd18	1.8 V	±5%
Vdd33	3.3 V	±5%
aVdd18	1.8 V	±5%
aVdd33	3.3 V	±5%
aVddx	1.8 V	±5%

Table 6-2: Voltage Variation

The typical estimated total power consumption is 6 W.

NOTE: During power-up, Vdd18 must come up before or simultaneously with Vdd33. Vdd33 should not exceed Vdd18 by more than 0.4 V while Vdd18 is less than 1V. There is no restriction on the power-down sequence.

Power Supply	Nominal Voltage	Estimated Max Steady State Current
Vdd18	1.8 V	2.8 A
Vdd33	3.3 V	0.25 A
aVdd18	1.8 V	10 mA
aVdd33	3.3 V	80 mA
aVddx	1.8 V	5 mA

Table 6-3: Steady State Current

6.3 DC Characteristics

Parameter	Description	Condition	Min	Max	Unit
V_{IL}	input low voltage	-	-0.5	0.7	V
V_{IH}	input high voltage	-	0.5 Vdd33	Vdd33 + 0.5	V
V_{OL}	output low voltage	I_{out} = 1500 µA	-	0.1 Vdd33	V
V_{OH}	output high voltage	I_{out} = 500 µA	0.9 Vdd33	-	V
I_{LI}	input leakage current	$0 < V_{in} <$ Vdd33	-10	10	µA
I_{OZ}	tri-state output leakage	$0 < V_{in} <$ Vdd33	-10	10	µA
C_{IN}	input pin capacitance	-	-	10	pF
C_{IDSEL}	idsel pin capacitance	-	-	8	pF
C_{CLK}	pci_clk pin capacitance	-	5	12	pF

Table 6-4: PCI Signals

Parameter	Description	Condition	Min	Max	Unit
V_{IL}	input low voltage	-	-0.5	0.6	V
V_{IH}	input high voltage	-	2.0	Vdd33 + 0.5	V
V_{OL}	output low voltage	I_{out} = 2 mA	-	0.4	V
V_{OH}	output high voltage	I_{out} = 2 mA	2.4	-	V
I_{LI}	input leakage current	$0 < V_{in} < Vdd33$	-10	10	µA
I_{LIPU}	leakage current of pull up pin	$0 < V_{in} < Vdd33$	-300	10	µA
I_{LIPD}	leakage current of pull down pin	$0 < V_{in} < Vdd33$	-10	300	µA
I_{OZ}	tri-state output leakage	$0 < V_{in} < Vdd33$	-10	10	µA
C_{IN}	input pin capacitance	-	-	10	pF
C_{IO}	input/output pin capacitance	-	-	12	pF

Table 6-5: Non-PCI Signals

Parameter	Min	Max	Unit
Operating Temperature	0	75	ºC

Table 6-6: Temperature Rating

NOTE: The relationship between gdac_fscale_f and the full scale output current on IOG is:

IOG (mA) = 24.12 * gdac_comp(V) / gdac_fscale_f(ohm)
where gdac_comp is 1.235 V (typical).

Parameter	Symbol	Min	Typical	Max	Unit
Resolutions (FS)	-	8	8	8	Bits
Integral nonlinearity	INL	-	-	± 2	LSB
Differential nonlinearity	DNL	-	-	± 1	LSB

Table 6-7: Video DAC Outputs

Parameter	Symbol	Min	Typical	Max	Unit
Monotonicity	-	-	guaranteed	-	-
White level relative to blank	-	17.69	19.05	20.40	mA
White level relative to black	-	16.74	17.62	18.50	mA
Black level relative to blank	-	0.95	1.44	1.90	mA
Blank level on IOG	-	6.29	7.62	8.96	mA
Blank level on IOR, IOB	-	0	5	50	µA
Sync level on IOG	-	0	5	50	µA
LSB size	-	-	69.1	-	µA
DAC-to-DAC matching	-	-	2	5	%
Output resistance	RAOUT	-	37.5	-	Ω

Table 6-7: Video DAC Outputs

6.4 AC Characteristics

The AC timing specifications listed in this section assume a 20 pF load on all output signals of the MAP-CA DSP.

6.4.1 PLL Reference Clock Input

Description	Value
Rise/fall time	2 ns maximum (0.4V to 2.4V)
Duty cycle	50% ± 10%
Maximum cycle to cycle jitter	± 200 ps

Table 6-8: PLL Reference Clock Input Conditions

6.4.2 SDRAM Interface Timing

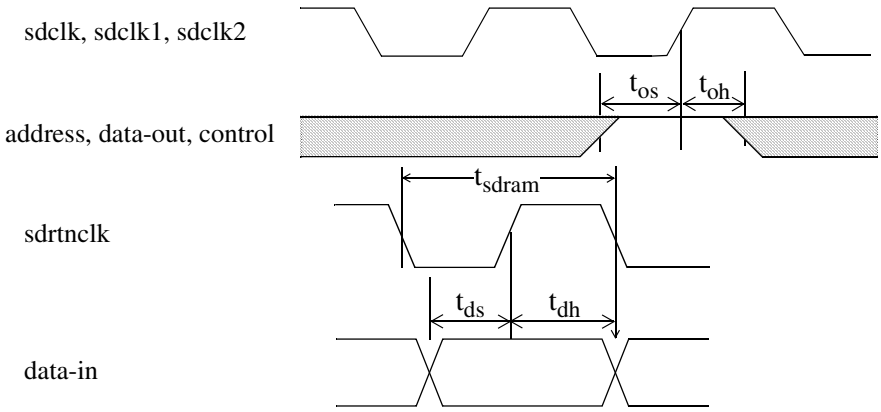


Figure 6-1: SDRAM Timing Measurement Conditions

Correct setup and hold times can be guaranteed through internal delay adjustment, controlled by bits [30:24] of the synchronizer/clock control register in MAP-CA DSP memory block. The SdMrckDly and SdMckDly fields control internal delay circuits that affect the timing of signals going to and from the SDRAM components. They should be adjusted so that setup and hold requirements of both the SDRAM and the MAP-CA DSP are met.

Symbol	Description	Min	Max	Unit
f_{sdram} [a]	sdclk frequency	-	133	MHz
t_{os}	Output setup time for address, data, control (sdcs_, sdras_, sdcas_, sdwe_, sddqm)	1.9	-	ns
t_{oh} [b]	Output hold time of address, data, control (sdcs_, sdras_, sdcas_, sdwe_, sddqm)	1.5	-	ns
t_{ds} [c, d]	Input data setup time	1	-	ns
t_{dh} [c, d]	Input data hold time	2	-	ns

Table 6-9: SDRAM Interface Timing Parameters[e]

a. $f_{sdram} = 1 / t_{sdram}$

b. The center of the rising edges of sdclk1 and sdclk2 is used as the reference point.

c. sdrtnclk is used as the reference clock.

d. A matching mechanism is provided to compensate for the propagation delay through circuit board traces to and from the external SDRAM devices. To optimize read timing margin, sdrtnclk should be connected to sdclk with a dedicated trace, with an optional lumped RC load attached to the middle, to account for the number of SDRAM devices attached to the clock line.

e. Measured with SdMrckDly = 0 and SdMckDly = 3.

6.4.3 PCI Bus Timing

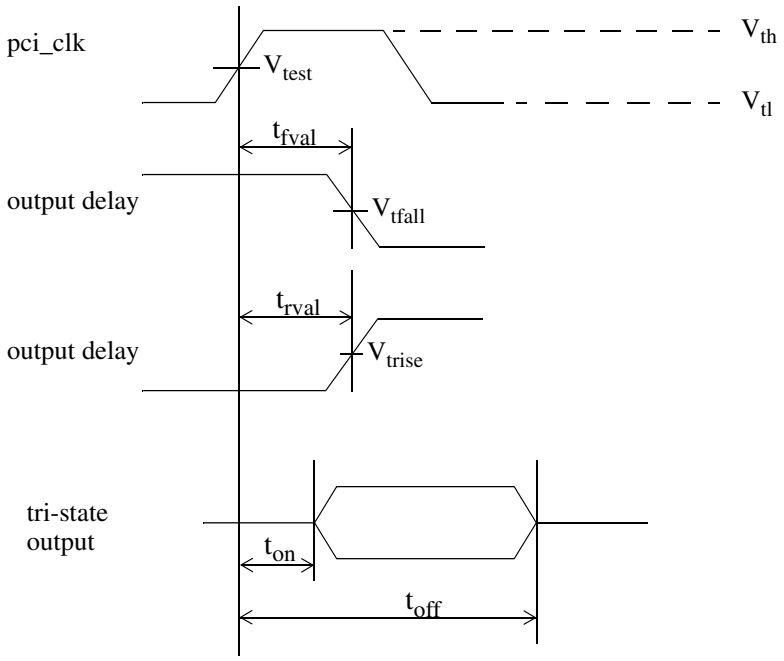


Figure 6-2: PCI Output Timing Measurement Conditions

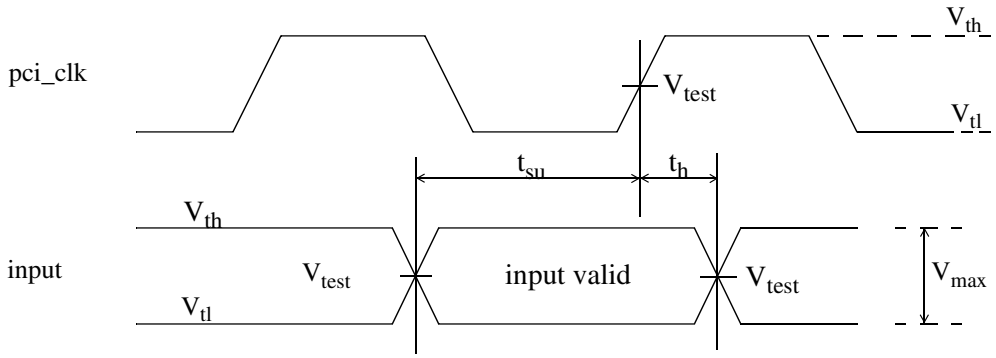


Figure 6-3: PCI Input Timing Measurement Conditions

Symbol	Description	Min	Max	Unit
t_{pci_clk}	clock cycle time	15	30	ns
t_{high}	clock high time	6	-	ns
t_{low}	clock low time	6	-	ns
clk_{slew}	clock slew rate	1.5	4	V/ns
$t_{su(bus)}$	input set up time to clk, bussed signals	3	-	ns
$t_{su(ptp)}$	input set up time to clk, point-to-point signals	5	-	ns
$t_{val(bus)}$	clk to signal valid delay, bussed signals	2	6	ns
$t_{val(ptp)}$	clk to signal valid delay, point to point signal	2	6	ns
t_{on}	float to active delay	2	-	ns
t_{off}	active to float delay	-	14	ns
t_h	input hold time from clock	500	-	ps
t_{rst} [a]	reset active time after power stable	1	-	ms
$t_{rst-clk}$	reset active time after clk stable	100	-	µs
$t_{rst-off}$	reset active to output float delay	-	40	ns

Table 6-10: PCI Interface Timing Parameters

a. pci_rst_ is asserted and de-asserted asynchronously with respect to pci_clk. All output drivers are floated when pci_rst_ is active.

Symbol	Value	Unit
V_{max}	0.4 Vdd33	V
V_{test}	0.4 Vdd33	V
V_{tfall}	0.615 Vdd33	V
V_{th}	0.6 Vdd33	V
V_{tl}	0.2 Vdd33	V
V_{trise}	0.285 Vdd33	V
input signal slew rate	1.5	V/ns

Table 6-11: PCI Measurement Conditions

6.4.4 IEC958 Interface Timing

Symbol	Description	Min	Typical	Max	Unit
F_s	Audio sample rate		32, 44.1, 48		kHz

Table 6-12: IEC958 Interface Timing Parameters

6.4.5 I²S Interface Timing

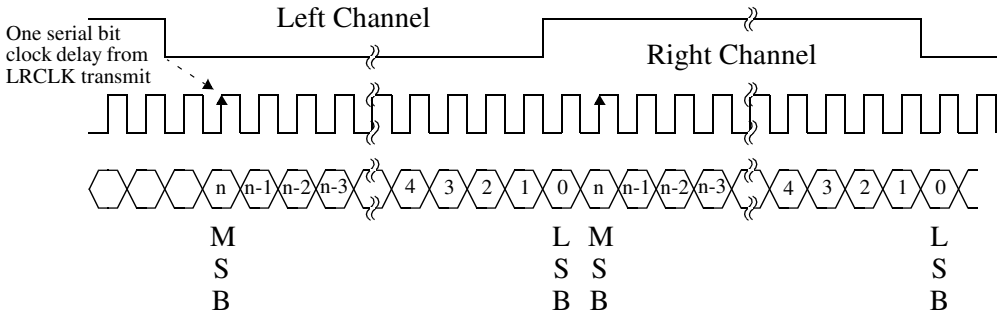


Figure 6-4: I²S Data Format

The audio PLL generates audioclk_out for use by external codecs as master MCLK. MCLK can be programmed for either 12.288 MHz or 16.933 MHz to achieve the desired audio sample rate (LRCLK), according to Table 6-13. The MSB:LSB ordering can be reversed by software programming.

LRCLK[a] (kHz)	MCLK[b] (MHz)	SCLK[c] (MHz)	MCLK/ LRCLK	MCLK/ SCLK	BITS/ FRAME[d]	BITS/ CHANNEL
48	12.288	1.536	256	8	32	16
44.1	16.933[e]	2.116	384	8	48	24
32	12.288	1.536	384	8	48	24

Table 6-13: I²S Clock Ratios

a. LRCLK = iis_in_lr or iis_out_lr.

b. MCLK = audioclk_out; MCLK defaults to 27 MHz on power-up (audio PLL bypassed).

c. SCLK = iis_in_bclk or iis_out_bclk.

d. Bits/Frame = 2*Bits/Channel = SCLK/LRCLK. When MCLK/LRCLK = 384, 24 bits per channel are always transmitted, but the number of valid bits is selectable from 16, 18, 20 or 24.

e. MCLK defaults to 16.933 MHz when audio PLL is enabled.

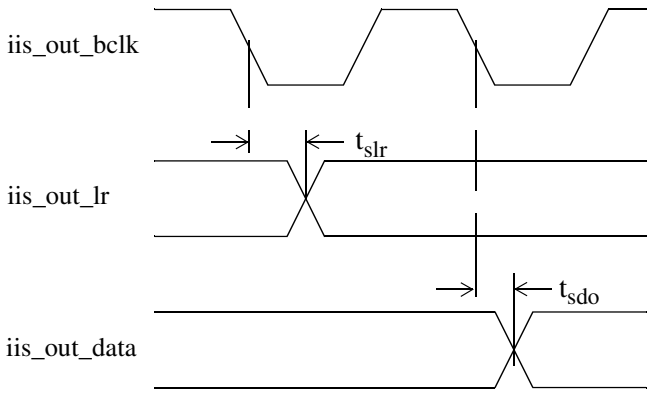


Figure 6-5: I²S Output Timing Measurement Conditions

Symbol	Description	Min	Max	Unit
F_s	Output sample rate	32, 44.1, 48		kHz
t_{slr}	SCLK falling to LRCLK delay	-10	10	ns
t_{sdo}	SCLK falling to SDATA valid	-10	10	ns

Table 6-14: I²S Output Timing Parameters

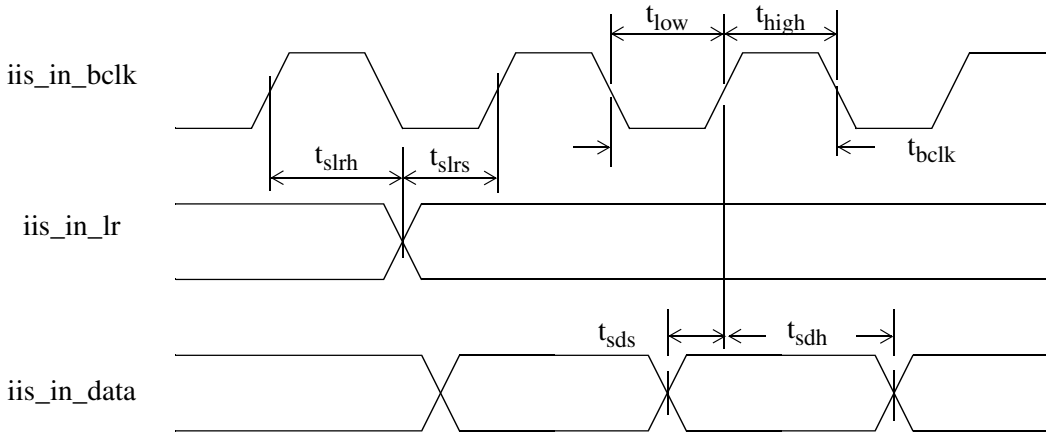


Figure 6-6: I²S Input Timing Measurement - Slave Mode

Symbol	Description	Min	Max	Unit
F_s	Input sample rate	32, 44.1, 48		kHz
F_{mclk}	MCLK frequency	see Table 6-13		From Table
T_{bclk}	SCLK period	$8/F_{mclk}$	-	From Table
T_{low}	SCLK pulse width low	$2/F_{mclk}$	-	From Table
T_{high}	SCLK pulse width high	$2/F_{mclk}$	-	From Table
t_{slrh}	SCLK rising to LRCLK hold	20	-	ns
t_{slrs}	SCLK rising to LRCLK setup	20	-	ns
t_{sds}	SDATA valid to SCLK rising setup	20	-	ns
t_{sdh}	SCLK rising to SDATA hold time	20	-	ns

Table 6-15: I^2S Input Timing Parameters - Slave Mode

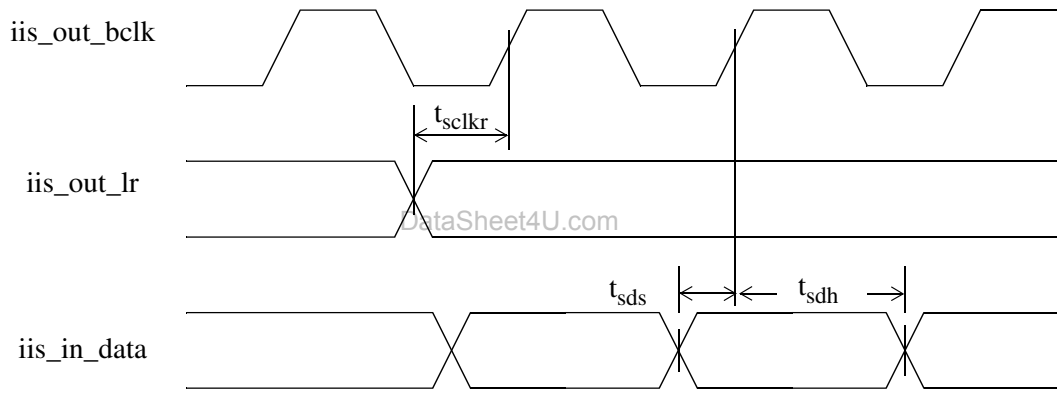


Figure 6-7: I^2S Input Timing Measurement - Master Mode

Symbol	Description	Min	Typical	Max	Unit
F_s	Input sample rate	-	32, 44.1, 48	-	kHz
F_{mclk}	MCLK frequency	see Table 6-13			From Table
T_{bclk}	SCLK period	$8/F_{mclk}$	-	-	From Table
t_{sclkr}	SCLK rising to LRCLK edge	-	$T_{bclk}/2$	-	µs
t_{sds}	SDATA valid to SCLK rising setup	$(1/F_{mclk})+10$	-	-	ns
t_{sdh}	SCLK rising to SDATA hold	$(1/F_{mclk})+15$	-	-	ns

Table 6-16: I^2S Input Timing Parameters - Master Mode

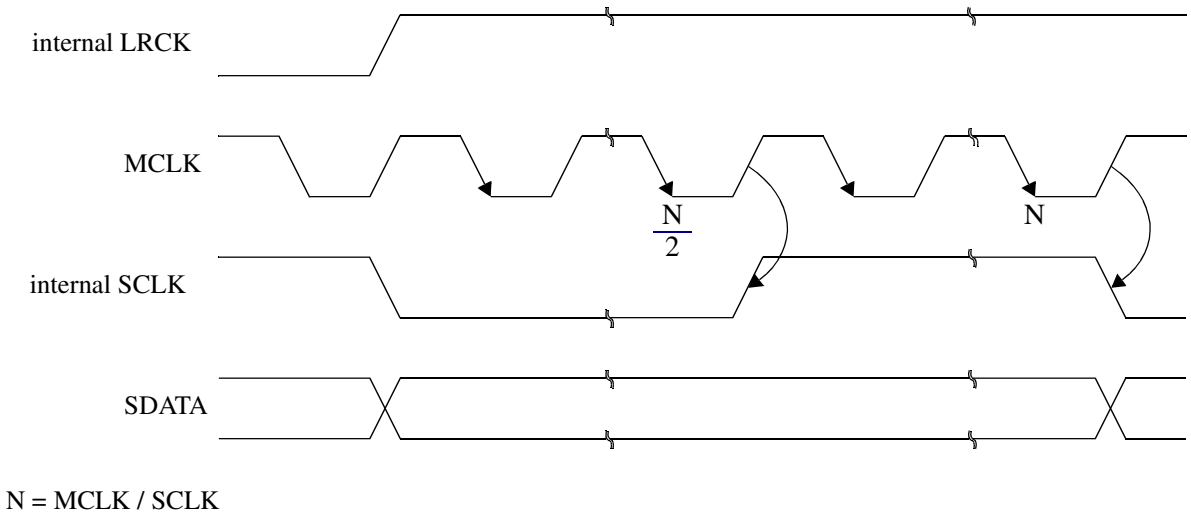


Figure 6-8: Internal Serial Clock Generation for I^2S Master Mode

6.4.6 Transport Channel Interface Timing

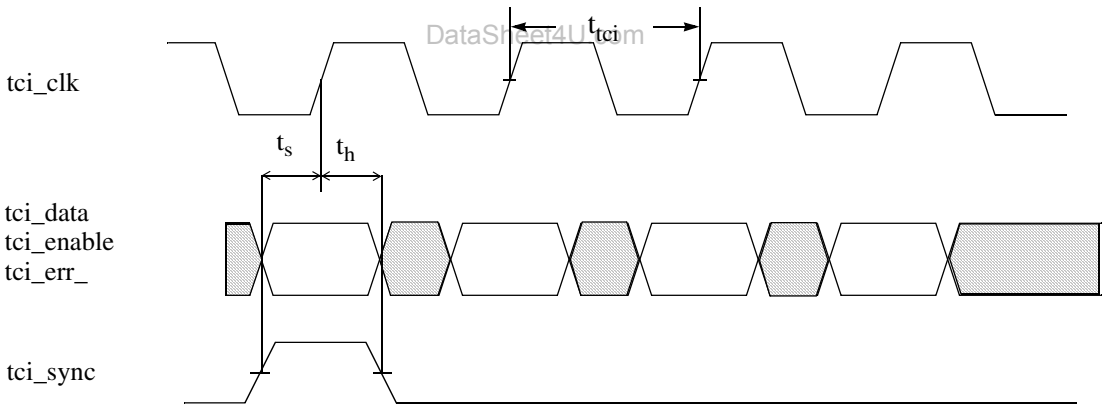


Figure 6-9: TCI Timing Measurement Conditions

NOTE: The timing diagram and Table 6-17 are relevant to the primary TCI input port. Timing relationships, input setup, and hold times are identical for the secondary TCI input port. However, the `tci_vdac` output is not present on the secondary output port. Inputs `video_ina[9:0]` includes `tci_data[7:0]` (bits 7:0), `tci_enable` (bit 8), and `tci_err_` (bit 9)

Symbol	Description	Min	Max	Unit
f_{tci}	TCI clock frequency[a, b, c, d]	-	27 (parallel) 80 (serial)	MHz
t_h	Hold time	1	-	ns
t_s	Setup time	4	-	ns

Table 6-17: TCI Timing Parameters

a. In parallel mode, it is required that $t_{core} > f_{tci\_clk}$.

b. In serial mode, it is required that $t_{core} > ½ f_{tci\_clk}$.

c. For correct audio clock counter operation, $f_{core}/f_{audio} > 4$, where f_{audio} is the frequency of audioclk_out produced by the on-chip PLL.

d. For correct video clock counter operation, $f_{core}/f_{video} > 4$, where f_{video} is the frequency of pclk.

6.4.7 ITU-R BT.601/656 Interface Timing

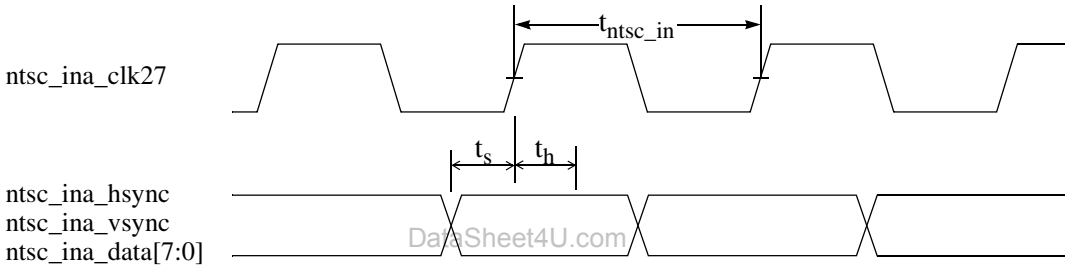


Figure 6-10: ITU-R BT.601/656 Input Timing Measurement Conditions

Symbol	Description	Min	Max	Unit
f_{ntsc_in}	NTSC input clock frequency	-	27	MHz
t_h	Input hold time for video_ina[9:0], from cross over of rising clock	1	-	ns
t_s	Input setup time video_ina[9:0], to the cross over of rising clock	5	-	ns

Table 6-18: ITU-R BT.601/656 Input Interface Timing Parameters

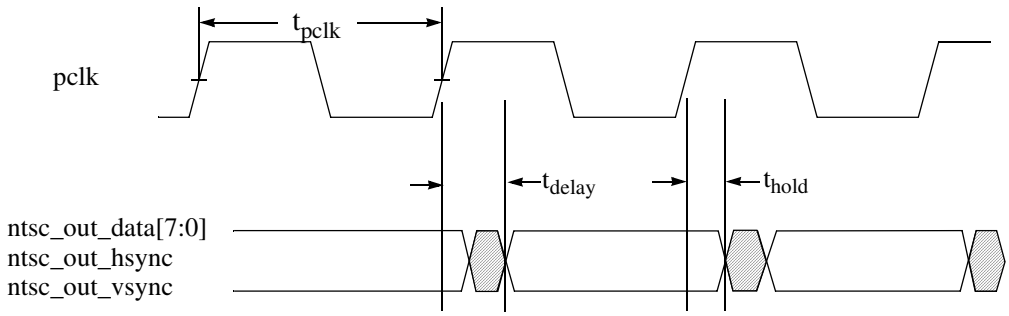


Figure 6-11: ITU-R BT.601/656 Output Timing Measurement Conditions

NOTE: This timing diagram and table include information for the primary video input port. The primary video input bus `video_ina[9:0]` includes the byte-wide data bus (bits 7:0), horizontal sync (bit 8), and vertical sync (bit 9). The secondary video input signals have identical timing relationships

.

Symbol	Description	Min	Max	Unit
t_{pclk}	pclk cycle time	18.5	37	ns
t_{delay}	Maximum delay time	-	11	ns
t_{hold}	Output hold time	4	-	ns

Table 6-19: ITU-R BT.601/656 Output Interface Timing Parameters

6.4.8 General Purpose Data Port

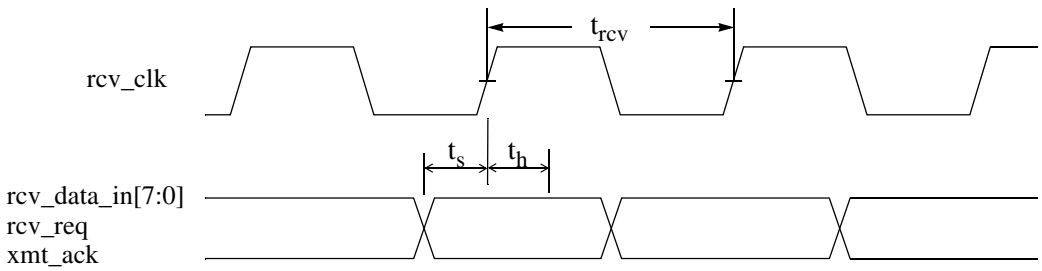


Figure 6-12: GPDP Input Timing Measurement Conditions

Symbol	Description	Min	Max	Unit
t_{rcv}	Receive clock cycle time	-	60	MHz
t_h	Hold time	0	-	ns
t_s	Setup time	4	-	ns

Table 6-20: GPDP Input Timing Parameters

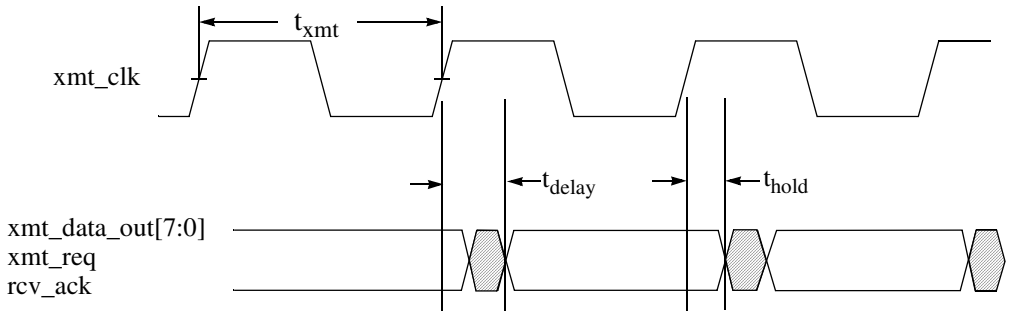


Figure 6-13: GPDP Output Timing Measurement Conditions

Symbol	Description	Min	Max	Unit
t_{xmt}	Transmit clock cycle time	-	60	MHz
t_{hold}	Output hold time	3.0	-	ns
t_{delay}	Maximum delay time	-	8	ns

Table 6-21: GPDP Output Timing Parameters

6.4.9 I²C Interface Timing

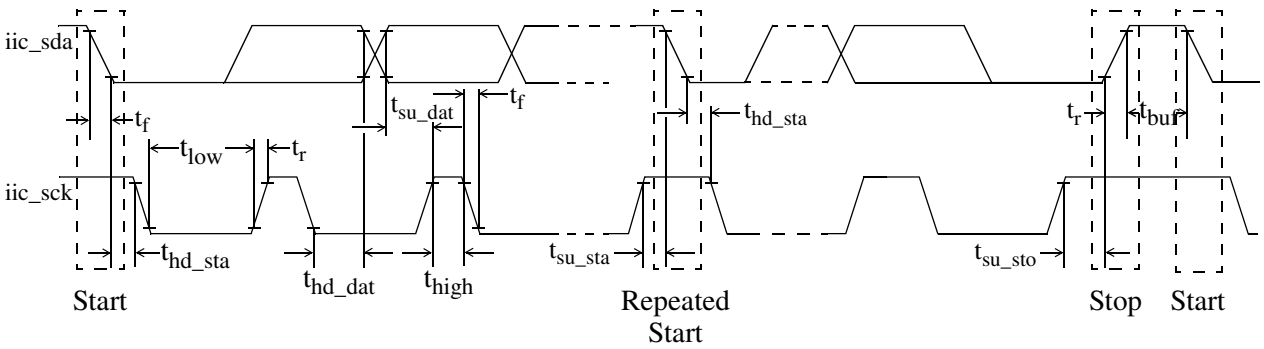


Figure 6-14: I²C Timing Measurement Conditions

Symbol[a]	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{sck}	iic_sck clock frequency.	0	100	0	400	kHz
t_{hd_sta}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	2.3	-	0.57	-	µs
t_{low}	LOW period of the iic_sck clock.	4.7	-	1.27	-	µs
t_{high}	HIGH period of the iic_sck clock.	4.0	-	0.6	-	µs
t_{su_sta}	Setup time for a repeated START condition.	4.7	-	0.6	-	µs
t_{hd_dat}	Data hold time.	0[b]	3.45	0[b]	0.9	µs
t_{su_dat}	Data setup time.	250	-	250	-	ns
t_r	Rise time of both iic_sda and iic_sck signals.	-	1000	$20 + 0.1C_b$[c]	300	ns
t_f	Fall time of both iic_sda and iic_sck signals.	-	300	$20 + 0.1C_b$	300	ns
t_{su_sto}	Setup time for STOP condition.	4.0	-	0.6	-	µs
t_{buf}	Bus free time between a STOP and START condition.	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line.	-	400	-	400	pF

Table 6-22: I^2C Interface Timing Parameters

a. All values referred to V_{IHmin} and V_{ILmax} levels. See Table 6-5.

b. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

c. C_b = total capacitance of one bus line in pF.

Appendix A Glossary

These acronyms and names used in this *Data Sheet*. These are their expansion or explanation.

BSDL .....Boundary Scan Description Language

DataStreamer controller ....High speed DMA engine that operates independent from VLIW core, also referred to as the DS controller

DRC .....Display Refresh Controller

DTS.....Data Transfer Switch - high speed MAP-CA DSP series internal data bus

FEC .....Forward error correction

I-ALU .....Integer ALU (Arithmetic Logic Unit) - performs loads, stores, branches, integer arithmetic, and logical operations

IG-ALU .....Integer, Graphics unit - performs integer arithmetic and (partitioned) multimedia operations

MAP-CA DSP .....Media Accelerated Processor for Consumer Appliances

MMU .....Memory Management Unit

PLC .....128-bit Partitioned Local Constant register

PLV .....128-bit Partitioned Local Variable register

SIMD .....Single Instruction Multiple Data

TLB.....Translation Lookaside Buffer

VLx .....A coprocessor on MAP-CA DSP that can accelerate variable length encoding and variable length decoding.

Appendix B Package Specifications

This appendix to the MAP-CA DSP Datasheet describes the specifications of the 352 pin BGA package

B.1 Mechanical Specifications

B.1.1 Outline and Footprint

The following sections use millimeter (mm) as the unit of measure.

B.1.1.1 Top and Bottom Views

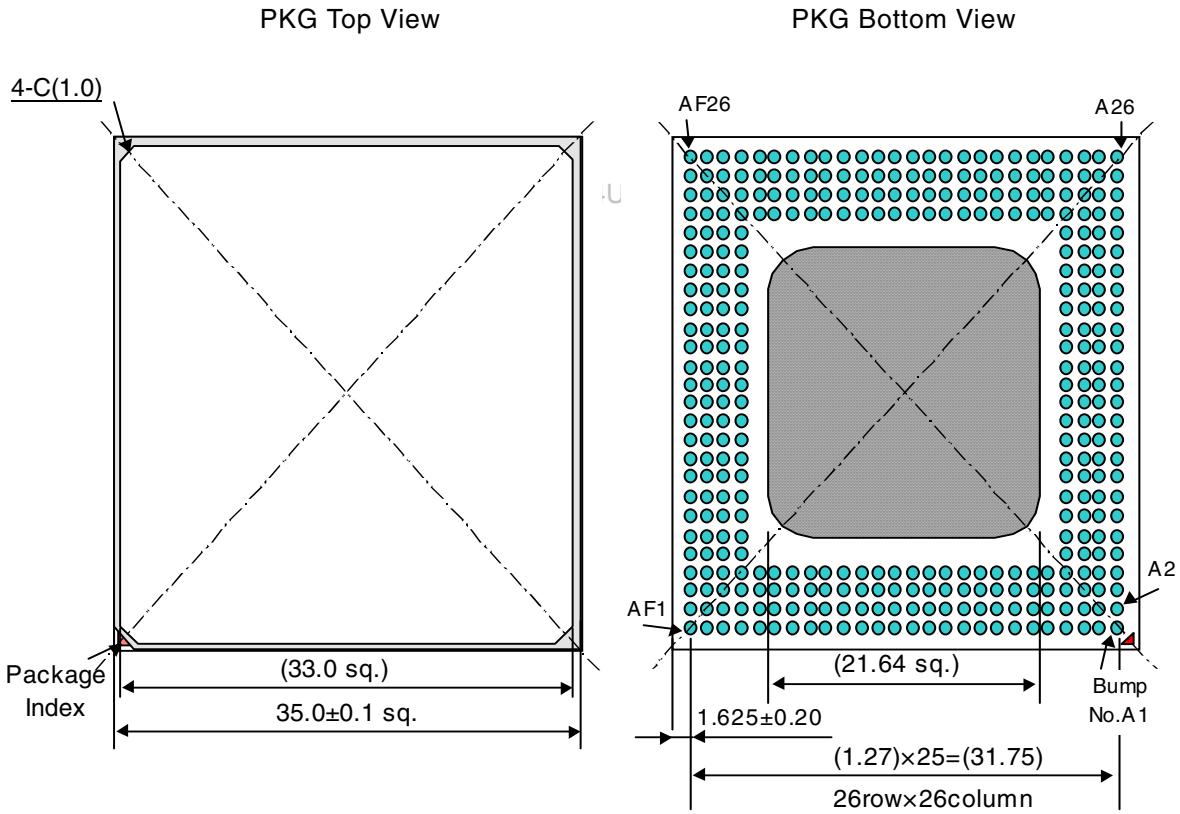
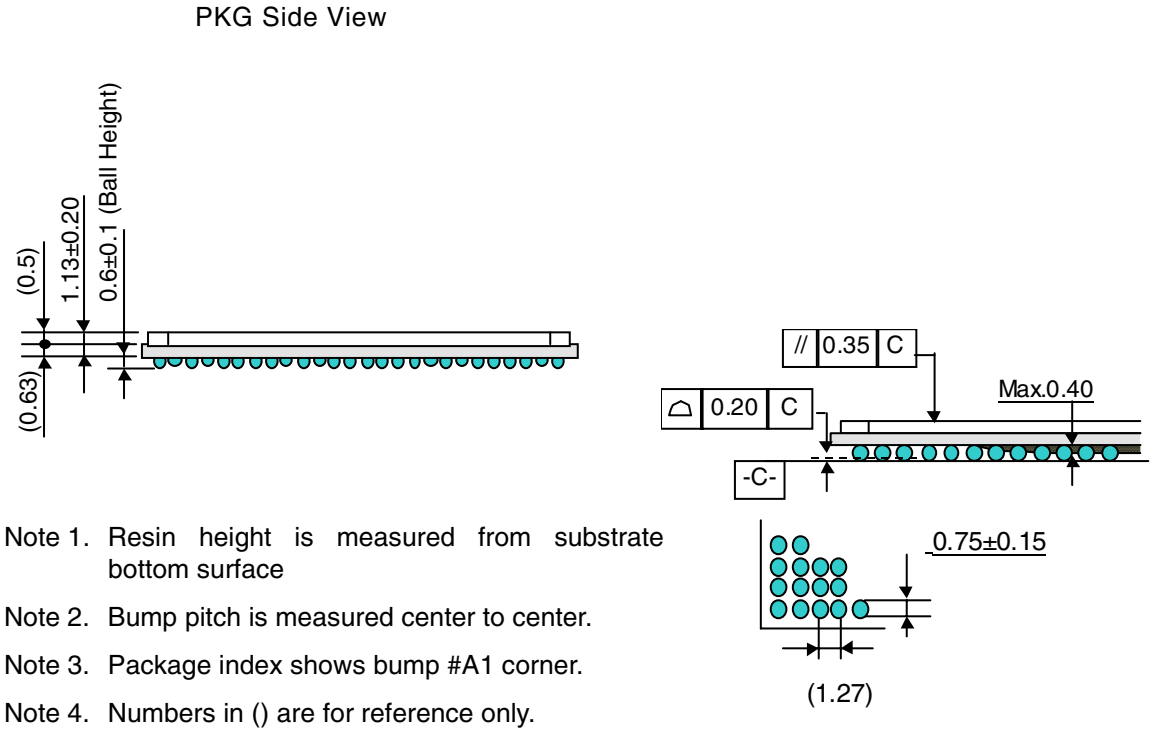


Figure B-1: 352 Pin BGA Outline and Footprint - Top and Bottom Views

B.1.1.2 Side View



Note 1. Resin height is measured from substrate bottom surface

Note 2. Bump pitch is measured center to center.

Note 3. Package index shows bump #A1 corner.

Note 4. Numbers in () are for reference only.

Figure B-2: 352 Pin BGA Outline and Footprint - Side Views

B.2 Package Materials

B.2.1 Materials Specification

Segment	Material
Package substrate	BT Resin
Encapsulation	Epoxy with filler
Heat Spreader	Cu + Ni plating
Solder Ball	37 Pb - 63 Sn

Table B-1: Material Used.

B.2.2 Index Location

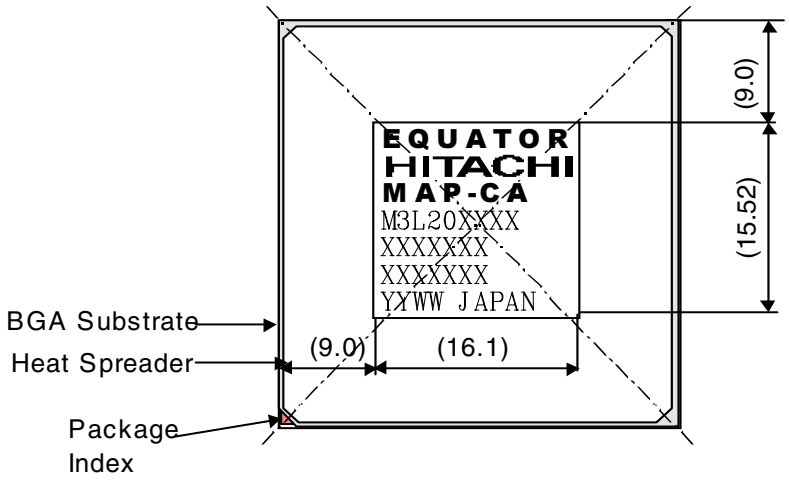


Figure B-3: Index Location