

SILICON GATE BiCMOS

8,192 WORD x 8 BIT BiCMOS STATIC RAM

Description

The TC55B88P/J is a 65,536 bit high speed BiCMOS static random access memory organized as 8,192 words by 8 bits and operated from a single 5V supply. Toshiba's BiCMOS technology and advanced circuit design enable high speed operation.

The TC55B88P/J features low power dissipation when the device is deselected using chip enable ($\overline{CE1}$, $\overline{CE2}$) and has an output enable input (\overline{OE}) for fast memory access.

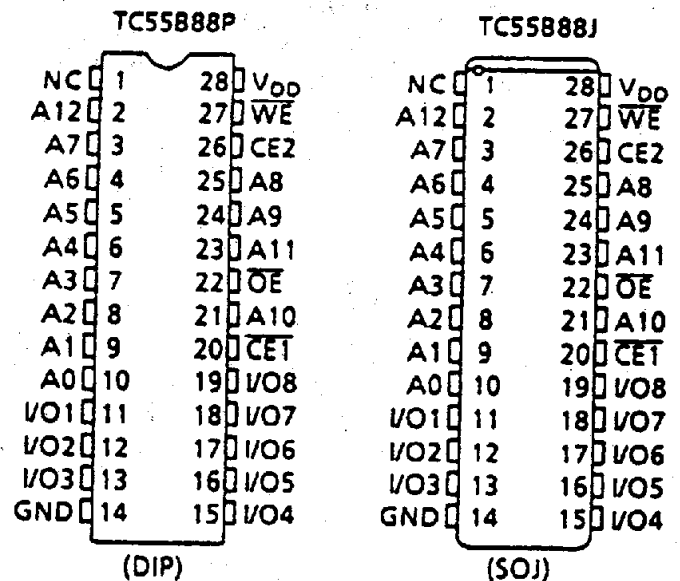
The TC55B88P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible.

The TC55B88P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC55B88P/J-10 10ns (max.)
 - TC55B88P/J-12 12ns (max.)
- Low power dissipation
 - Operation: 155mA (max.)
 - Standby: 10mA (max.)
- Single 5V power supply: 5V±5% (-10)
5V±10% (-12)
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC55B88P: DIP28-P-300B
 - TC55B88J: SOJ28-P-300A

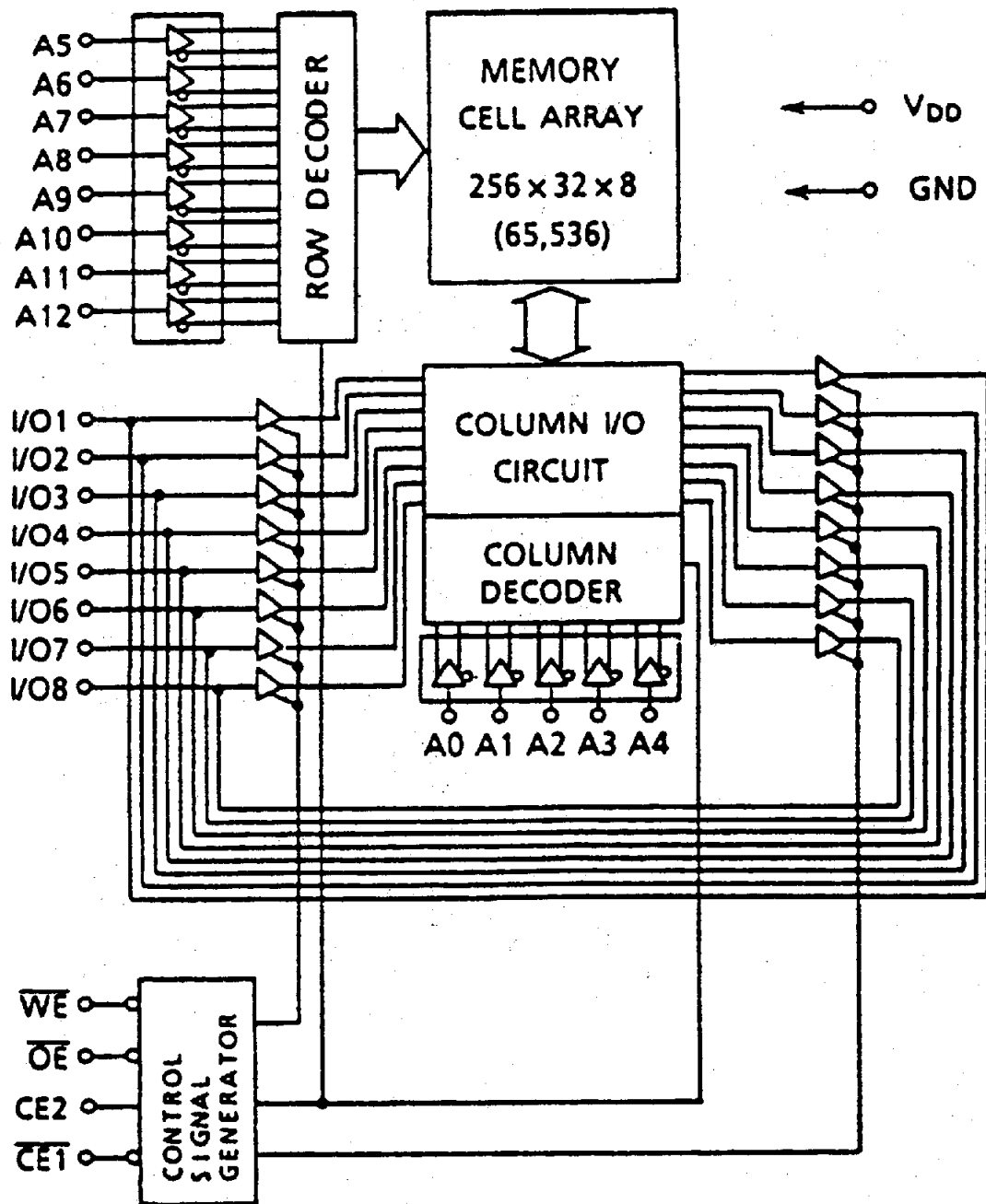
Pin Connection (Top View)



Pin Names

A0 - A12	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Inputs
WE	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power (+5V)
GND	Ground
NC	No Connection

Block Diagram



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
V _{DD}	Power Supply Voltage	-10	4.75	5.0	5.25	V
		-12	4.5	5.0	5.5	
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.5	V	
V _{IL}	Input Low Voltage	-0.5*	-	0.8	V	

* -3V with a pulse width of 10ns

DC Characteristics (Ta = 0 ~ 70°C, -10: V_{DD} = 5V±5%, -12: V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}		-	-	±10	μA	
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or WE = V _{IL} or OE = V _{IH} , V _{OUT} = 0 ~ V _{DD}		-	-	±10	μA	
I _{OH}	Output High Current	V _{OH} = 2.4V		-4	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4V		8	-	-	mA	
I _{DDC}	Operating Current	t _{cycle} = Min cycle CE1 = V _{IL} and CE2 = V _{IH} Other Inputs = V _{IH} /V _{IL} I _{OUT} = 0mA	V _{DD} = 5.25V	-10	-	-	155	mA
		t _{cycle} = Min cycle CE1 = V _{IL} and CE2 = V _{IH} Other Inputs = V _{IH} /V _{IL} I _{OUT} = 0mA	V _{DD} = 5.5V	-12	-	-		
I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL} Other Inputs = V _{IH} /V _{IL}	V _{DD} = 5.25V	-10	-	-	30	mA
		CE1 = V _{IH} or CE2 = V _{IL} Other Inputs = V _{IH} /V _{IL}	V _{DD} = 5.5V	-12	-	-		
I _{DDS2}		CE1 = V _{DD} - 0.2V or CE2 = 0.2V Other Inputs = V _{DD} - 0.2V or 0.2V		-	-	10		

Capacitance* (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	7	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics ($T_a = 0 \sim 70^\circ\text{C}^{(1)}$, -10: $V_{DD} = 5V \pm 5\%$, -12: $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55B88P/J-10		TC55B88P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	–	12	–	ns
t_{ACC}	Address Access Time	–	10	–	12	
t_{CO1}	$\overline{CE1}$ Access Time	–	10	–	12	
t_{CO2}	CE2 Access Time	–	10	–	12	
t_{OE}	\overline{OE} Access Time	–	6	–	7	
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	3	–	3	–	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	–	5	–	6	
t_{OEE}	Output Enable Time from \overline{OE}	1	–	1	–	
t_{ODO}	Output Disable Time from \overline{OE}	–	5	–	6	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	10	–	12	

Write Cycle

SYMBOL	PARAMETER	TC55B88P/J-10		TC55B88P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	–	12	–	ns
t_{CW}	Chip Enable to End of Write	7	–	8	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{AW}	Address Valid to End of Write	7	–	8	–	
t_{WP}	Write Pulse Width	6	–	7	–	
t_{WR}	Write Recovery Time	1	–	1	–	
t_{DS}	Data Setup Time	6	–	7	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from \overline{WE}	1	–	1	–	
t_{ODW}	Output Disable Time from \overline{WE}	–	5	–	6	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

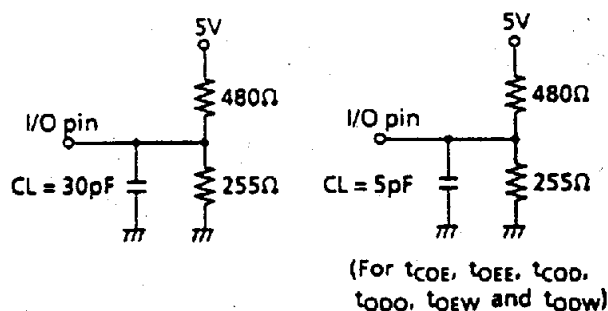
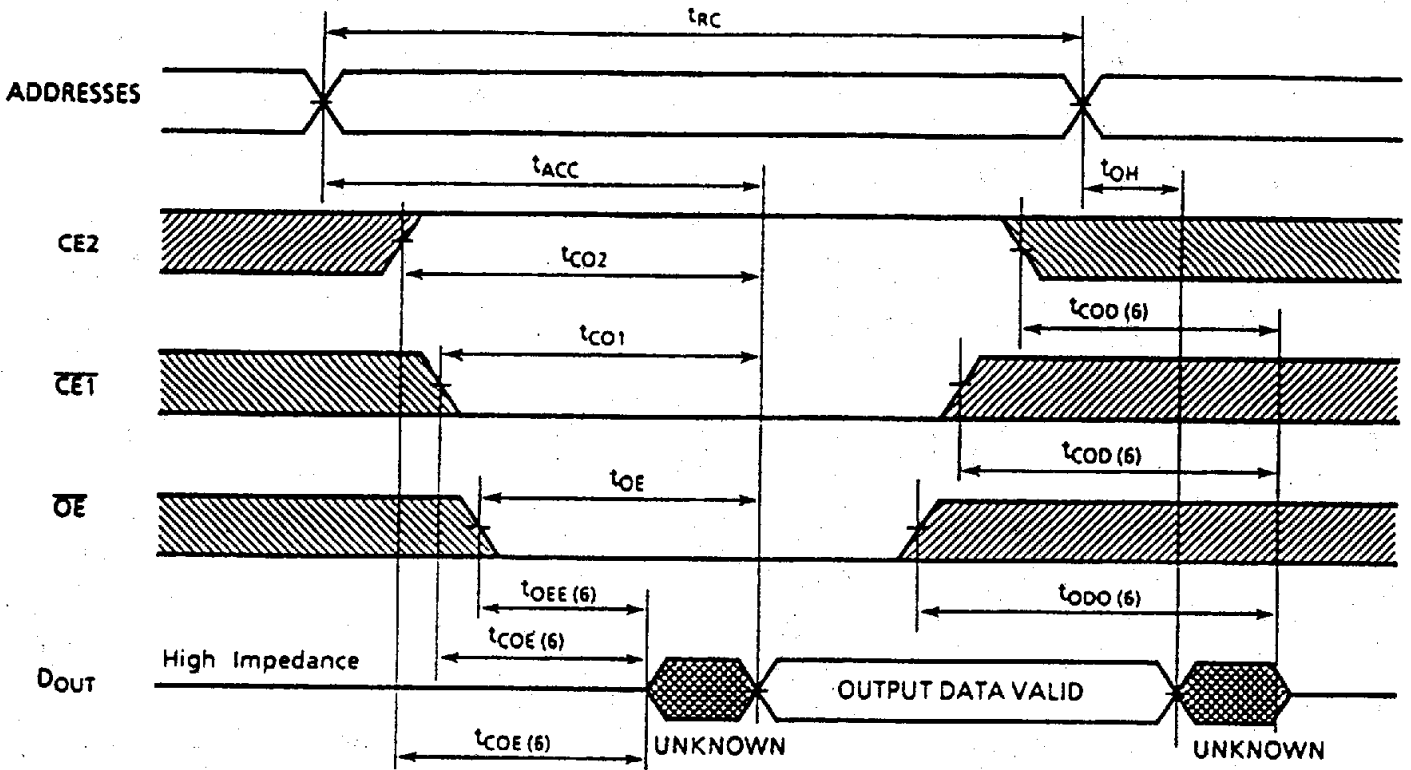


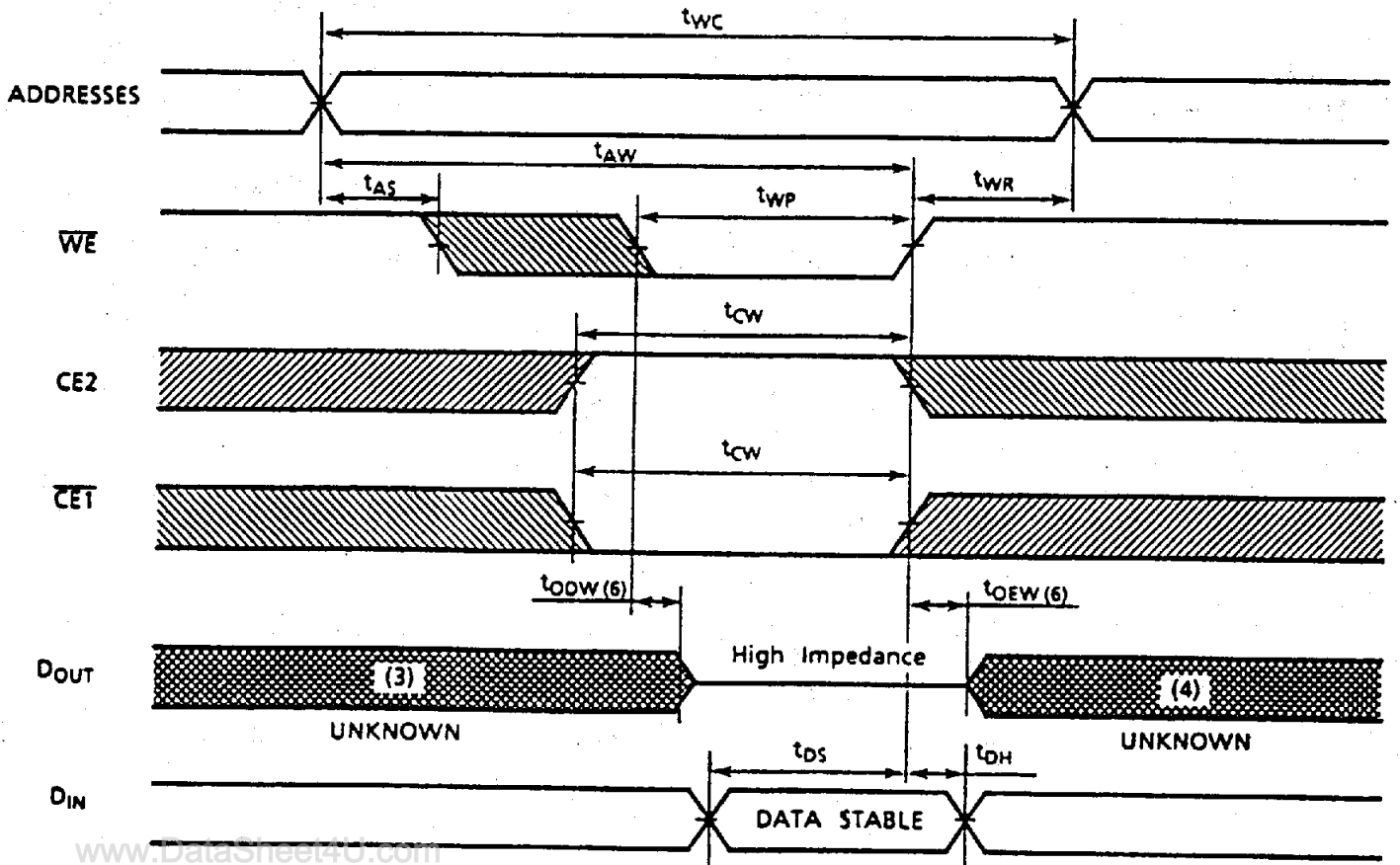
Figure 1.

Timing Waveforms

Read Cycle ⁽²⁾

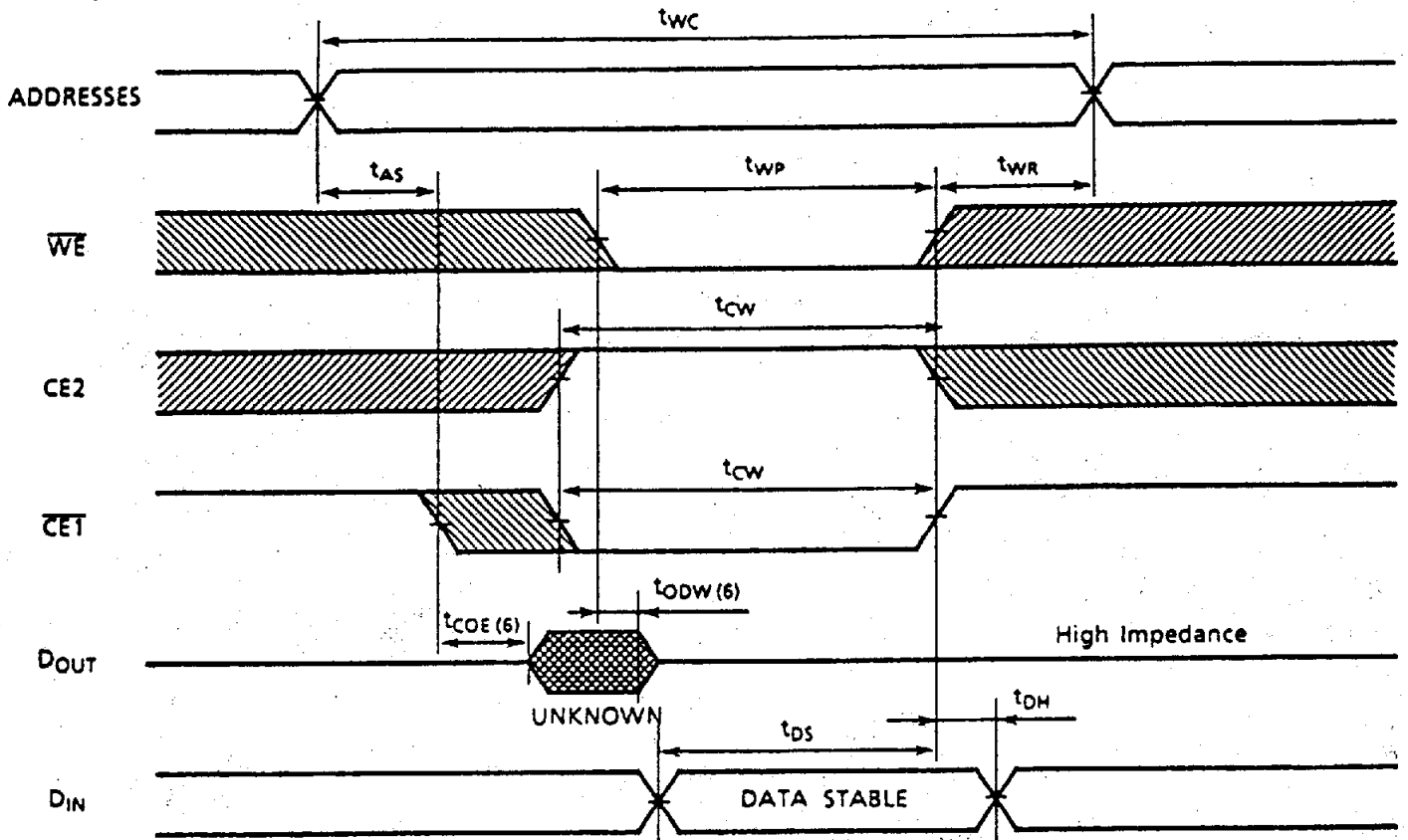


Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)

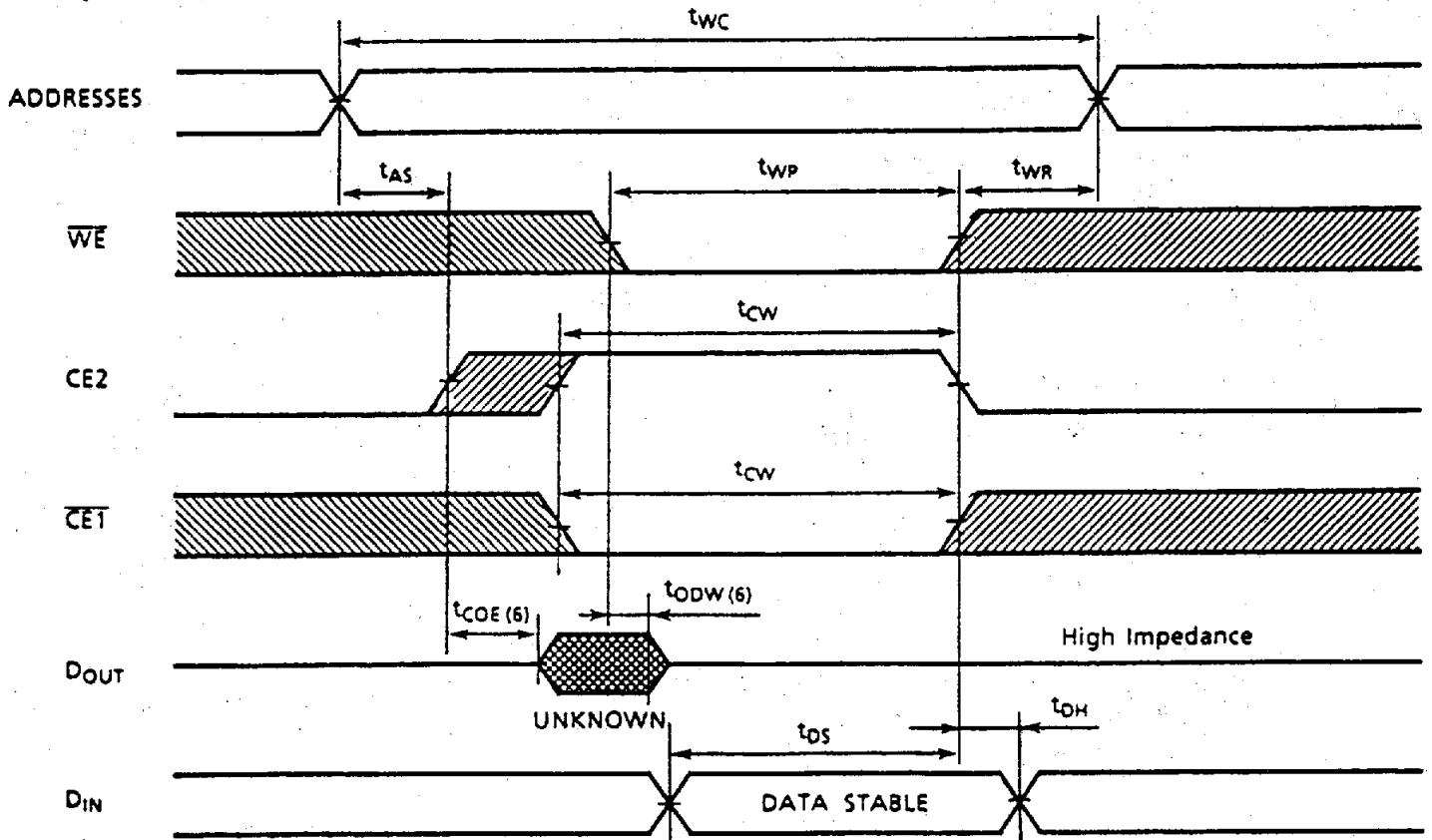


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Write Cycle 2 ⁽⁵⁾ ($\overline{\text{CE1}}$ Controlled Write)



Write Cycle 3 ⁽⁵⁾ (CE2 Controlled Write)



Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or CE2 high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or CE2 low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , t_{OEw} Output Enable Time
 - (B) t_{COD} , t_{ODO} , t_{ODW} Output Disable Time

