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Product Specification

1.5" COLOR TFT-LCD MODULE

MODEL NAME: A015AN04 V4

FOR GLEICHMANN INTERNAL USE ONLY

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

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A. Physical specifications

| NO. | Item | Specification | Remark |
|-----|-------------------------|--------------------------|--------|
| 1 | Display resolution(dot) | 280(W) ×220(H) | |
| 2 | Active area(mm) | 29.96(W) ×22.66(H) | |
| 3 | Screen size(inch) | 1.48(Diagonal) | |
| 4 | Dot pitch(mm) | 0.107(W) ×0.103(H) | |
| 5 | Color configuration | R. G. B. delta | |
| 6 | Overall dimension(mm) | 37.06(W) ×34(H) ×3.04(D) | Note 1 |
| 7 | Weight(g) | 6 Typ. | |
| 8 | Panel surface treatment | Hard coating (3H) | |

Note 1: Refer to Fig. 4

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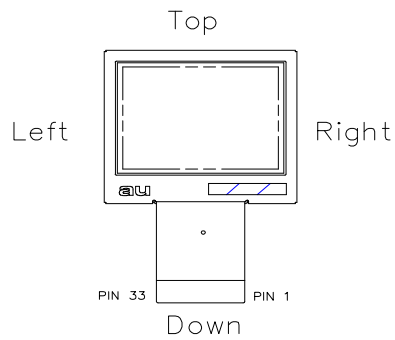
B. Electrical specifications

1.Pin assignment

| Pin no | Symbol | I/O | Description | Remark |
|--------|-----------|-----|---|--------|
| 1 | VCOM | I | Common electrode driving signal | |
| 2 | VGH | P | Positive power for scan driver | |
| 3 | V1 | C | Power setting capacitor connect pin | |
| 4 | V2 | C | Power setting capacitor connect pin | |
| 5 | Vgoff_H | PS | Negative power supply (High) for G1~G240 outputs | |
| 6 | Vgoff_L | PS | Negative power supply (Low) for G1~G240 outputs | |
| 7 | V3 | C | Power setting capacitor connect pin | |
| 8 | V4 | C | Power setting capacitor connect pin | |
| 9 | AVDD1 | P | FRP level supply | |
| 10 | FRP | O | Frame polarity output for panel Vcom | |
| 11 | GND | P | Ground pin for digital circuits | |
| 12 | DRV | VO | Power transistor gate signal for the boost converter | |
| 13 | LED Anode | I | LED Anode | |
| 14 | FB | VI | Main boost regulator feedback input | |
| 15 | VCC | P | Power supply for digital circuits | |
| 16 | AGND | P | Ground pin for analog circuits | |
| 17 | AVDD | P | Power supply for analog circuits | |
| 18 | HSYNC | I | Horizontal sync input. Negative polarity | |
| 19 | VSYNC | I | Vertical sync input. Negative polarity | |
| 20 | DCLK | L | Clock signal; latch data onto line latches at the rising edge | |
| 21 | DD5 | I | Data input: MSB | |
| 22 | DD4 | I | Data input | |
| 23 | DD3 | I | Data input | |
| 24 | DD2 | I | Data input | |
| 25 | DD1 | I | Data input | |
| 26 | DD0 | I | Data input: LSB | |
| 27 | NC | I | NC | |
| 28 | GRB | I | Global reset pin | |
| 29 | CS | I | Serial communication chip select | Note2 |
| 30 | ISDA | I | Serial communication data input | Note2 |
| 31 | ISCL | I | Serial communication clock input | Note2 |
| 32 | VCC | P | Power supply for digital circuits | |
| 33 | GND | P | Ground pin for digital circuits | |

I: Input; O: Output. VI: voltage input VO: voltage output P:Power.

Note 1 : Definition of scanning direction. Refer to figure as below



Note 2 :Please refer to application note for 3-wire serial communication setting

2. Equivalent circuit of I/O

| Pin no & Pin name | Schematics |
|--|------------|
| 12.DRV | |
| 21.DD5 22.DD4 23.DD3 24.DD2 25.DD1 26.DD0 | |
| 28.GRB | |

3. Absolute maximum ratings

| Item | Symbol | Condition | Min. | Max. | Unit | Remark |
|-----------------------|-----------|-------------|------|------|------|---------------------|
| Power voltage | V_{CC} | GND=0 | -0.5 | 5. | V | |
| | AV_{DD} | $AV_{SS}=0$ | -0.5 | 5.5 | V | |
| Input signal voltage | VCOM | | -2.9 | 5.6 | V | |
| Operating temperature | Topa | | 0 | 60 | °C | Ambient temperature |
| Storage temperature | Tstg | | -25 | 80 | °C | Ambient temperature |

4. Electrical characteristics

a. Typical operating conditions (GND= $AV_{SS}=0V$)

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-------------------------|-----------|----------|--------------|---------|-------------|-----------------|
| | V_{CC} | 3.0 | 3.3 | 3.6 | V | |
| | AV_{DD} | 3.0 | 3.3 | 3.6 | V | |
| Output Signal voltage | H Level | V_{OH} | $V_{CC}-0.4$ | | | |
| | L Level | V_{OL} | GND | GND+0.4 | | |
| Input Signal voltage | H Level | V_{IH} | $0.7V_{CC}$ | - | V_{CC} | V |
| | L Level | V_{IL} | GND | - | $0.3V_{CC}$ | V |
| Output current | H Level | IOH | 10 | | | uA |
| | L Level | IOL | -10 | | | uA |
| Analog stand by current | Ist | | | 200 | uA | DCLK is stopped |

b. Current consumption (GND= $AV_{SS}=0V$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|-----------|----------|----------------|------|------|------|------|--------|
| | I_{CC} | $V_{CC}=3.3V$ | - | 2 | 2.5 | mA | |
| | I_{DD} | $AV_{DD}=3.3V$ | - | 1.5 | 2.0 | mA | |

c. LED driving conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------|--------|-------|------|------|------|----------|
| LED current | | | 20 | 25 | mA | |
| LED voltage | V_L | 6.6 | 7.8 | 8.6 | V | Note1 |
| LED Life Time | L_L | 10000 | | | Hr | Note 2,3 |

Note 1 : Max.voltage :1pcs/4V, FB=0.6V, VL=LED anode(PIN 13)

Note 2 : Ta. = 25°C, I_L = 20mA

Note 3 : Brightness to be decreased to 50% of the initial value

5. AC Timing

a. UPS051 Timing conditions

| Parameter | | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|----------------------------|-----------------------------|----------------|------|-------|--------|----------------|--------|
| DCLK | Frequency | 1/Tvc | | 5.67 | | MHZ | |
| | High time | Tvch | 15 | | | ns | |
| | Low time | Tvcl | 15 | | | ns | |
| Rising time | | t _r | - | - | 10 | ns | Note 1 |
| Falling time | | t _f | - | - | 10 | ns | Note 1 |
| HSYNC | Period | TH | 60 | 63.56 | 67 | us | Note 2 |
| | | | | 360 | | DCLK | |
| | Display period | THd | | 49.4 | | us | |
| | Pulse width | THp | 1 | 25 | | DCLK | |
| HSYNC-Clk timing | | THc | 15 | | Tvc-15 | ns | |
| Hsync setup time | | Tvst | 12 | | | ns | |
| Hsync hold time | | Thhd | 12 | | | ns | |
| Horizontal lines per field | | t _v | 256 | 262 | 268 | t _H | |
| VSYNC | Period | TV | | 16.6 | | ms | Note 2 |
| | | | | 262 | | t _H | |
| | Display period | TVd | | 13.97 | | ms | |
| | Pulse width | TVp | 1 | | | DCLK | |
| | | | 3 | | TH | | |
| Vsync setup time | | Tvst | 12 | | | ns | |
| Vsync hold time | | Tvhhd | 12 | | | ns | |
| DATA D00~D05 | DCLK-DATA timing | Tds | 10 | - | - | ns | |
| | DATA-CLK timing | Tdh | 10 | - | - | ns | |
| | Rising time Falling time | Tdrf | - | - | 10 | ns | |

Note 1: For all of the logic signals.

Note 2: Display position

a-1 Horizontal display position

The display starts from the data of (57DCLK, TH=57DCLK) as shown in Fig 5.

(TH : From Hsync falling edge to 1st displayed data.)

a-2. Vertical display position

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------------------|--------|------|------|------|------|--------|
| Vertical display position | TVS | | 25 | | TH | NTSC |

a-3 Timing diagram

Please refer to the attached drawing, from Fig.6 to Fig.6 to Fig.10

b. UPS052 Timing conditions

| Parameter | | Symbol | Min. | Typ. | Max. | Unit. | Remark |
|----------------------------|-----------------------------|----------------|------|-------|-------|----------------|--------|
| DCLK | Frequency | 1/Tvc | | 24.54 | | MHz | |
| | High time | Tvch | 10 | | | ns | |
| | Low time | Tvcl | 10 | | | ns | |
| Rising time | | t _r | - | - | 10 | ns | Note 1 |
| Falling time | | t _f | - | - | 10 | ns | Note 1 |
| HSYNC | Period | TH | 60 | 63.56 | 67 | us | Note 2 |
| | | | | 1560 | | DCLK | |
| | Display period | THd | | 49.4 | | us | |
| | Pulse width | THp | 1 | 25 | | DCLK | |
| HSYNC-Clk timing | | THc | 15 | | Tc-15 | ns | |
| Hsync setup time | | Tvst | 4 | | | ns | |
| Hsync hold time | | Thhd | 12 | | | ns | |
| Horizontal lines per field | | t _v | 256 | 262 | 268 | t _H | |
| VSYNC | Period | TV | | 16.6 | | ms | Note 2 |
| | | | | 262 | | t _H | |
| | Display period | TVd | 4 | 13.97 | | ms | |
| | Pulse width | TVp | 1 | | | DCLK | |
| | | | 3 | | TH | | |
| Vsync setup time | | Tvst | 12 | | | ns | |
| Vsync hold time | | Tvhd | 12 | | | ns | |
| DATA D00~D05 | DCLK-DATA timing | Tds | 10 | - | - | ns | |
| | DATA-CLK timing | Tdh | 10 | - | - | ns | |
| | Rising time Falling time | Tdrf | - | - | 10 | ns | |
| Data set-up time | | Tds | 4 | | | ns | |
| Data hold time | | Tdh | 12 | | | ns | |

Note 1: For all of the logic signals.

Note 2: Display position

b-1 Horizontal display position

The display starts from the data of (269DCLK, TH=268DCLK) as shown in Fig 11.

 (TH : From Hsync falling edge to 1st displayed data.)

b-2 Vertical display position

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------------------|--------|------|------|------|------|--------|
| Vertical display position | TVS | | 25 | | TH | NTSC |

b-3 Timing diagram

Please refer to the attached drawing, from Fig.9 to Fig.15

6. 3-wire serial communications

For 3-wire serial communication timing ,as shown in Fig16 ,for register setting, please refer to application note.

7. DC-DC Converter Circuit

A015AN04 contains one high-power step-up DC-DC converter, and backplane drive circuitry for active matrix TFT LCDs. The output voltage of the main boost converter can be set from VCC to 13.5V with external resistors. Also included in A015AN04 are a precision 0.6V reference voltage, fault detection and logic shutdown.

a .Boost Converter

A015AN04 main boost converter uses a boost PWM architecture to produce a positive regulated voltage, Please refer to figure1 for the DC-DC converter block diagram.

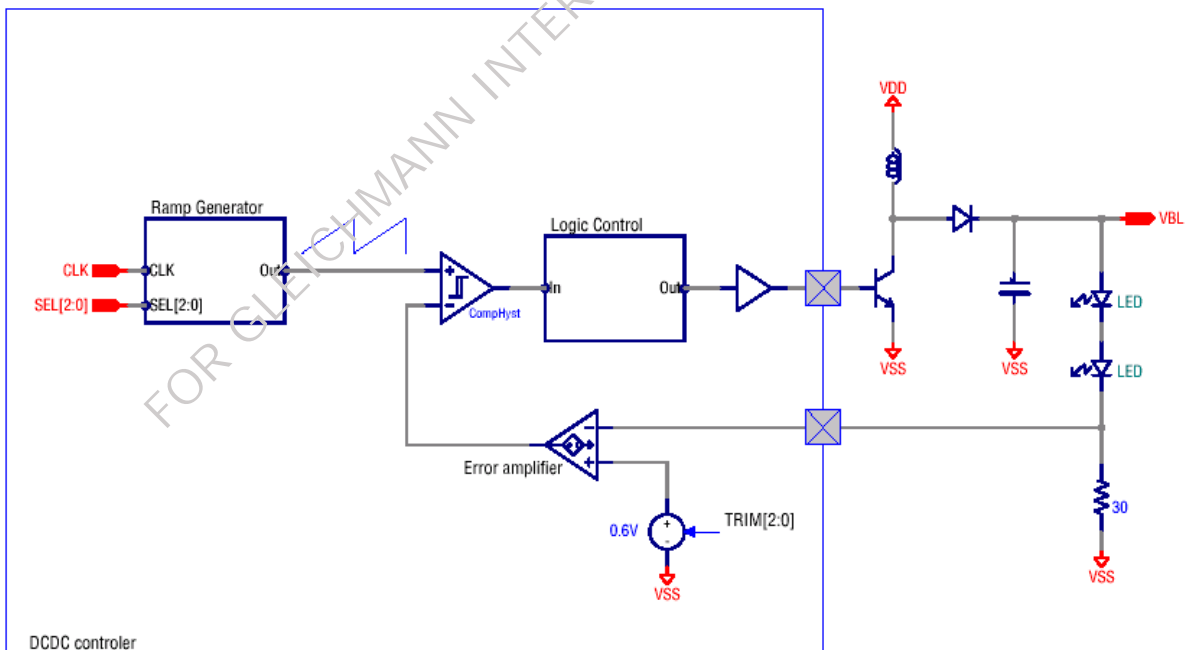


Fig 1 Dc-Dc converter block diagram

In the internal architecture of DC-DC converter as Fig2 showed. The feedback voltage(VFB) will connect to the tri-angle waveform comparator ,and generates the output signal (CP0) which determines the duty cycle for (Fdc).

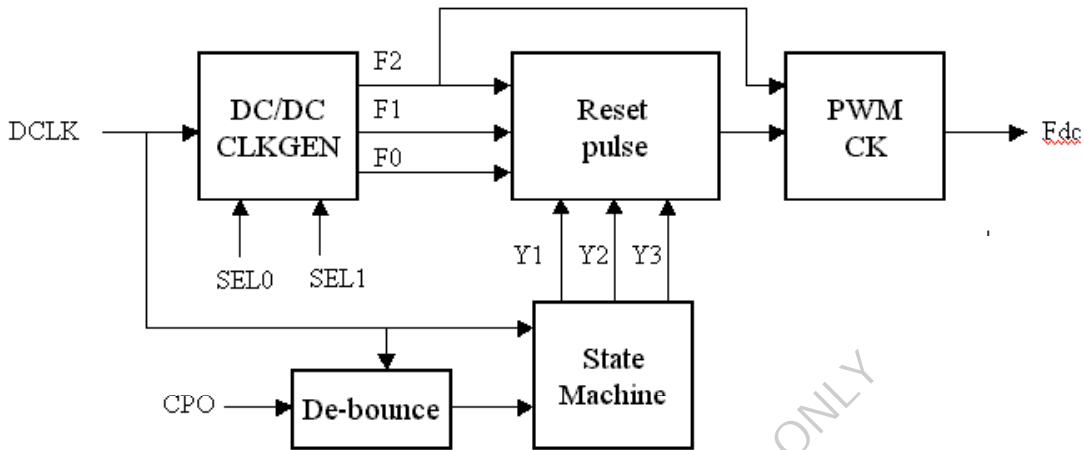


Fig 2 DC CK block diagram

To reduce the noise affect,CP0 will processed by De-bounce circuit. State-machine will generate the duty cycle by CP0 signal. To make sure that VFB can reach default VREF quickly, so State-machine's is designed as a discrete step by step function. please refer to Fig 3. If CP0 is low , Duty cycle will work from 0% to 75%. The maximum duty ratio is 75%.

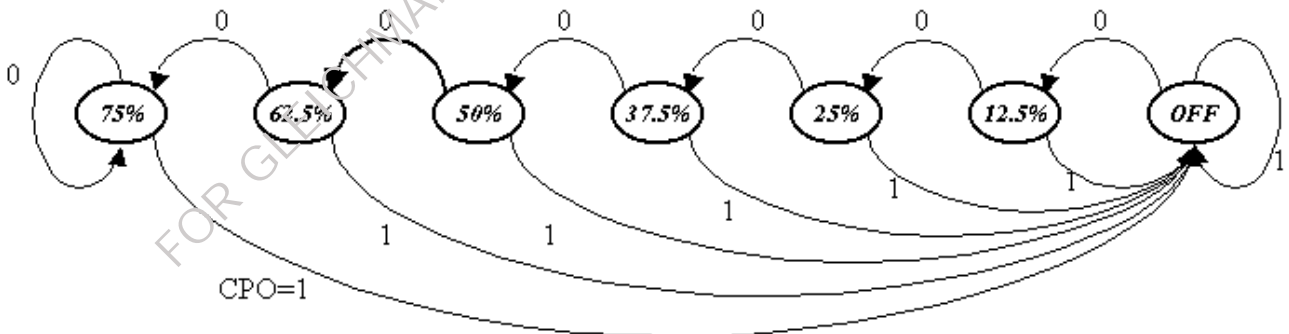


Fig 3 PWM Control state diagram

C. Optical specification (Note 1,Note 2, Note 3)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|--------------------|--------|----------------------------|--------|--------|--------|----------|----------|
| Response time | Rise | $\theta = 0^\circ$ | - | 25 | 50 | ms | Note 4 |
| | Fall | | - | 30 | 60 | ms | |
| Contrast ratio | CR | At optimized viewing angle | 60 | 150 | - | | Note 5,6 |
| Viewing angle | Top | $CR \geq 10$ | 10 | - | - | deg. | Note 7 |
| | Bottom | | 30 | - | - | | |
| | Left | | 40 | - | - | | |
| | Right | | 40 | - | - | | |
| Brightness | Y_L | $\theta = 0^\circ$ | 120 | 180 | - | cd/m^2 | Note 8 |
| White chromaticity | X | $\theta = 0^\circ$ | (0.26) | (0.31) | (0.36) | | |
| | y | $\theta = 0^\circ$ | (0.29) | (0.35) | (0.40) | | |

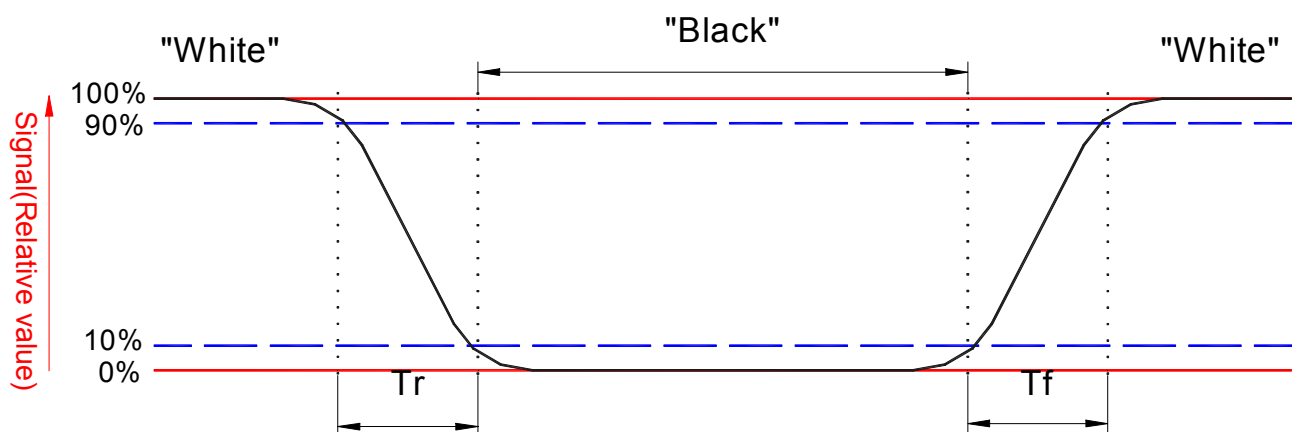
Note 1. Ambient temperature =25°C

Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White $V_i = V_{i50} \mp 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

"±" Means that the analog input signal swings in phase with COM signal.

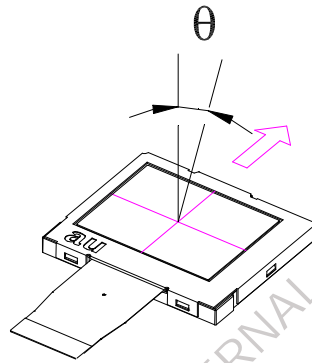
“ $-$ ” Means that the analog input signal swings out of phase with COM signal.

V_{i50}^+ : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:

Refer to figure as below.



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

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D. Reliability test items:

| No. | Test items | Conditions | Remark |
|-----|------------------------------------|---|---------------|
| 1 | High temperature storage | Ta= 80°C 240Hrs | |
| 2 | Low temperature storage | Ta= -25°C 240Hrs | |
| 3 | High temperature operation | Ta= 60°C 240Hrs | |
| 4 | Low temperature operation | Ta= 0°C 240Hrs | |
| 5 | High temperature and high humidity | Ta= 60°C . 90% RH 240Hrs | Operation |
| 6 | Heat shock | -25°C~80°C/50 cycle 2Hrs/cycle | Non-operation |
| 7 | Electrostatic discharge | ±200V,200pF(0Ω), once for each terminal | Non-operation |
| 8 | Vibration (with carton) | Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/Octave from 200~500Hz | IEC 68-34 |
| 9 | Drop (with carton) | Height: 60cm 1 corner, 3 edges, 6 surfaces | |

Note: Ta: Ambient temperature.

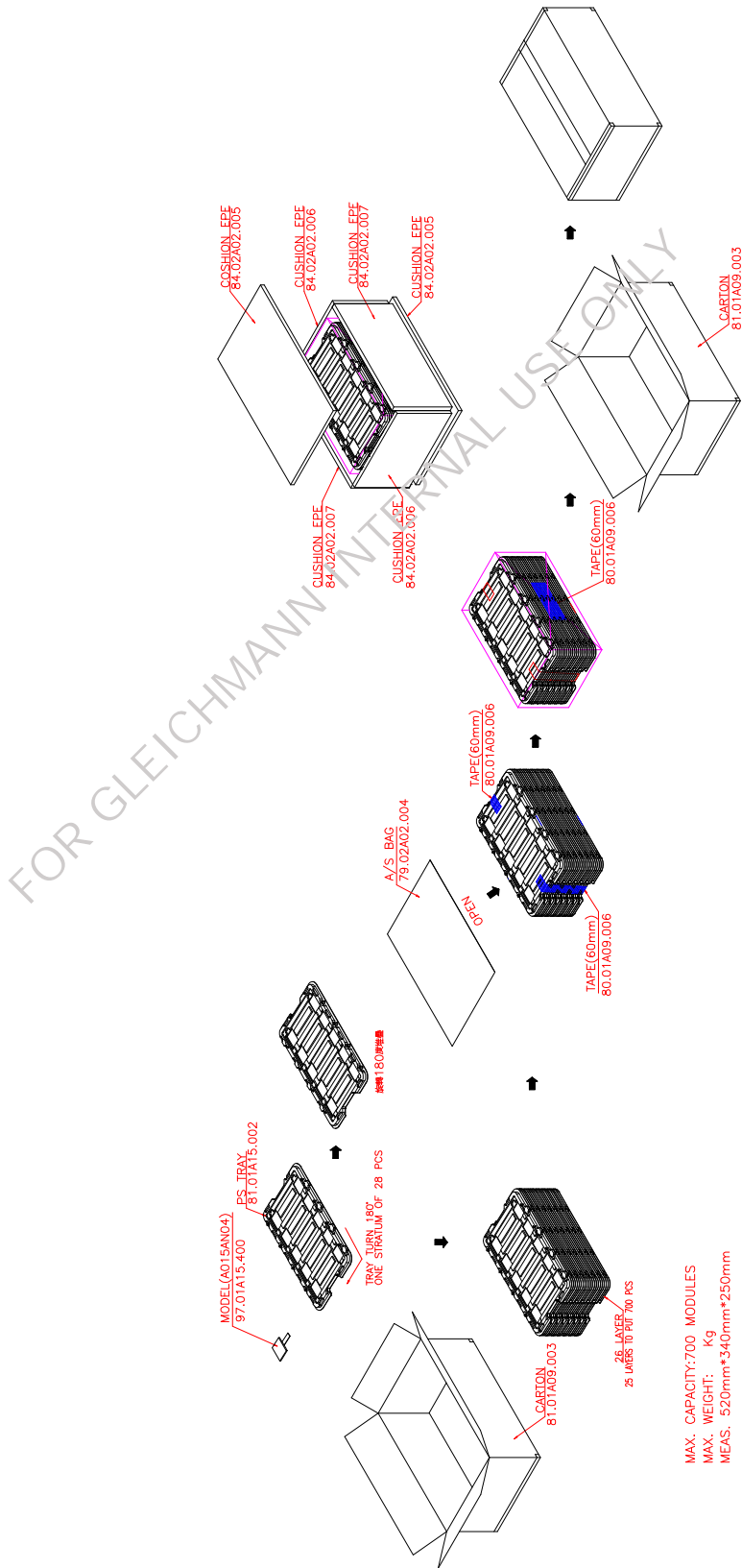
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E. Packing form

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MAX. CAPACITY:700 MODULES
MAX. WEIGHT: Kg
MEAS. 520mm*340mm*250mm

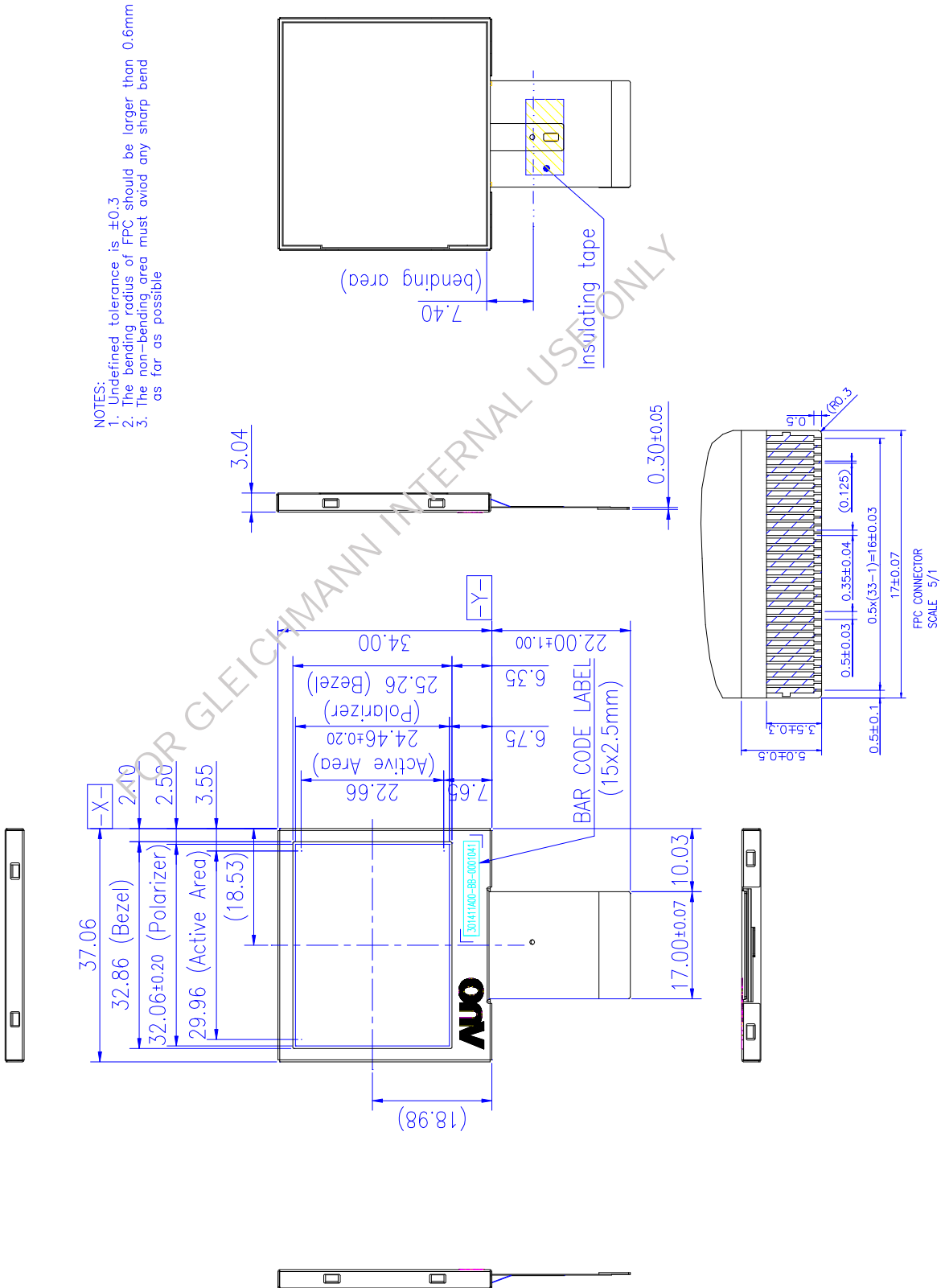


Fig. 4 Outline dimension of TFT-LCD module

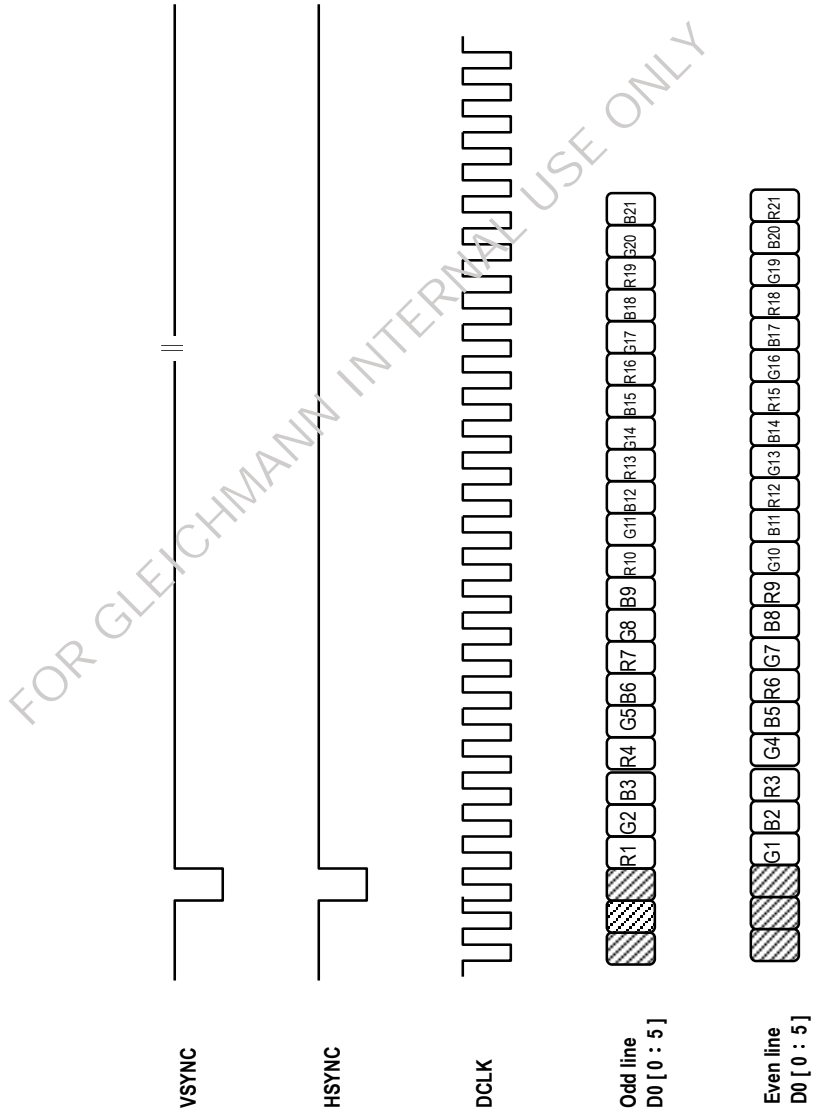


Fig. 5 UPS051 Input signals timing relationship

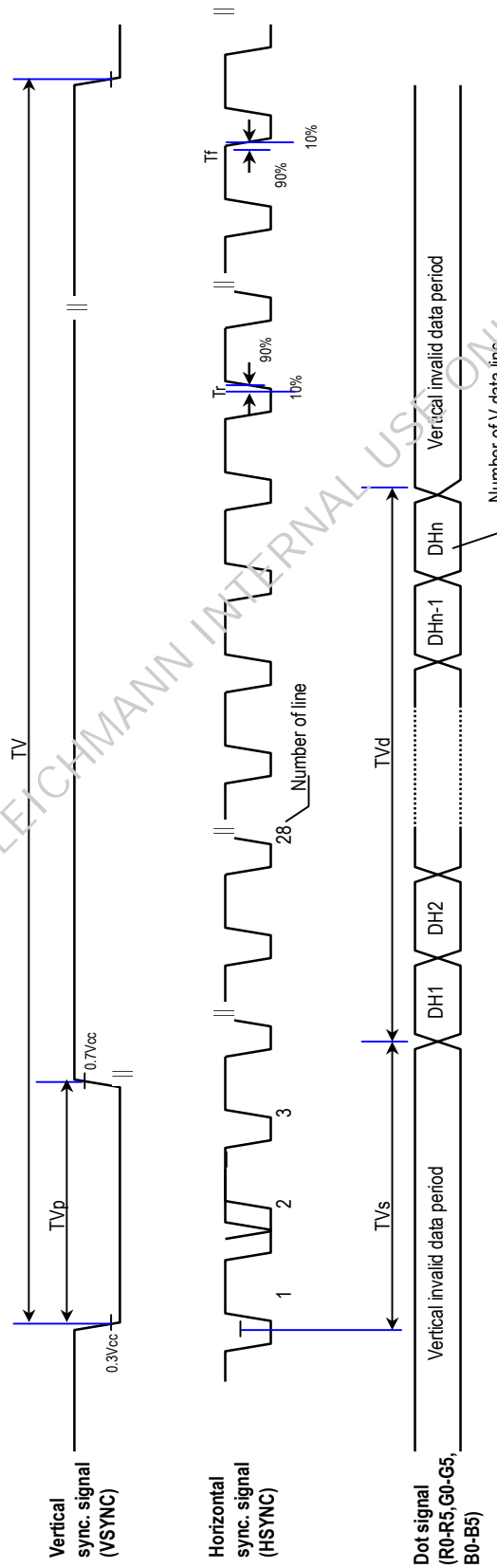


Fig .6 UPS051 Input Vertical Timing

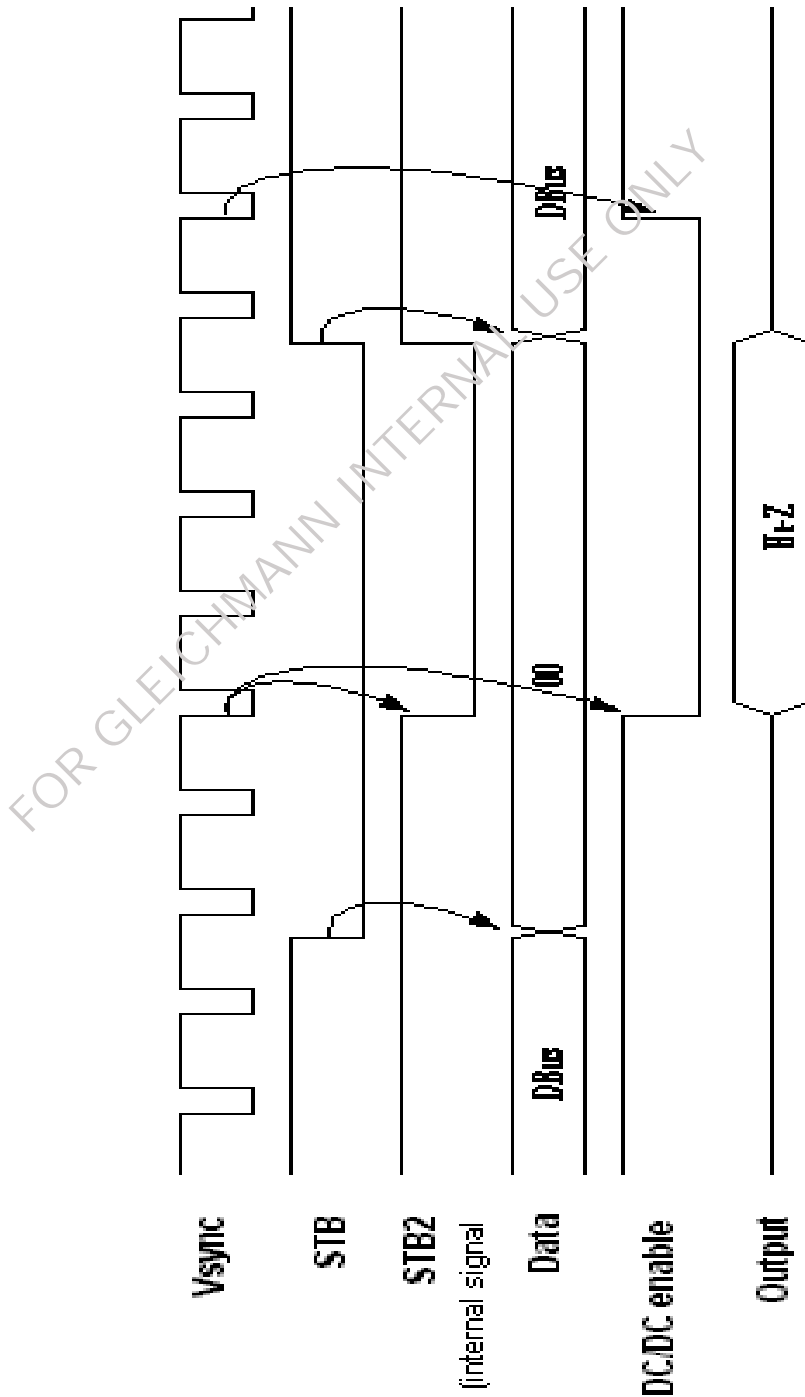
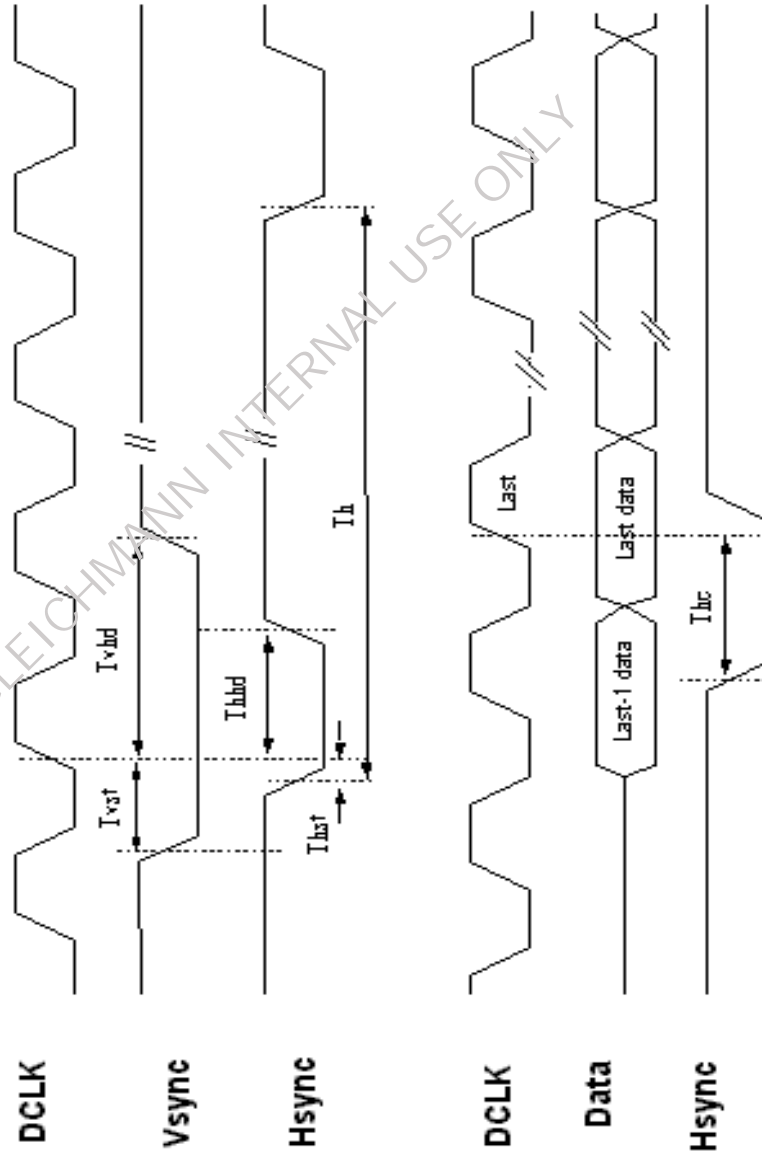


Fig.9 UPS051/UPS052 Standby Mode Timing



1 Fig 10. UPS051/UPS052 Hsync,Vsync,Data,DCLK relationship

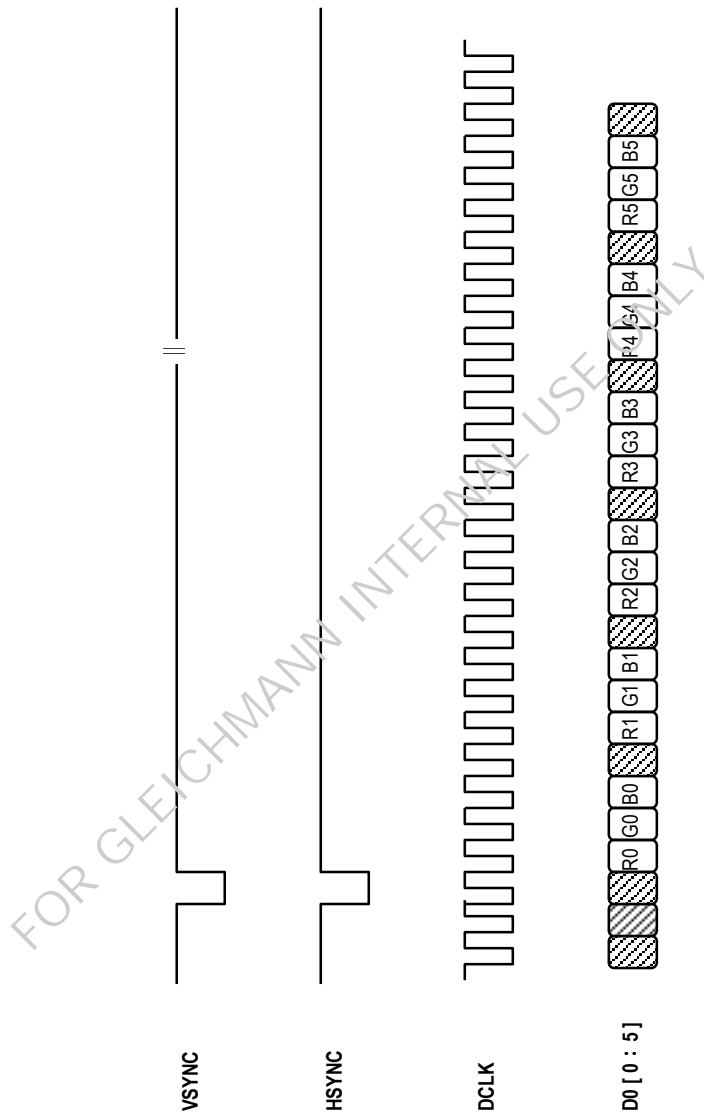


Fig. 11 UPS052 input signals timing relationship

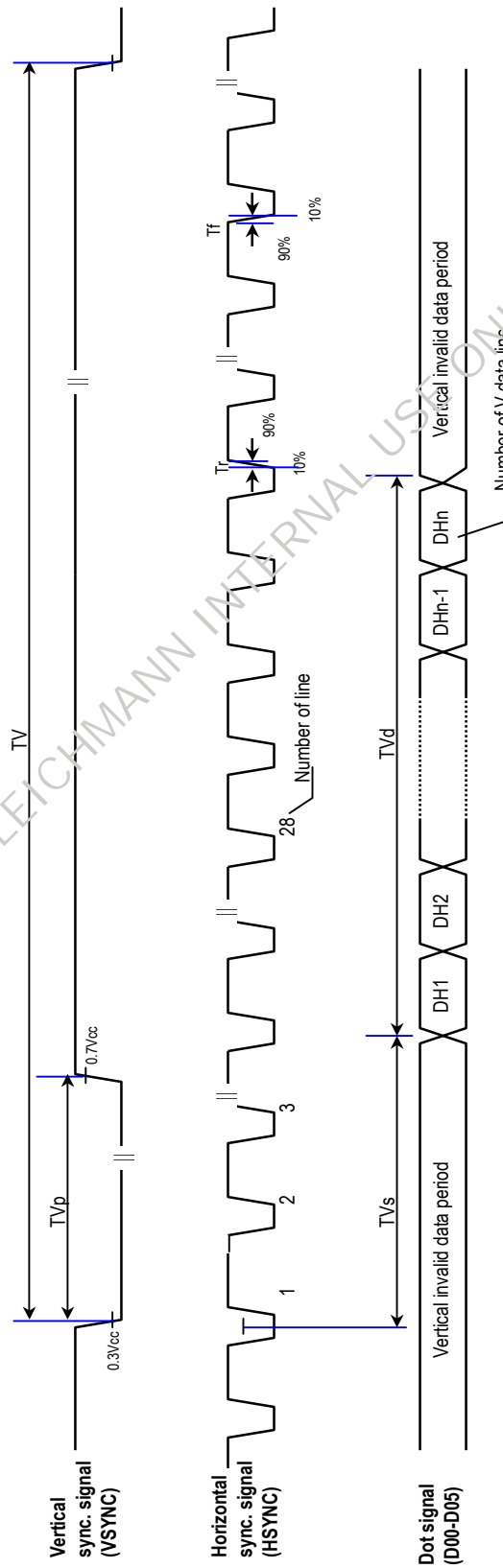
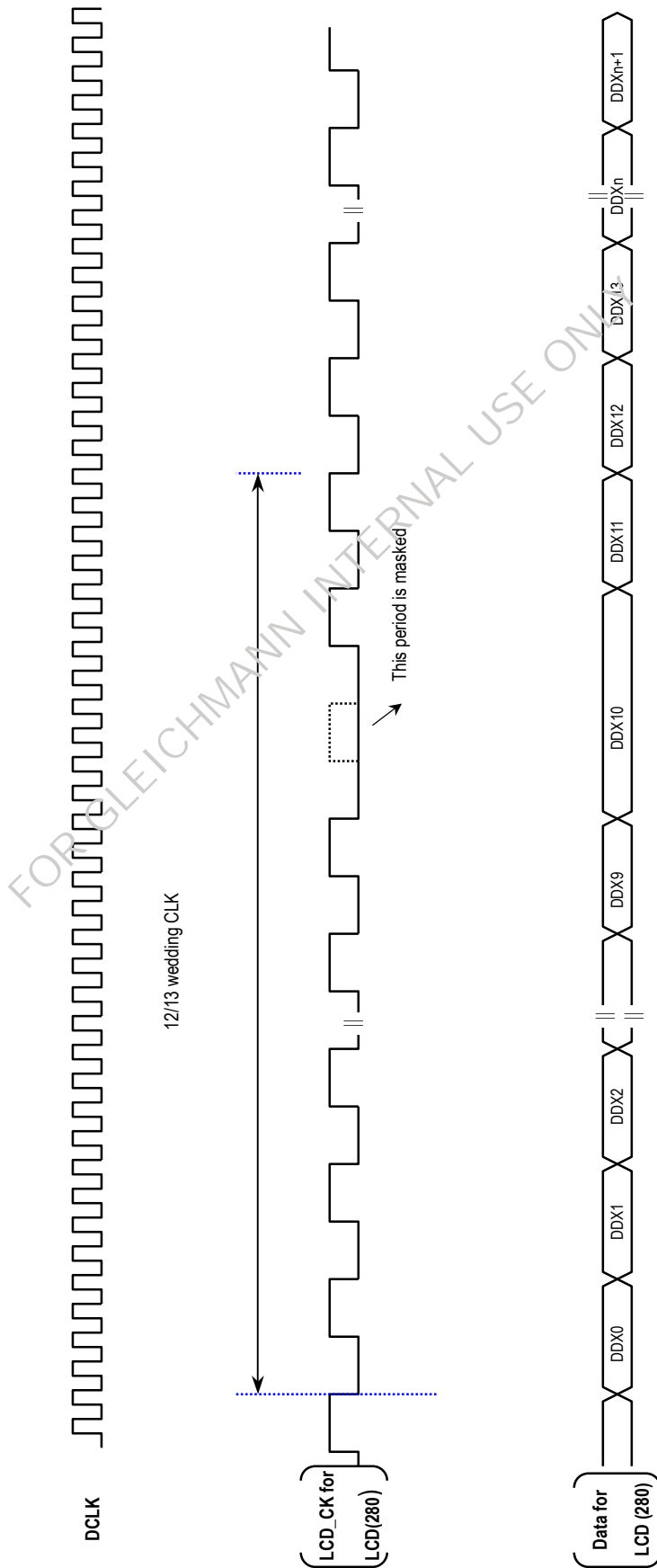


Fig. 12 UPS052 Input Vertical Timing



**Fig.14 UPS052 Horizontal Input Timing
(Wedding CLK Explanation)**

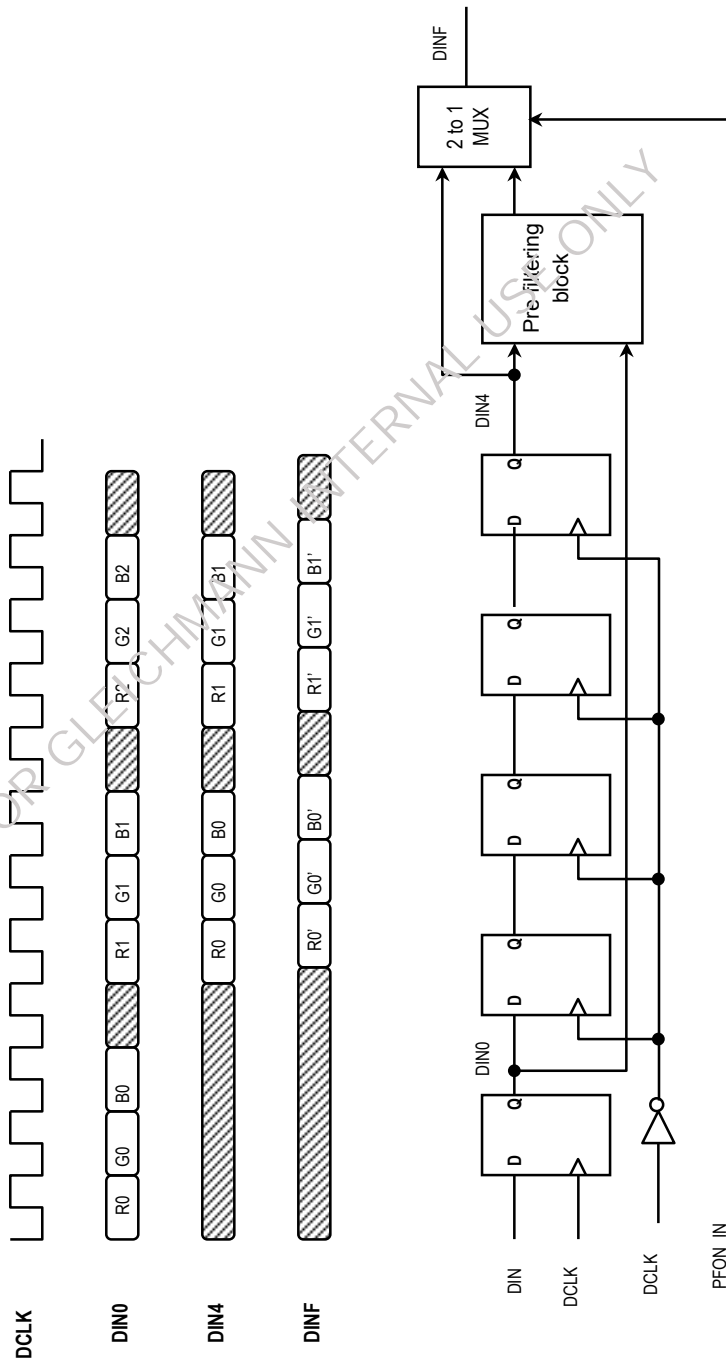


Fig.15 UPS052 Pre-filtering function timing diagram and block diagram

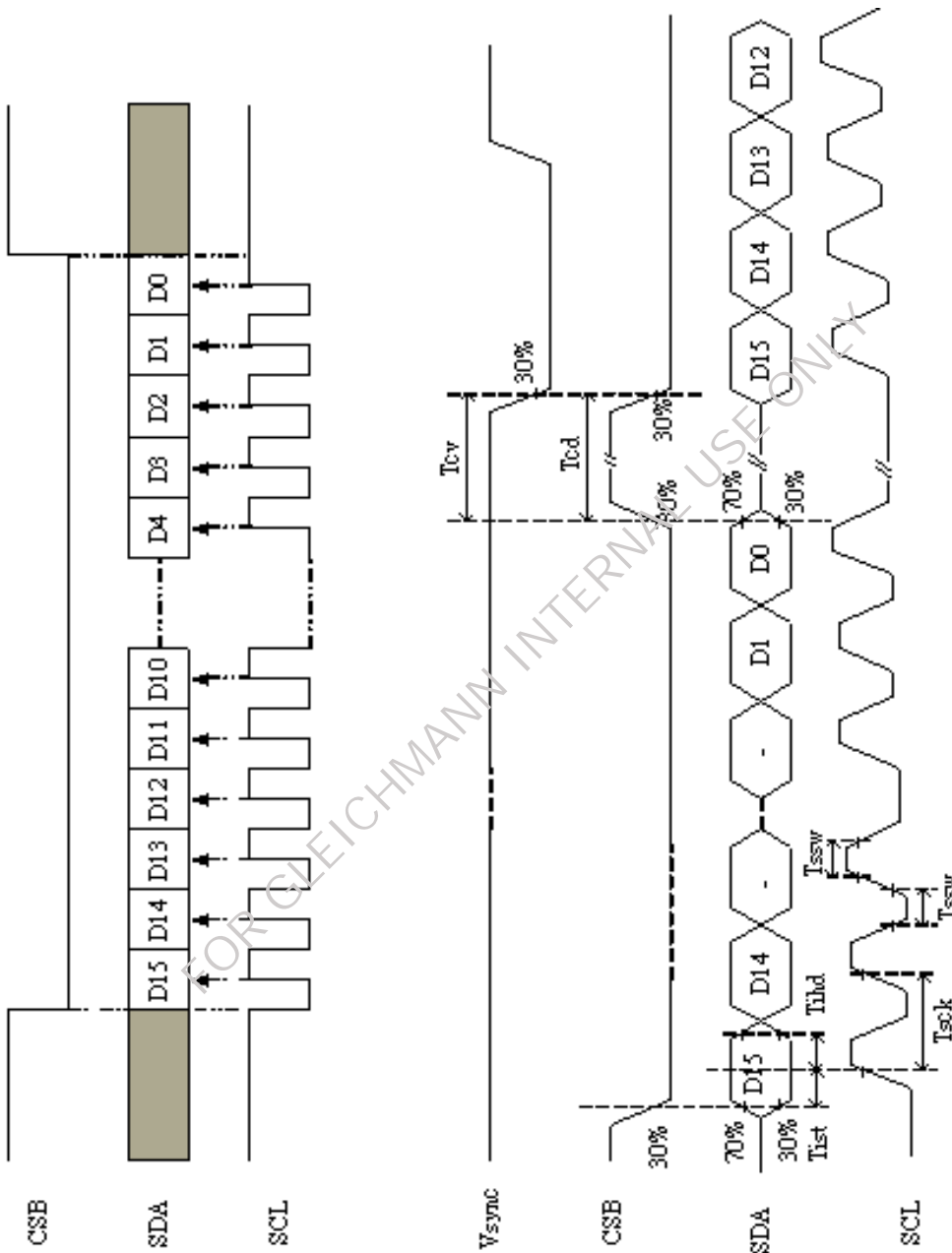


Fig.16 3-wire programming function Timing

H. Application Notes

A015AN04 is designed with smart integration advance (SIA) concept for DSC application. This panel integrated not only source driver & gate driver, but also built in power generator and embedded serial communication interface for function setting.

Two kinds of input timing format: UPS051 and UPS052 are supported to A015AN04. Customer can use 3-wire serial port for setting register and select different timing for its own feature.

In this document, we list essential parameter for configuration, please follow our recommend setting to achieve the best performance. In the last page, we provide application circuit to drive A015AN04.

For A015AN04 driving circuit design, you just need input one set of power 3.3V, because the charge-pump circuit inside the driver IC produces V_{gh} & V_{gl}. The external peripheral is very simple and good for saving BOM cost for customer.

1. 3-wire serial communication AC timing

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------|------------------|------|------|------|------|
| Serial clock | T _{sck} | 320 | - | | ns |
| SCL pulse duty | T _{scw} | 40 | 50 | 60 | % |
| Serial data setup time | T _{ist} | 120 | - | - | ns |
| Serial data hold time | T _{iht} | 120 | - | - | ns |
| Serial clock high/low | T _{ssw} | 120 | - | - | ns |
| Chip select distinguish | T _{cd} | 1 | - | - | us |
| Time that the CSB to Vsync | T _{cv} | 1 | - | - | us |

2. The configuration of serial data at SDA terminal is at below

MSB

LSB

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|-----|-----|-----|-------------|-----|----|----|----|----|----|----|----|----|----|----|
| Register address | | | X | DATA | | | | | | | | | | | |

3. Recommend register table for UPS051 timing

| No. | Description | Address | | | | | | | | | | | | | | | |
|-----|--------------------|---------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| | | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R0 | Scan direction | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 |
| R1 | Data setting | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 |
| R2 | Source IC setting | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | 1 | 1 | 0 | 0 |
| R3 | Timing select | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 |
| R4 | VCAC level setting | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | 1 | 1 | 0 | 0 |

“X” => Don't care.

4.Recommend register table for UPS052 timing

| No. | Description | Address | | | | MSB LSB | | | | | | | | | | | |
|-----|--------------------|---------|-----|-----|-----|------------|-----|----|----|----|----|----|----|----|----|----|----|
| | | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R0 | Scan direction | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 |
| R1 | Data setting | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 |
| R2 | Source IC setting | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | 1 | 1 | 0 | 0 |
| R3 | Timing select | 0 | 1 | 1 | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 1 |
| R4 | VCAC level setting | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | 1 | 1 | 0 |

“X” => Don't care.

5.Register detail description

a. Register R0

| Bit | Function |
|-----|--|
| D0 | Up/down scan direction. “0”=> Down to up. “1”=> Up to down. |
| D1 | Left/Right scan direction. “0”=> Left to right. “1”=>Right to left. |

b. Register R1

| Bit | Function |
|-----|--|
| D0 | “0”=>When UPS051 mode selected. “1”=>When UPS052 mode selected. |
| D1 | Always fixed at “0” |

c. Register R2

| Bit | Function |
|-----|--|
| D0 | Always fixed at “0”. |
| D1 | Always fixed at “0”. |
| D2 | Standby mode setting. “0”=> Turn off driver & DCDC. “1”=> Normal operating. |
| D3 | Always fixed at “1” |

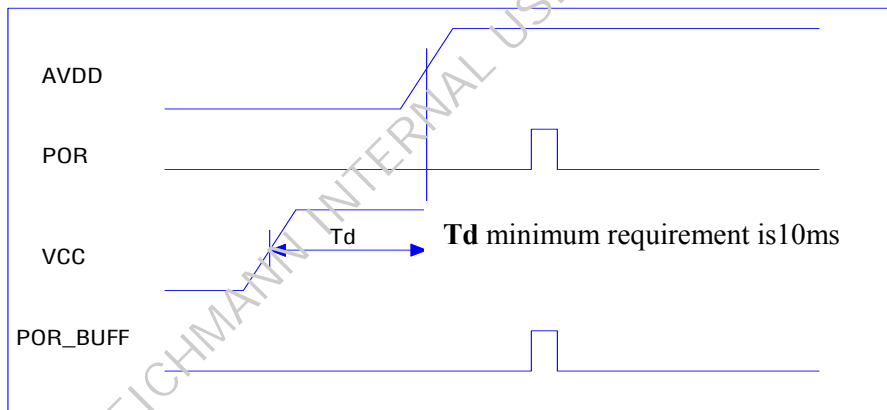
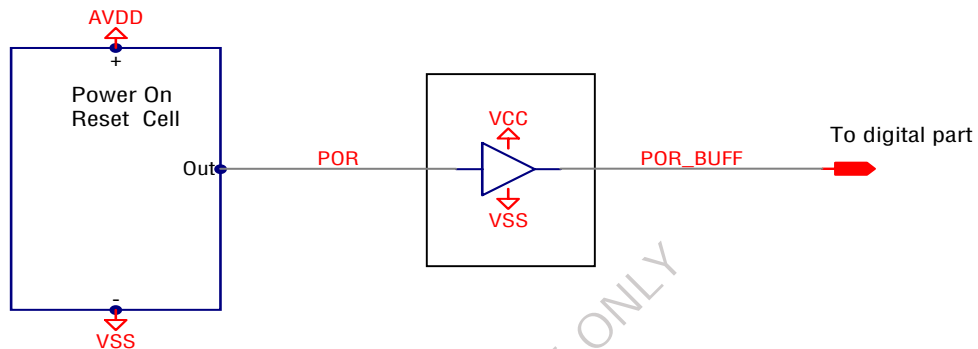
d. Register R3

| Bit | Function |
|-----|--|
| D0 | Always fixed at “0”. |
| D1 | Always fixed at “0”. |
| D2 | “0”=> To select UPS051 timing. “1”=> To select UPS052 timing. |

e. Register R4 *

| Bit | Function |
|-----|----------------------|
| D0 | Always fixed at “0”. |

7.Suggestion power on sequence of VCC and AVDD



We strongly recommend separate VCC and AVDD power with 10ms (Min)~30ms(Max) delay period. To make sure power on reset function can work successfully in every time power on.